HY14E10

HY14E ENOB Software User Manual

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1. Software Installation Description

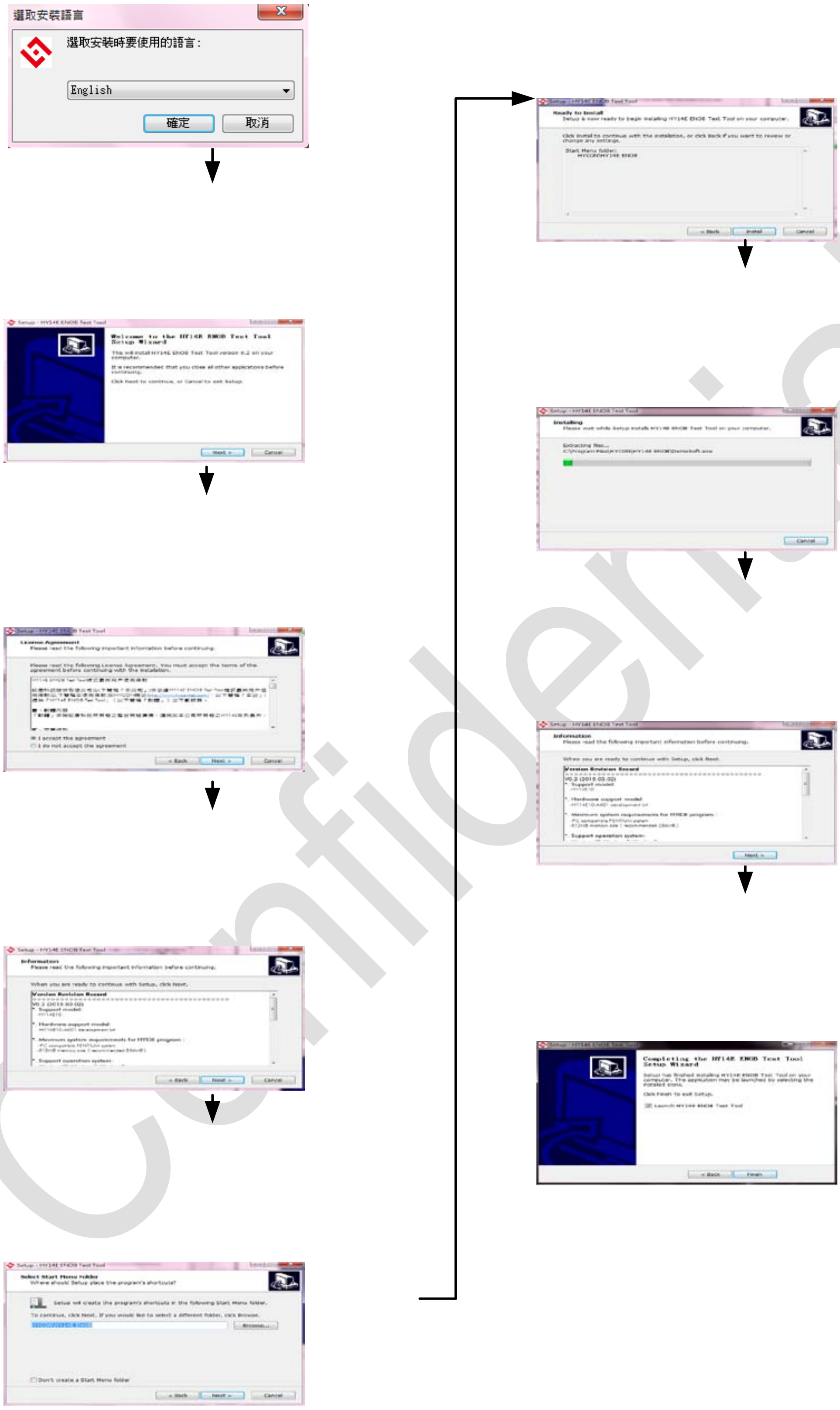

Figure1

2. Software Operation

- Enable HY14EXX test software: Confirm the statuses of the IC and the control panel are “Connect”; if they are “Disconnect”; please directly click the “Disconnect” by the mouse to check their connection status.

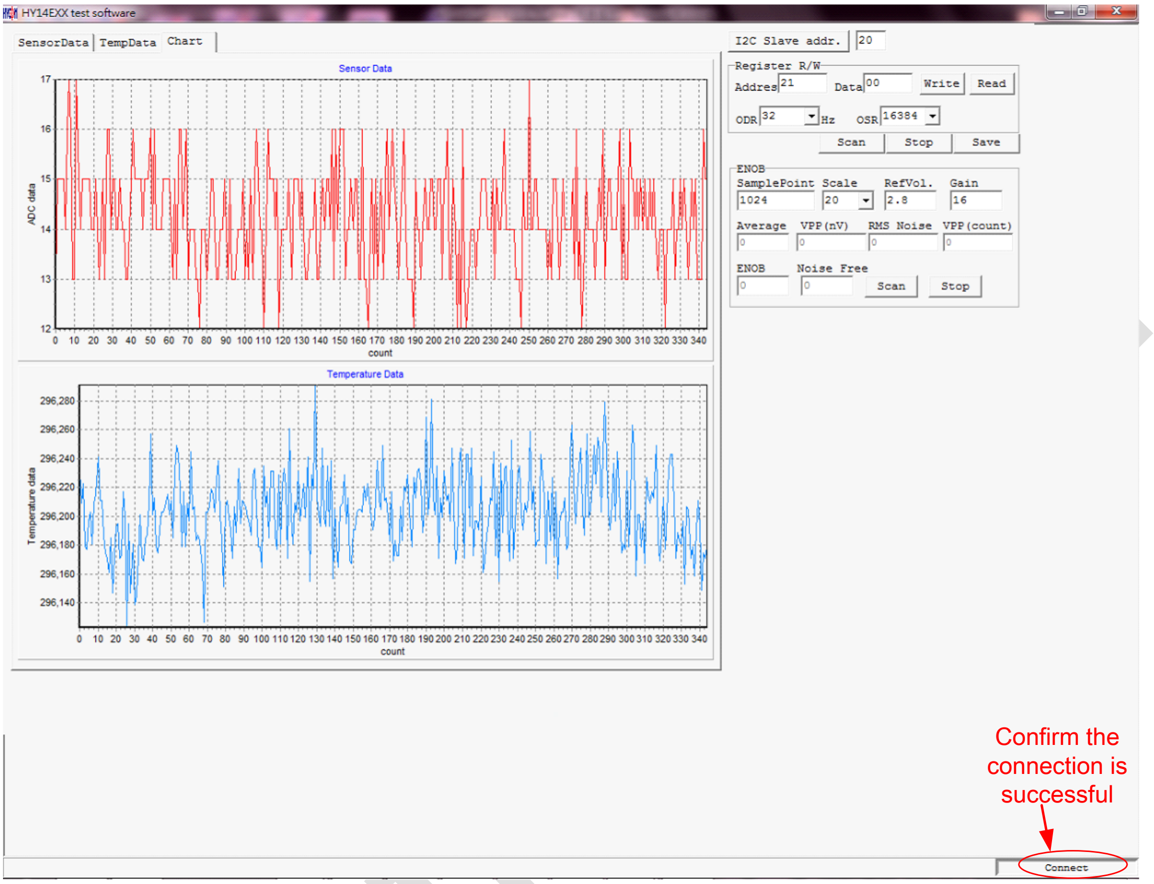

Figure2

- I2C Slave addr: the value inputted from the IDE software is converted by the binary system to obtain the value at the blue circle.

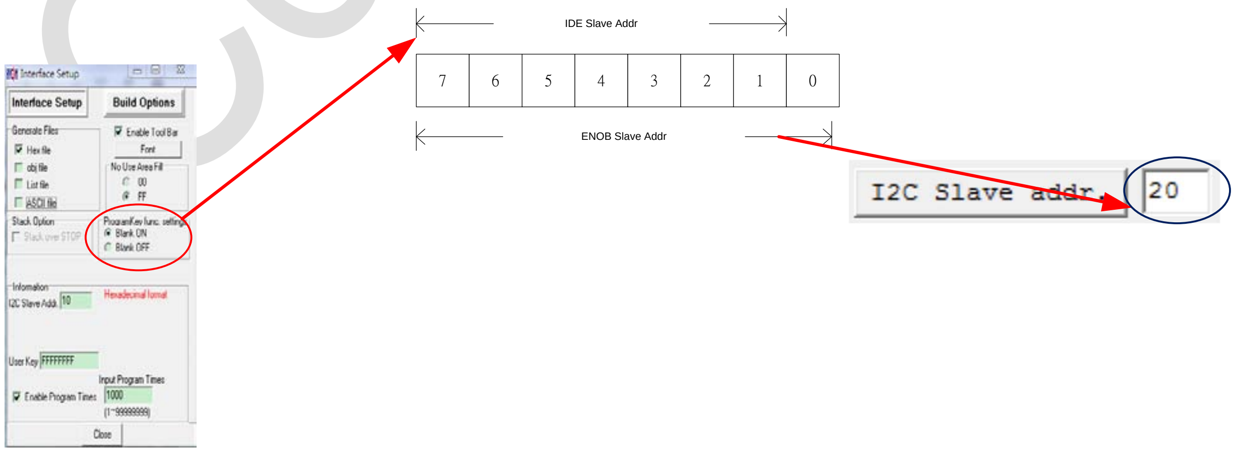

Figure3

■ The Data presentation method can be selected.

Figure4

■ Select ODR & OSR.

- There are two modification methods: 1. Use the pull-down menu to directly perform the selection; 2. Perform the modification via the Address and Data.
- After the Data are scanned, the Data can be saved as the CSV file via the "Save" button (The Data will be stored in the DataLog folder of the open catalog).

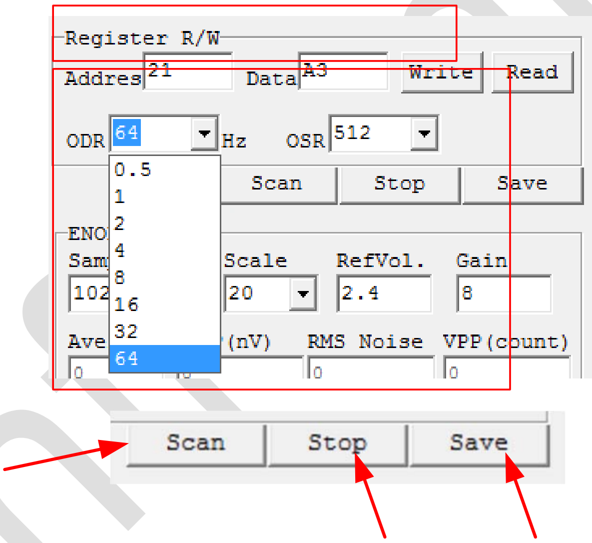

Figure5

■ Test and settings of ENOB：

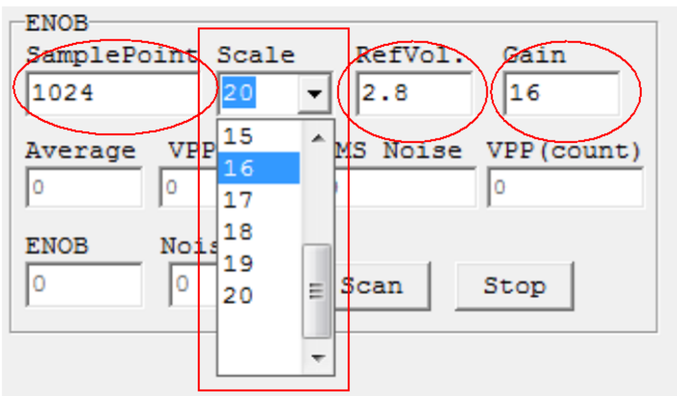

Figure6

- SamplePoint: At least 128 pieces of data; the value should be the multiple of 128. The maximal value should not exceed 10240.
- Scale: It can be selected via the pull-down menu, which is the effective numbers of the data grabbed by the ADC.
- RefVol: It can determine what the input is according to the setting of the Address 0x21.

Address=0x21, Sensor driving control address.

IIC COMMAND	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x21	DCSET2	DCSET1	DCSET0	TCR1	TCR0	SDRV1	SDRV0	REF
Access	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	1	0	0

- 0x21[SDRV1, SDRV0], Sensor Driver Vrefp pin voltage selection control
  - 00b：1.65V
  - 01b：2.20V
  - 10b：2.80V (default)
  - 11b：3.80V

- 0x21[REF], ADC reference voltage network selection control
  - 0b：ADC reference voltage channel is (Vrefp-Vrefn)/2 (default).
  - 1b：ADC reference voltage channel is (Vrefn-VSS)/1.

- Gain= determine what the input is according to the settings of the Address 0x21 and 0x22. The input value formula: $\frac{ADGN}{REF}$.

Address=0x22, ADC Gain control address.

IIC COMMAND	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x21	-	-	-	-	ADGN1	ADGN0	-	-
Access	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	1	0	0

- 0x22[ADGN1, ADGN0], ADC Gain adjustment
  - 00b：ADC Gain x 1
  - 01b：ADC Gain x 2
  - 10b：ADC Gain x 4
  - 11b：ADC Gain x 8 (default)

3. Description of ENOB and Noise Free

$$\mathrm{ENOB} = Log_2\left(\frac{\mathrm{FSR}}{\mathrm{RMS\ Noise}}\right) = \frac{In\left(\frac{\mathrm{FSR}}{\mathrm{RMS\ Noise}}\right)}{In(2)} \quad \text{Formula1}$$

$$\mathrm{Noise\ Free\ Bits} = Log_2\left(\frac{\mathrm{FSR}}{\mathrm{Peak\text{-}to\text{-}Peak\ Noise}}\right) = \frac{In\left(\frac{\mathrm{FSR}}{\mathrm{Peak\text{-}to\text{-}Peak\ Noise}}\right)}{In(2)} \frac{S}{} \quad \text{Formula2}$$

RMS Noise generated by the Sigma Delta ADC itself can determine the minimal voltage value of the sampled signal; therefore, the ENOB (the effective output bit number) is calculated according to the ratio of the RMS Noise to the Full Scale Range; however, the RMS Noise needs to be calculated by many pieces of the average values; if the sample number is not enough, which can only the RMS Noise during a period of time but cannot express the RMS Noise of the total ADC calculation; accordingly, the number of the pieces of the calculation of the RMS Noise should not be lower than 1024 pieces.

However, if the Count outputted by the ADC value does not roll, it is the Noise Free Bits; thus, the Noise Free Bits is the stable output performance of the ADC; the defined Bits calculation is the ratio of the Peak-to-Peak Noise to the Full Scale Range.

The calculation method of the RMS Noise：

Average Counts ➔ $\mathrm{Average} = \frac{\sum_{k=1}^{n} \mathrm{ADC}[k]}{n}$ Formula3

*n = The total sample number of the ADC.

$$\mathrm{RMS\ Noise} = \frac{V_{REF} \times \sqrt{\frac{\sum_{k=1}^{n} (\mathrm{ADC}[k] - \mathrm{Average})^2}{n}}}{2^{\mathrm{Scale}}} \quad \text{Formula4}$$

* Scale = The total bits of the output of the ADC.

The calculation method of the Peak-to-Peak Noise：

$$\mathrm{Peak\text{-}to\text{-}Peak\ Noise} = \frac{V_{REF} \times (\mathrm{ADC}_{Max} - \mathrm{ADC}_{Min})}{2^{\mathrm{Scale}}} \quad \text{Formula5}$$

*ADCMax = the maximum of the ADC in the total samples.

*ADCMin = the minimum of the ADC in the total samples.

4. Hardware Description

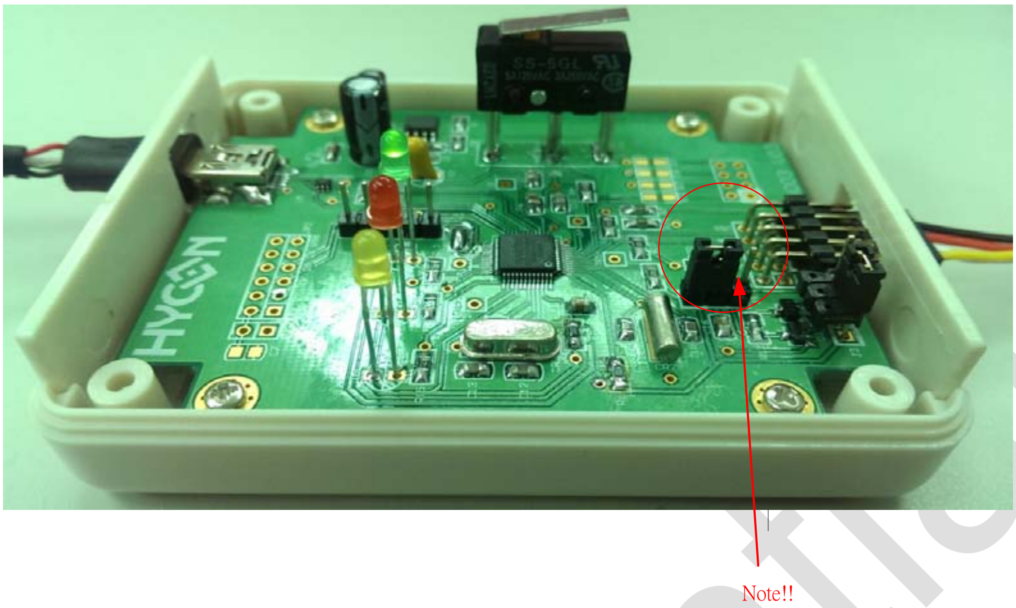

Figure7

Note！！

When you execute the ENOB connection of the communication box, please adjust the jump toward left side according to the red circle shown in Figure7.

When you execute the simulation development by the IDE and the chip via the communication, please adjust the jump toward the right side.

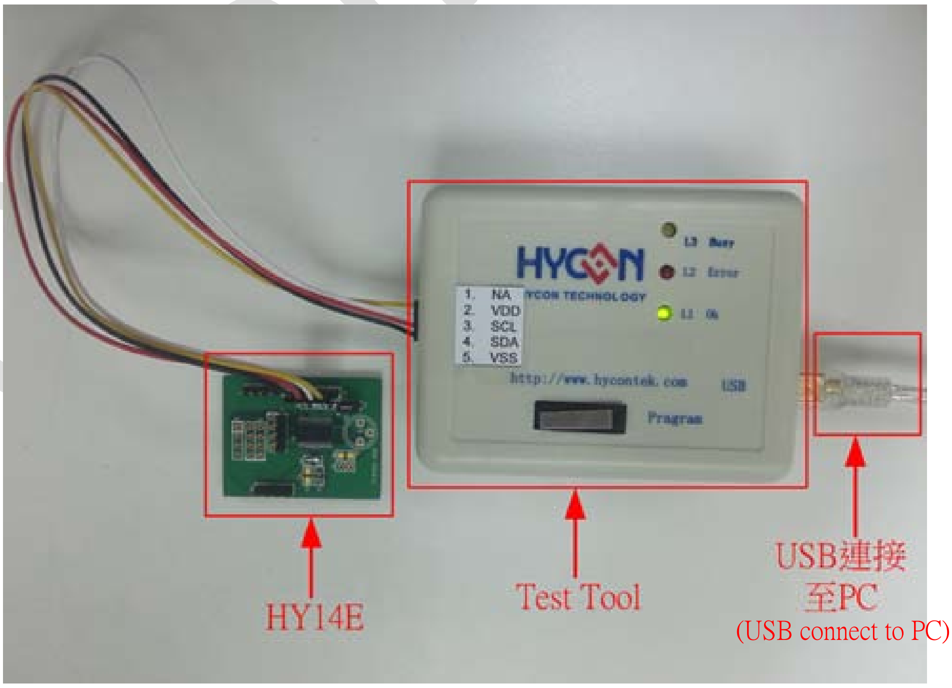

Figure8

4.1. Transmission Structure

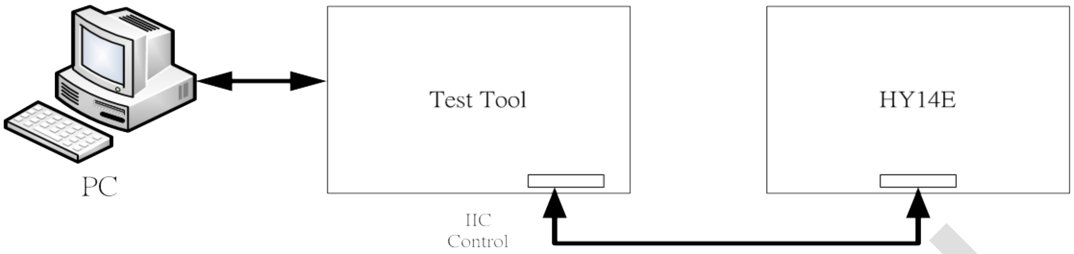

Figure9

The overall structure is to transmit the Command or Data from the PC to the USB ENOB Test Board; then, the SRAM Data of the Hycon OTP is read and written in from the USB ENOB Test Board or read and write data in the Flash Memory.

5. Modification Record

The following content describes the significant change of the document; the changes of the punctuation and the character forms are not in the description range.

Version	Page	Summary of Changes
V01	All	The initial version was issued.