HYCON TECHNOLOGY

PCB Layout Suggestions of HY11P Series

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1. Introduction

Products of HYCON ∑ △ ADC+MCU series equip with high resolution and precision ability. The ability to process 100nVrms signal is extremely sensitive to tiny power leakage and signal interference. Thus this article aims to describe basic PCB layout concept that related to the ICs to improve users' proficiency of product development.

Pin Definition

2. PCB Layout Suggestions

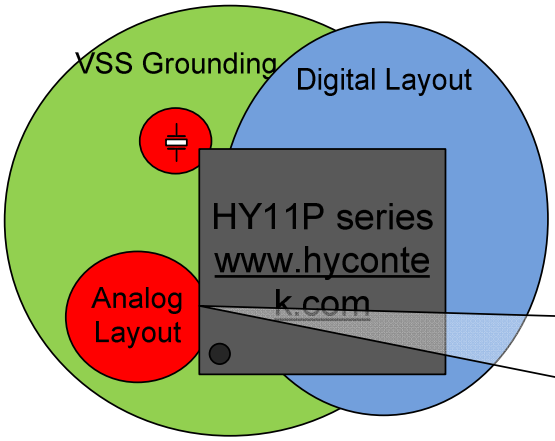

Figure 1

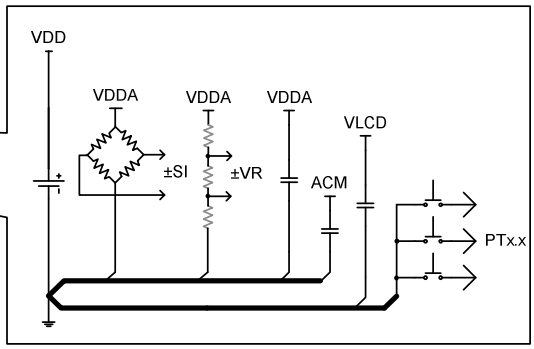

Figure 2

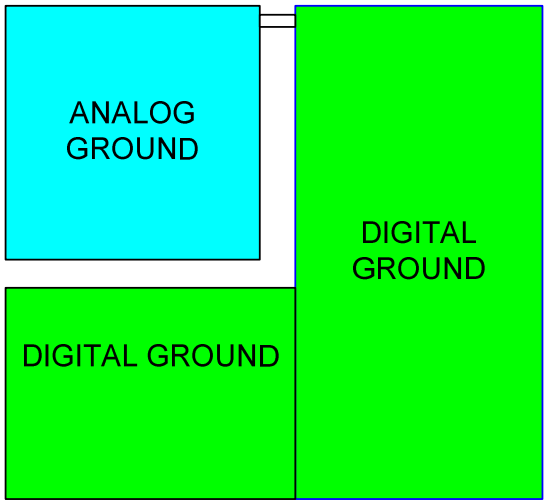

Figure 3

2.1. Power Layout

2.1.1. Analog and digital signal must use VSS grounding to isolate and layout independently, as shown in Figure 2

Bad grounding will have direct impact to button switch by having current loop into VSS to generate potential difference (PCB grounding resistor). This potential difference may lead to measurement deviation (from a couple of d to a dozen of d) of high resolution ADC products. It is suggested to keep analog and digital grounding separately as to prevent measurement error and keep close to VSS grounding that was grounded independently.

In order to reinforce anti-interference ability, VSS grounding is illustrated as Figure 3. Short analog and digital ground and it is better to place it close to the location of battery VSS.

If PCB is a double-layer board, please design vias of VSS ground to decrease ground impedance.

Besides, this measurement deviation can be removed by using software process, which is judging stability of measurement value or using delay time program. When button switch is pressed and released, ADC measurement would have several incorrect data if the power was interfered and its deviation would ranges from a couple of d to a dozen of d. If adding proper judge measurement value or delay time program, it will help to diminish measurement errors.

2.1.2. The shorter the power lead wire or ground, the higher the impedance will be. Please layout the pin regulated capacitor closes to the IC (as pin, VDD, VDDA, ACM and VLCD)

2.1.3. Connecting metal ground of COB where the IC is placed to VSS

These methods can effectively enhance system ESD ability, avoid abnormal reset situation, and reduce ADC external input noise.

2.2. Analog Layout

2.2.1. Keep the input capacitor (0.1uF) of analog input, AI0 & AI1, AI2 & AI3… as closer as the pin as possible. When external signal inputted, the trace must pass through the filer capacitor then to the IC pin

2.2.2. Input pin (AIx) trace

- ✓ Make parallel traces as short as possible, avoiding interlaced traces.
- ✓ When design traces of multilayer boards, the top and bottom board of AIx pin trace must prevent interlacing other horizontal or vertical traces.
- ✓ It is suggested to ground AIx pins if permitted.
- ✓ It is better to keep ACM external capacitor in the range of 22nF～100nF and to keep it closer to the pin.

The above description can decrease interference which means adding measurement stability of ADC to lower external input noise.

2.3. Digital Ground

2.3.1. RST & VPP use common pin, which has below considerations:

- ✓ Customer Programming
  RST/VPP pin cannot connect to VDD in order to avoid power short that caused by IC reset signal when programming. Once programming was done, RST/VPP can connect 100KΩ to VDD or short this pin after soldering the sensor.
- ✓ HYCON Programming Service
  This pin can be directly designed to connect to VDD to improve immunity to interference and reduce IC reset.

2.3.2. PT2.0/PT2.1 pin must connected to external oscillator 32768Hz (RTC)

- ✓ Keep the trace as short as possible. Using ground to isolate other AC signal generated by I/O and to prevent influence to RTC generated frequency from signal interference
- ✓ Keep distance between AIx pin and PT2.0/PT2.1
- ✓ Avoiding power pin layout passes through PT2.0/PT2.1 pin
- ✓ Isolating PT2.0/PT2.1 pin by grounding

The above description is given to enhance RTC anti-interference ability, preventing CLOCK from being influenced by noise.

2.4. Description of ESD Protection

2.4.1. PT1.3 Application Notice

- ✓ PT1.3 uses TST mode of the IC. Thus, its immunity of ESD is weaker than other I/O.
- ✓ It is suggested not to use PT1.3 as external input button or to expose it. If it was used as external button, please add low pass circuit to improve system anti-ESD ability.
- ✓ When this I/O was influenced by ESD, the IC would have reset or crash situation.

2.4.2. PT1.0 Application Notice

- ✓ PT1.0 is close to VPP/RST pin, so its immunity of ESD is weaker than other I/O.
- ✓ If it was used as external button, it is recommended referring to Figure 3 to layout its circuit when the button was gilded or made by metal.
- ✓ If this I/O was influenced by ESD, the IC would have reset, signal interrupt or crash situation.

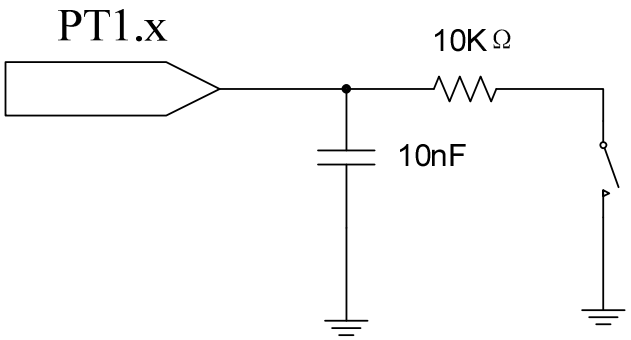

Figure 4

2.4.3. Notice of Battery Case

- ✓ Battery plays an important role in ESD test which is the best discharge route.
- ✓ Please make the shorter the power line or the lower the line impedance that connected to battery case when grounding PCB as to achieve optimum discharge route in ESD test.
- ✓ If the layout of battery pack was poor, the chance of IC to have reset or crash situation would be increased.

2.5. HY11P32 Analog Input Port

- ✓ ESD protection ability of AI0~AI1 pin of HY11P32 is not as competitive as the rest of HY11P series products, it is recommended to design load cell circuit as Figure 5 circuit.

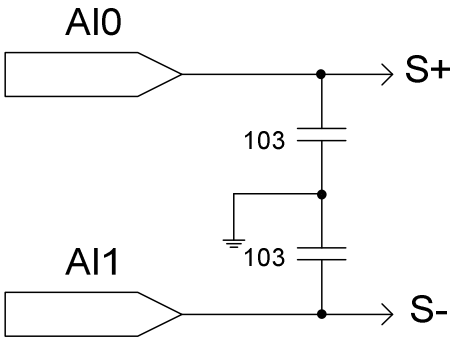

Figure 5