HY-ADC ENOB Test User's Manual

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1. ENOB and Noise Free Description

$$\text{ENOB} = Log_2\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) = \frac{In\left(\frac{\text{FSR}}{\text{RMS Noise}}\right)}{In(2)} \qquad \textit{Equation 1}$$

$$\text{Noise Free Bits} = Log_2\left(\frac{\text{FSR}}{\text{Peak - to - Peak Noise}}\right) = \frac{In\left(\frac{\text{FSR}}{\text{Peak - to - Peak Noise}}\right)}{In(2)} \qquad \textit{Equation 2}$$

RMS Noise that generated from Sigma Delta ADC is the minimum voltage value of distinguishable sampling signal. Hence, ENOB (Effective Number of Bits) is calculated by RMS Noise and Full Scale Range ratio. However, RMS Noise must be calculated by many average times. Insufficient sampling times can only represent RMS Noise for a specific period of time instead of the RMS Noise of the entire ADC operation. Therefore, RMS Noise operation times cannot be less than 1024 times.

However, Noise Free Bit represents that ADC output value count is not rolling. Noise Free Bits are stable ADC output performance. Bit operation is defined as Peak-to-Peak Noise and Full Scale Range ratio.

RMS Noise Calculation:

$$\text{Average Counts} \rightarrow \text{Average} = \frac{\sum_{k=1}^{n} \text{ADC}[k]}{n} \qquad \textit{Equation 3}$$

n = Total ADC sampling times.

$$\text{RMS Noise} = \frac{V_{REF} \times \sqrt{\frac{\sum_{k=1}^{n} (\text{ADC}[k] - \text{Average})^2}{n}}}{2^{\text{Scale}}} \qquad \textit{Equation 4}$$

Scale = Total ADC Output Bits

Peak-to-Peak Noise Calculation:

$$\text{Peak - to - Peak Noise} = \frac{V_{REF} \times (\text{ADC}_{Max} - \text{ADC}_{Min})}{2^{\text{Scale}}} \qquad \textit{Equation 5}$$

ADCMax = Maximum ADC value of total sample

ADCMin = Minimum ADC value of total sample

2. Software Description

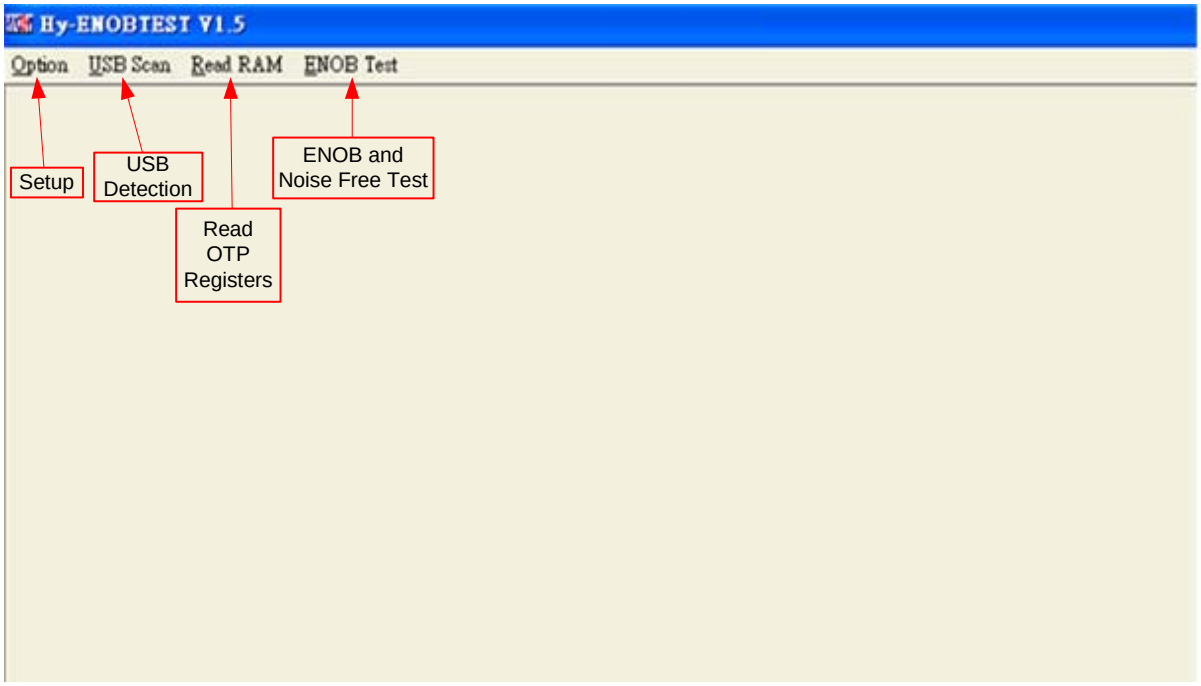


Figure 1

2.1 Option

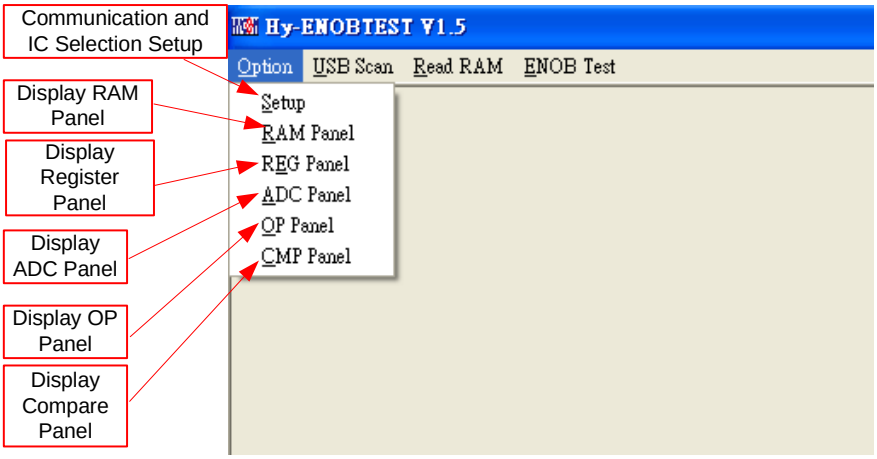


Figure 2

2.1.1 Setup

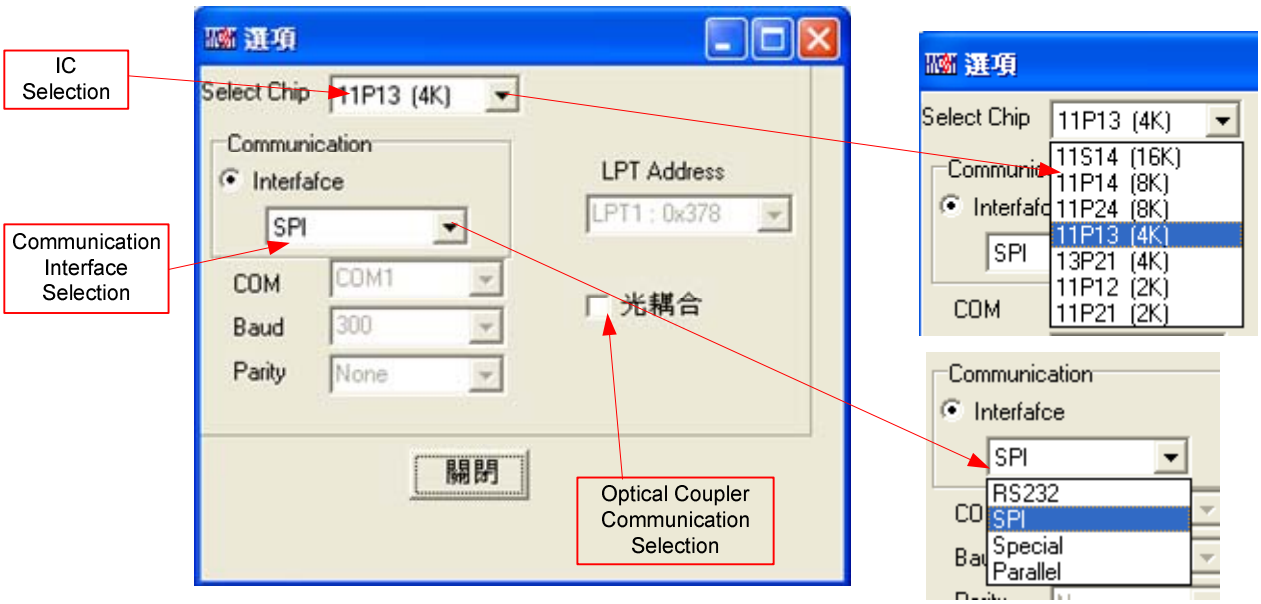


Figure 3

1. IC Selection

   Choose OTP IC, OTP IC program needs to add-in SPI or Special communication program.

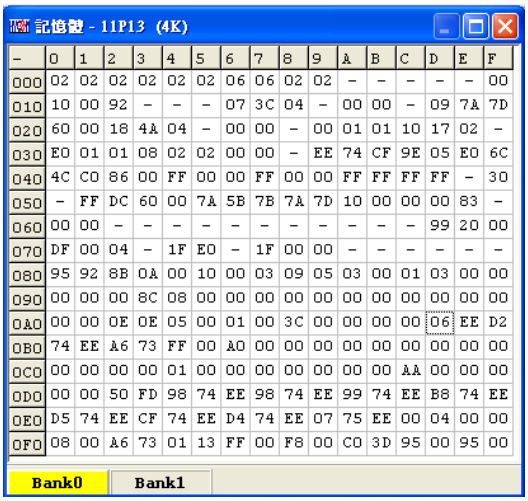
2. Communication Interface Selection

   Only SPI or Special is selectable. The function is not supportive for other interface.

3. Optical coupler Selection

   The option used when choosing optical coupler as isolator of communication interface.

2.1.2 RAM Panel



-	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	02	02	02	02	02	02	06	06	02	02	-	-	-	-	-	00
010	10	00	92	-	-	-	07	3C	04	-	00	00	-	09	7A	7D
020	60	00	18	4A	04	-	00	00	-	00	01	01	10	17	02	-
030	E0	01	01	08	02	02	00	00	-	EE	74	CF	9E	05	E0	6C
040	4C	C0	86	00	FF	00	00	FF	00	00	FF	FF	FF	FF	-	30
050	-	FF	DC	60	00	7A	5B	7B	7A	7D	10	00	00	00	83	-
060	00	00	-	-	-	-	-	-	-	-	-	-	-	99	20	00
070	DF	00	04	-	1F	E0	-	1F	00	00	-	-	-	-	-	-
080	95	92	8B	0A	00	10	00	03	09	05	03	00	01	03	00	00
090	00	00	00	8C	08	00	00	00	00	00	00	00	00	00	00	00
0A0	00	00	0E	0E	05	00	01	00	3C	00	00	00	00	06	EE	D2
0B0	74	EE	A6	73	FF	00	A0	00	00	00	00	00	00	00	00	00
0C0	00	00	00	00	01	00	00	00	00	00	00	00	AA	00	00	00
0D0	00	00	50	FD	98	74	EE	98	74	EE	99	74	EE	B8	74	EE
0E0	D5	74	EE	CF	74	EE	D4	74	EE	07	75	EE	00	04	00	00
0F0	08	00	A6	73	01	13	FF	00	F8	00	C0	3D	95	00	95	00

Figure 4

Please refer to Chapter 3.2 RAM Window Operation of HY-IDE Software User's Manual.

2.1.3 REG Panel

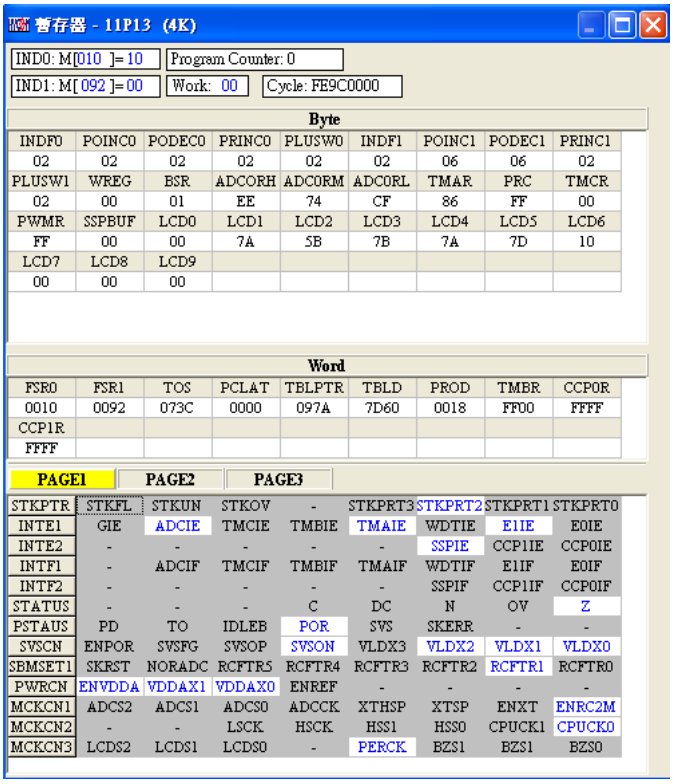


Figure 5

Please refer to Chapter 3.3 Register Window Operation of HY-IDE Software User's Manual.

2.1.4 ADC Panel

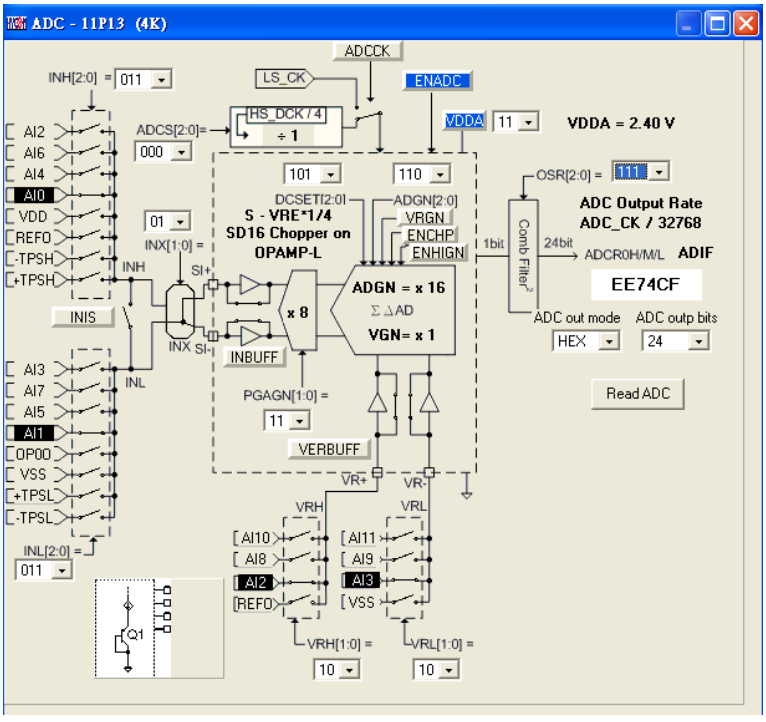


Figure 6

Please refer to Chapter 3.6 ADC Window Operation of HY-IDE Software User's Manual.

2.1.5 OP Panel

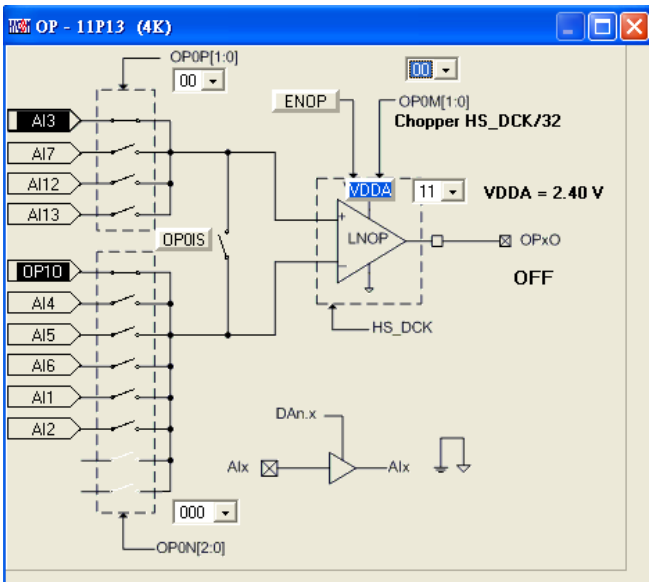


Figure 7

Please refer to Chapter 3.7 OP Window Operation of HY-IDE Software User's Manual.

2.1.6 CMP Panel

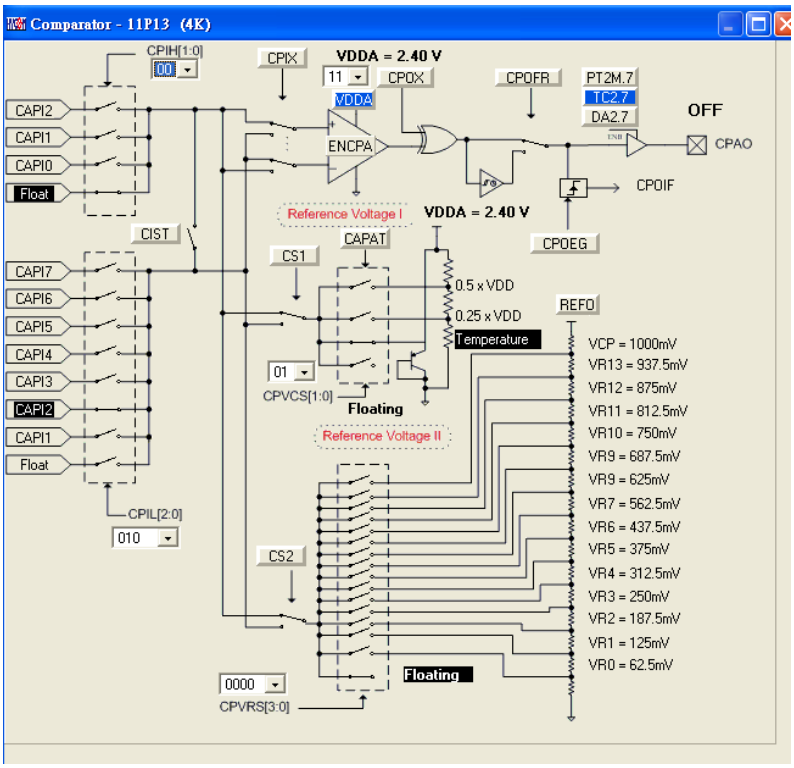


Figure 8

Please refer to Chapter 3.8 Comparator Window Operation of HY-IDE Software User's Manual.

2.2 USB Scan

USB scan function help to detect whether USB scan communication port is connected to ENOB Control Board. If it is connected, the status, USB On Line, will be shown in left corner, as Figure 9

displayed.

Figure 9

If it is not connected, the status, USB not Connect, will be shown in left corner, as Figure 10 displayed.

Figure 10

PC program will scan once in every minute.

2.3 Read RAM

After USB Scan is executed, make sure USB is On Line. Then executes Read RAM, OTP Chip RAM and Registers at this moment, will be written into PC buffer. This will influence RMS Noise and Peak-to-Peak Noise operation of ENOB Test.

2.4 ENOB Test

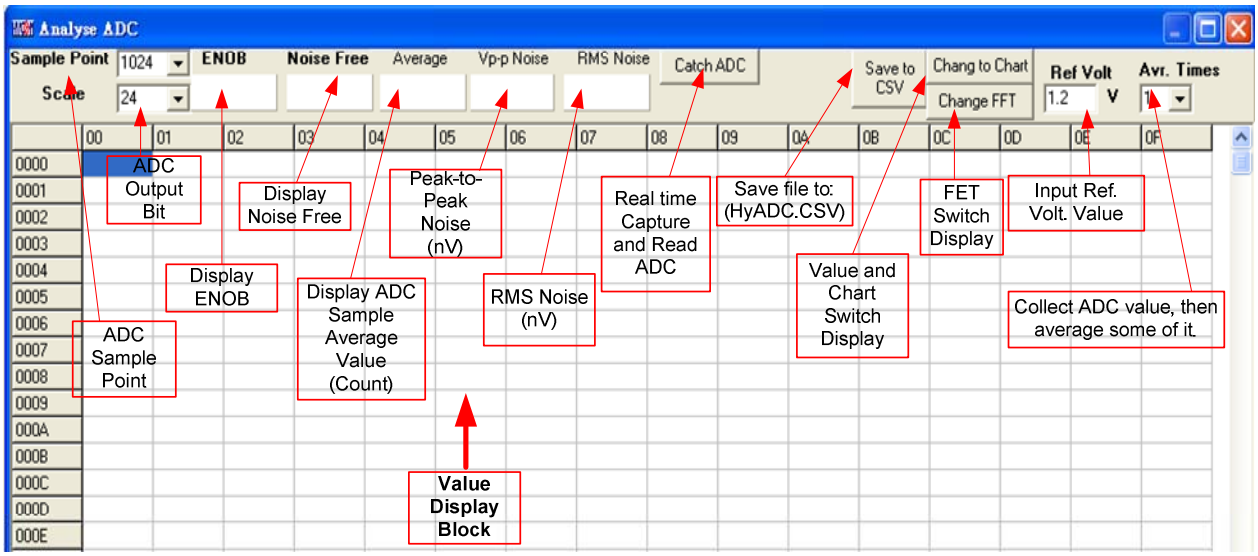


Figure 11

1. Sample Point

   "Catch ADC" and "Ca.Flash" function of ADC sample point. The minimum OTP ADC sampling output amount is 256, the maximum is 1024.

2. Scale

   ADC output bits. The minimum of ADC output is 8-bit, maximum is 24-bit.

3. ENOB

   Display ENOB (Effective Number of Bits). The Calculation is shown as Equation 1. The unit is Bit.

4. Noise Free

   Display Noise Free Bits. The Calculation is shown as Equation 2. The unit is Bit.

5. Average

Display ADC sampling average value. The Calculation is shown as Equation 3. The unit is Count.

6. Vp-p Noise

   Display Peak-to-Peak Noise. The Calculation is shown as Equation 3. The unit is nV.

7. RMS Noise

   Display RMS Noise. The Calculation is shown as Equation 4. The unit is nV.

8. Catch ADC

   Real time catch and display ADC value in sequence in value display block.

9. Save to CSV

   Save the value of display block into HyADC.CSV file, including ENOB, Noise Free, Average, Vp-p Noise and RMS Noise.

10. Change To Chart

    Change to display chart and value in value display block.

11. Change FFT

    Chart switch, displaying frequency domain and time domain.

12. Ref Volt

    Input Reference Voltage value (unit is V).

13. Avr. Times

    Select software average. Values in the value display block will be averaged based on the selected times, then to be shown in the block.

3. Hardware Description

3.1 Communication Structure

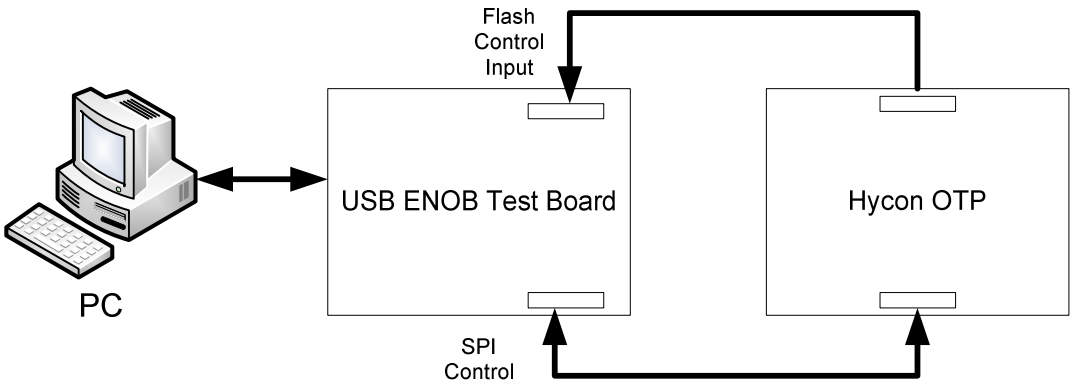


Figure 12

The whole structure starts from PC sending Command or Data to USB ENOB Test Board. The PC can read/write HYCON OTP SRAM Data or Flash Memory through USB ENOB Test Board.

3.2 USB ENOB Test Board Description

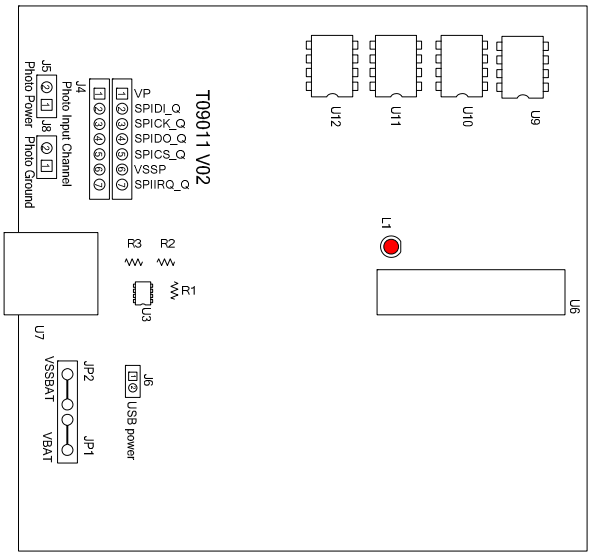


Figure 13

1. J2, J3: SPI Communication Port

   J2 Description

   PIN 1 → VDDIN supplies U1power.

   J3 open➔HYCON OTP powered by external

   J3 short➔HYCON OTP powered from ENOB test Board

   PIN 2 → ICESDI_Q, DI signal line of SPI.

   PIN 3 → ICESCK_Q, CK signal line of SPI.

   PIN 4 → ICESDO_Q, DO signal line of SPI.

   PIN 5 → ICECS_Q, CS signal line of SPI.

PIN 6 → VSS

PIN 7 → ICEIRQ_Q, signal line for detecting whether HYCON OTP writing into Flash Memory is accomplished.

2. J4, J5, J8 : Optical Coupler Communication Port

J4 Description

PIN 1 → VP supplies power to optical coupler IC (U9~U13).

J5 & J8 open➔ thoroughly separate the power of optical coupler IC and HYCON OTP.

J5 & J8 short➔ optical coupler IC and HYCON OTP uses the same power

PIN 2 → SPIDI_Q, DI signal line of optical coupler.

PIN 3 → SPICK_Q, CK signal line of optical coupler.

PIN 4 → SPIDO_Q, DO signal line of optical coupler.

PIN 5 → SPICS_Q, CS signal line of optical coupler.

PIN 6 → VSSP, optical coupler ground.

PIN 7 → SPIIRQ_Q, signal line (optical coupler) for detecting whether HYCON OTP writing into Flash Memory is accomplished.

3. J9, J10, J11 and U8

U8 is Flash Memory that capacitates 512K byte memory.

J10 and J11 is Flash Memory power source.

J10 & J11 pin1-2 short➔ powered by External (J5-pin1 and J8-pin2)

J10 & J11 pin2-3 short➔ power is regulated from U3 (J5-pin2 and J8-pin1)

J9 Description:

PIN 1 → VDD_X, supplying U8 power.

PIN 2 → FLDI, controlling DI signal line of U8.

PIN 3 → FLCK, controlling CK signal line of U8.

PIN 4 → FLDO, controlling DO signal line of U8.

PIN 5 → FLCS, controlling CS signal line of U8.

PIN 6 → VSS_X, U8 ground.

4. JP1, JP2, J6 and U3

JP1 and JP2 supplies external power to U3 in order to generate VDD power

J6 open➔using external power (5V) that inputted from JP1 and JP2.

J6 short➔ using USB power.

The regulator composed by U3, R1, R2 and R3 generates VDD power. The output voltage can be amended through R1, R2 and R3. The equation is described in below:

$$\mathrm{VDD} = 1.240V \times (1 + \frac{R1 + R2}{R3}))$$

4. Revision History

Major differences are stated thereinafter:

Version	Page	Revision Summary
V01	ALL	First edition
V02	9	Delete 2.5 Switch test information.
	ALL	Update all the figures