Instant On Measuring Theory

For HY11P13 Bridge Sensor Application

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1. Brief Introduction

The products of HYCON's HY11P series have high speed measuring and low power consumption features. This article describes how the chip completes the judgment of many kinds of combined measuring values and the calculation of the relative current consumption in the shortest time. We expect to achieve the feature of saving the external switches while enduring over a long period of time.

2. Theory Description

In the fixed physical quantity measuring system, the chip with ADC function must delay a period of time after receiving the awaking signal (the breaking signal / the trigger signal) from sleep or Idle Mode, to complete the internal oscillator start and to proceed the system initial setup, and then output the ADC measuring conversion. Only when the start is finished, all functional modules can work normally.

In the system's start process, some designs require external components to trigger, some achieve the trigger by asymmetric theory in circuit, while we use the compound trigger, that is, to use the timer to awake and use ADC to proceed the fast measuring, and then complete the trigger signal through the computing conditions. For above three methods, there are advantages and drawbacks respectively that are compared simply as Table 1.

	Mechanical Switch	Trigger Circuit	Consuming Current	Consuming Current Per Second（Rs=1KΩ）
Trigger by External Components	Yes	Simple; Trigger by I/O	Very small	Nearly no
Asymmetrical Trigger in Circuit	No	Complex; Cost increasing in the circuit design	Big	Uncertain
Compound Trigger	No	No; The original measuring network	Small	About 12.5uA

Table 1 Simple Comparison for Advantages and Lacks of the System Initiation Methods

3. Testing Items

If the chip is in Idle Mode, it needs some delay time from producing the breaking signal to awake the system to the internal oscillator (HAO) finishing start. Also, after the internal oscillator (HAO) start being finished, it needs some delay time from the system's initial setup to VDDA finishing start. This article provides the results of the following testing items for reference:

a. The analysis of the delay time for the chip from awaking to S18 output first record converting value, and the evaluation and tests for all stages of current.
b. To proceed the periodical (1Hz) measuring for SD18 OSR under the condition of setup individually the output rate to 1KHz with the watchdog WDT, and measure individually the sensor's zero, 1%F.S., 3%F.S., 5%F.S. and 10% F.S to check out the response time of the former six records converting output and the stability of the four times measuring values by using WDT breaking to awake.
c. The demonstrating procedure of the periodical measuring for the chip:
   - ✓ The measuring system progresses the measurement by awaking one time about each second and detects the zero change.
   - ✓ To awake completely to measure when the zero change of the sensor surpasses 1%F.S.
   - ✓ To display the measuring value directly or after processed by adding the digital filter (processing the average of eight records).
   - ✓ The measuring parameters (change quantity, cycle, SD18 resolution and records to display) are changeable.

PS. Note the following when the chip starts ADC measuring:

Note the stable time when start VDDA. It needs to delay 500uS to start the related analog circuit module when connect externally 1μF, and delay 5mS when connect externally 10μF.

SD18 module switches when starting or measuring the network after starting network. The first two records of its analog/digit converting output are the reference values, and the following values after the two records are valid values.

4. Testing Conclusion

4.1. The Evaluation of Power Consumption

The delay time for the chip from awaking to SD18 output the first record converting value is approximately 3.52ms. It includes the chip start delay and VDDA start delay. The evaluation of its HY11P12 power consumption is calculated as follow:

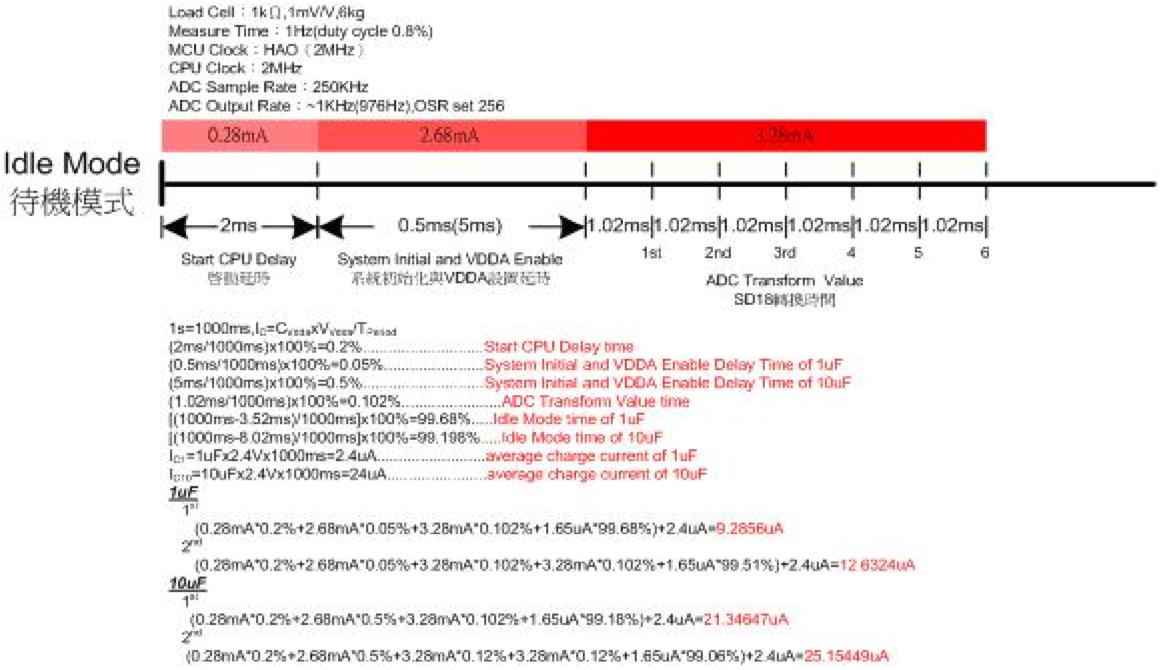

Figure 1 HY11P12 Power Consumption Evaluation

Therefore, if use 1uF capacitor and take the second output as ADC zero detection, the consuming current is 12.6324uA/S. For the chip supplied by a 240mA/H lithium battery, if it works only at Idle Mode and makes the zero detection by 1KHZ frequency, the available time of a battery is estimated to be 791.6 days.

If measuring 10 times one day and 15S for each time, due to the chip consumes 3.28mA current in measuring, its average of the consuming current is approximately: {(3280×15S×10) ÷86400} +12.6324=18.3268 uA/S. For a 240mA/H lithium battery, its estimating available time is: 545 days

4.2. Stability Evaluation

The response time from awaking to SD18 proceeding six outputs is approximately 9.7ms. To analyze the ADC values for each weight, ADC is stable after output two records, and each starting is good for its consistency after the second record. The biggest change COUNT of the starting zero each time is 10 that is approximately 0.2% full scale for the sensor. The second data is shown as Table 2. For third to seventh ADC data, please see Table 3.

Measuring Weight	ADC Output Record	Measuring Times			
		1	2	3	4
Zero	2	15926	15927	15926	15925
1%	2	15879	15878	15879	15874
3%	2	15782	15787	15783	15787
5%	2	15692	15682	15686	15685
10%	2	15443	15445	15442	15442

Table 2 The Second Data of SD18 Fast Start

4.3. Demonstration Procedure Description

Enter IDLE after the demonstration procedure starting and awaken by the WATCH DOG:

- ✓ Initialize system, setup CPUCK to 2M, setup VDDA, take the instruction circulation with delay time approximately 500uS (the VDDA capacitor is 1μF), and setup ADC output frequency to be 1KHZ;
- ✓ Detect sensor's change, when the change surpasses sensor's 1% full scale change, enter directly into the measuring mode, otherwise enter IDLE MODE again;
- ✓ Under the measuring mode, you may select to make 8 records average or not through PT1.7 that connects to the ground or not.
- ✓ Under the measuring mode, you may select ADC BIT to display on LCD through PT1.0 breaking (ADC displays after the process of adding 3FFFFF. If press PT1.0, LCD will display a number. For example, LCD displays 6, then the ADC display number is 24-6 on LCD, that is, ADC valid digit is ±16BIT).
- ✓ IDLE Mode is awakened by Watch dog in 1 second.
  - ■ Enters IDLE MODE. CPU Clock is setup to internal 28Khz and closes internal 2Mhz OSC
  - ■ ICE simulates the testing result. IDLE Mode current ~ 4.67uA. For the actual chip, it is approximately 1.7uA/3uA;
  - ■ Existing chip IDLE Mode current ~ 3uA (HY11P12), 1.65uA （HY11P13/HY11P14）

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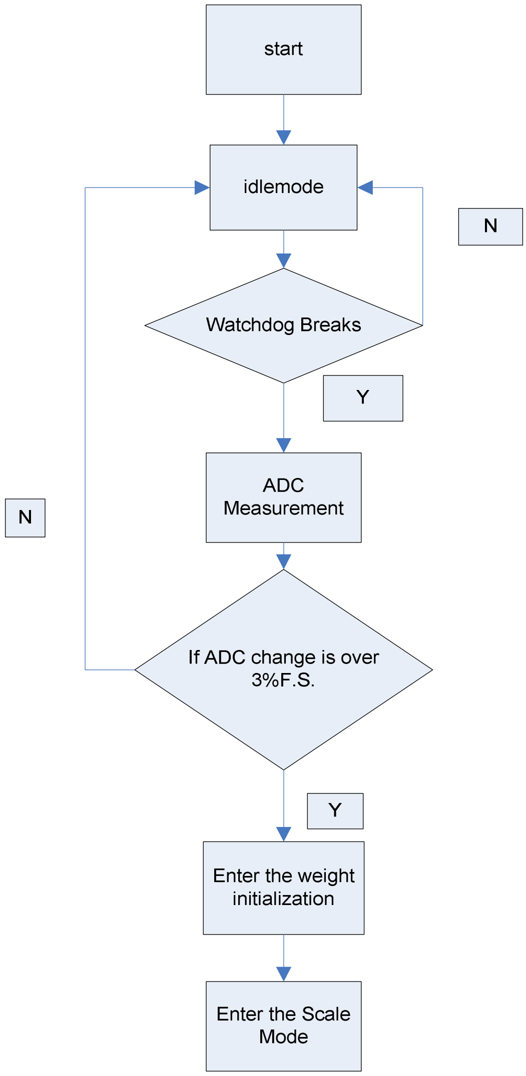
Procedure Flow:



5. Technical Specification

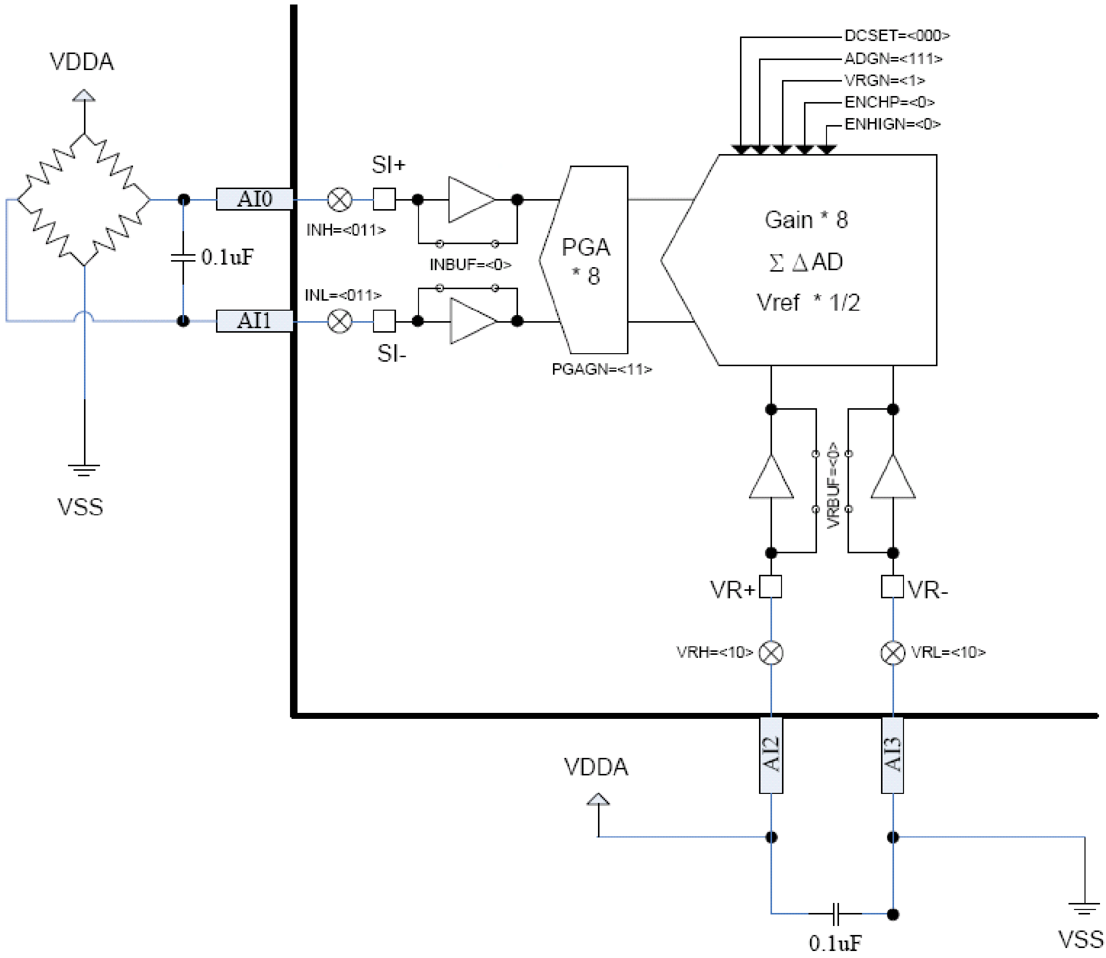
5.1. Chip Parameters and Setup Description

VDD: 3.0V
VDDA Output Voltage (1uF): 2.4V
System Clock: 2MHz(HAO)
CPUCK: 2MHz
ADC Sampling Frequency: 250KHz
ADC Output Frequency is about: 1kHz

5.2. The Measuring Instruments and The Sample

Measuring Instruments: Agilent DSO5034A, BRYMEN BM859CF
Testing Sample: HY11S14 (LOT#:MQ1JJ.01)
Sensor: 6Kg, 1mV/V, 1KΩ

5.3. Test Theory Schematic



6. Testing Records and Methods Description

6.1. Power Consumption Analysis

Take HY11P12 as the example, the ADC output speed is 1KHz, the sensor power is 2.4V, the capacitance of the sensor power is 1uF, the internal resistance of the sensor is 1KΩ and the current of MCU+ADC is 750uA. Under the Idle mode, MCU current is approximately 3uA (approximately 1000mS). Take 2 records of ADC values (approximately 2.04mS) by each second to calculate the average current:

- ✓ The average current each second of the sensor power switch is approximately I×t = C×V → 2.4uA/S
- ✓ Under the Idle mode, the current each second of MCU is approximately 1.65uA/S
- ✓ The current of the chip start delay is approximately 0.56uA/S
- ✓ The current of the chip to complete the system initialization and the VDDA setup delay is approximately 1.35 uA/S
- ✓ The current of the measuring time for the chip to take two records of ADC is approximately 6.732 uA/S
- ✓ Therefore the average current each second is approximately 0.6 +1.35＋6.732＋2.4＋1.65 ≒12.6312uA/S

Because it is unable to forecast the measuring time and the number of times that we can only list the average current needed by the detection each second.

6.2. Data Analysis

Table 3 and Feature 2, 3, 4, 5 and 6 are the output material by continuous sampling.

Table 3 Continuous Sampling Seven Data by Fast Start SD18

Measuring Weight	ADC Output Record	Measuring Times			
		1	2	3	4
Zero	1	16305	16344	16403	16303
	2	15926	15927	15926	15925
	3	15934	15930	15931	15932
	4	15929	15930	15928	15931
	5	15927	15928	15925	15926
	6	15935	15930	15930	15933
	7	15941	15941	15941	15939
1%	1	16146	16280	16201	16279
	2	15879	15878	15879	15874
	3	15885	15882	15882	15882
	4	15880	15879	15877	15879
	5	15878	15882	15881	15878

	6	15885	15881	15881	15881
	7	15893	15890	15893	15891
3%	1	16231	16234	16233	16232
	2	15782	15787	15783	15787
	3	15785	15788	15788	15784
	4	15783	15783	15783	15783
	5	15787	15779	15779	15789
	6	15792	15782	15782	15785
	7	15790	15788	15788	15793
5%	1	16184	16141	16184	16181
	2	15692	15682	15686	15685
	3	15697	15691	15693	15693
	4	15694	15688	15690	15691
	5	15690	15691	15686	15687
	6	15688	15695	15691	15687
	7	15698	15702	15698	15696
10%	1	16022	16102	16065	16052
	2	15443	15445	15442	15442
	3	15446	15448	15449	15449
	4	15448	15450	15450	15450
	5	15448	15449	15445	15445
	6	15450	15452	15451	15447
	7	15455	15461	15461	15458

Table 3 Continuous Sampling Seven Data by Fast Start SD18

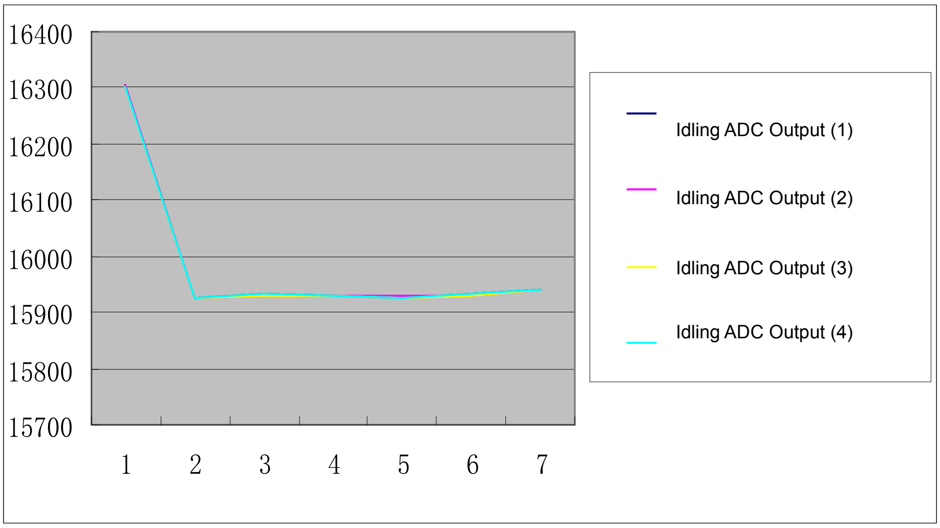


Figure 2 ADC Output in Frequency 1HZ and LOAD CELL Idling

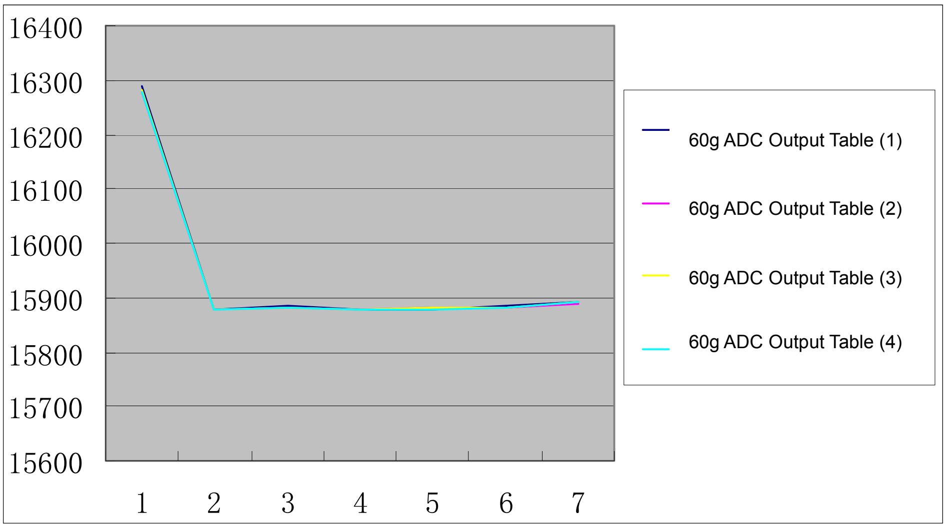


Figure 3 ADC Output in Frequency 1HZ and LOADCELL Laying 60g

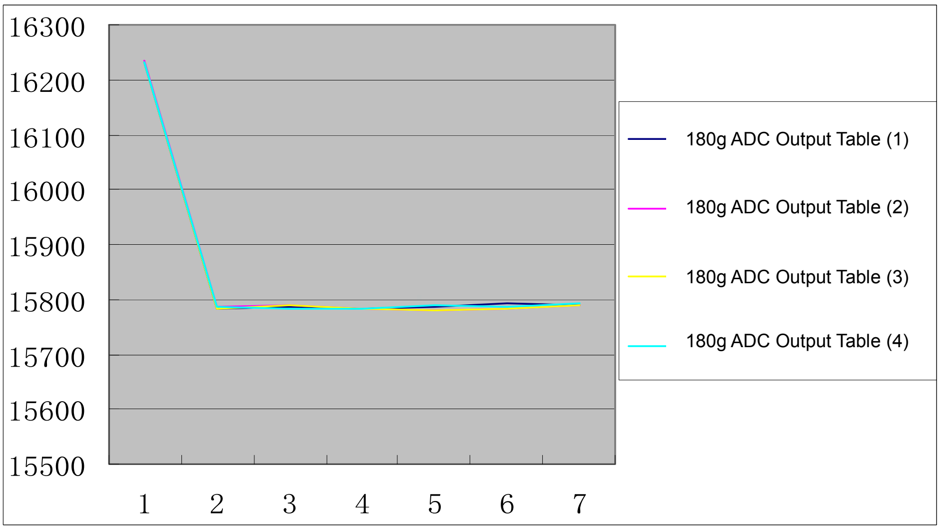


Figure 4 ADC Output in Frequency 1KHZ and LOADCELL Idling 180g

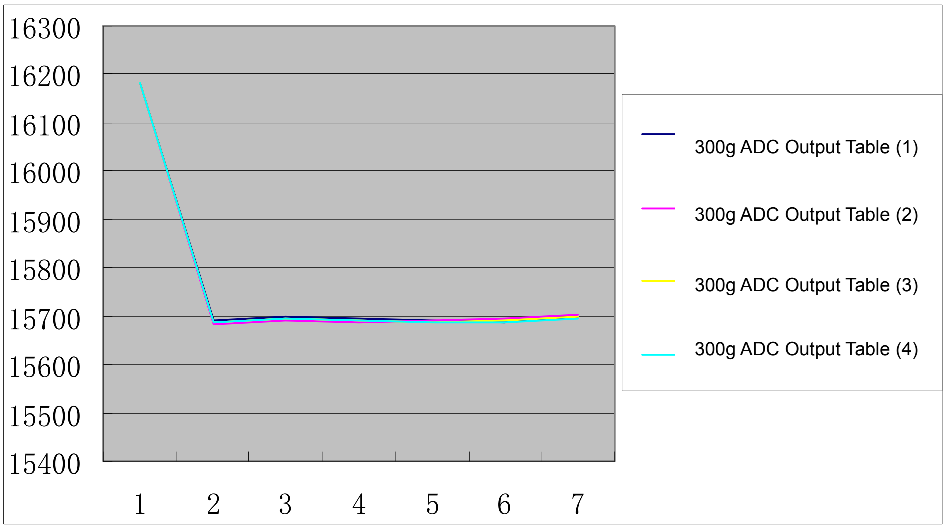


Figure 5 ADC Output in Frequency 1KHZ and LOADCELL Laying 300g

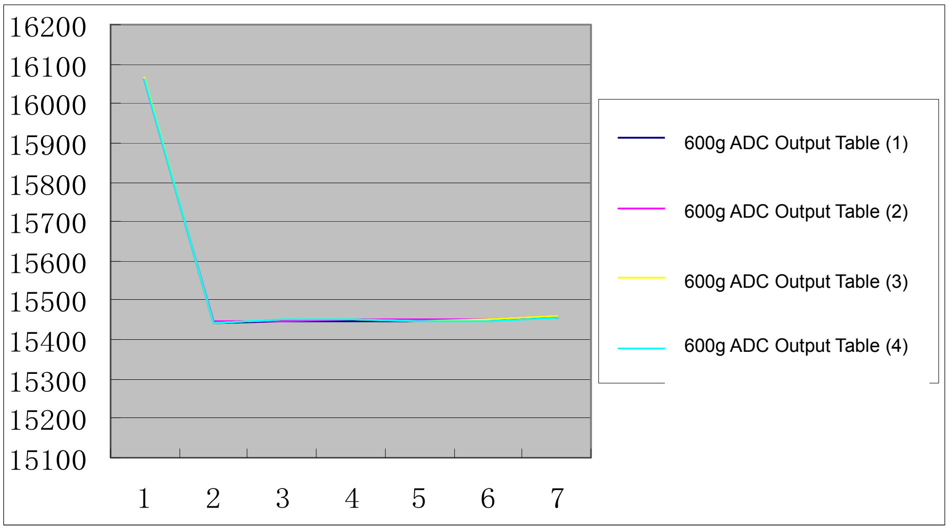


Figure 6 ADC Output in Frequency 1KHZ and LOADCELL Laying 600g

6.3. Chip Start Wave

Figure 7, 8, 9 and 10 are the start wave in output frequency 1KHZ.

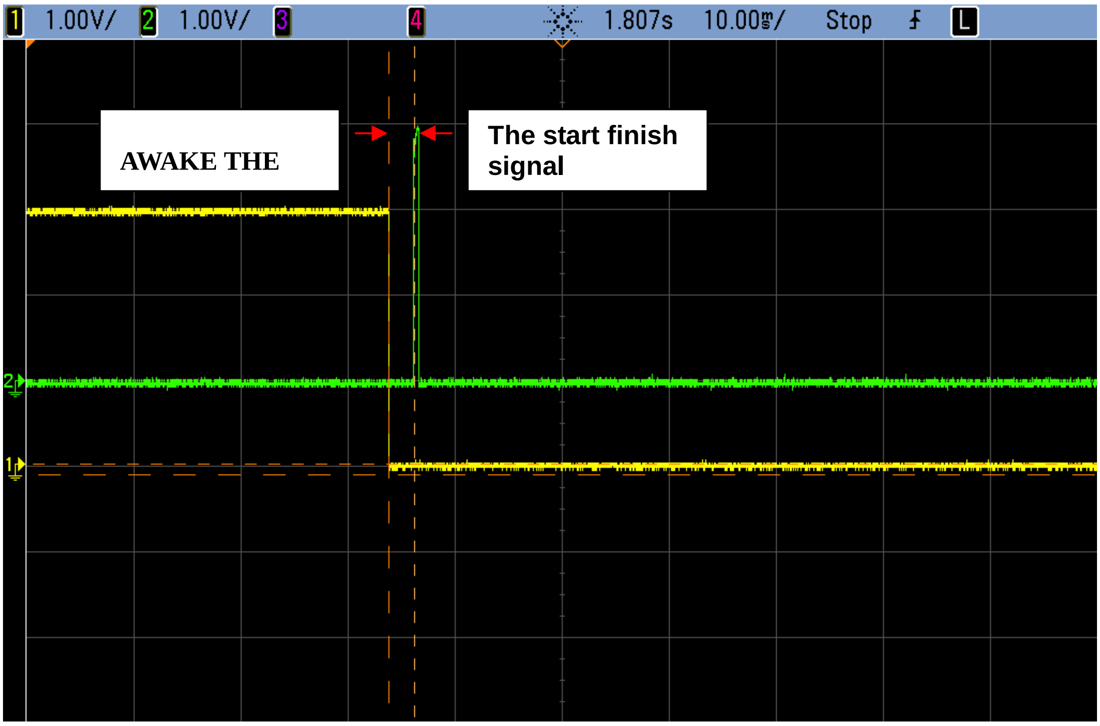


Figure 7 The Breaking Wave from IDLE MODE Awaken to Start CPU, △T=2mS

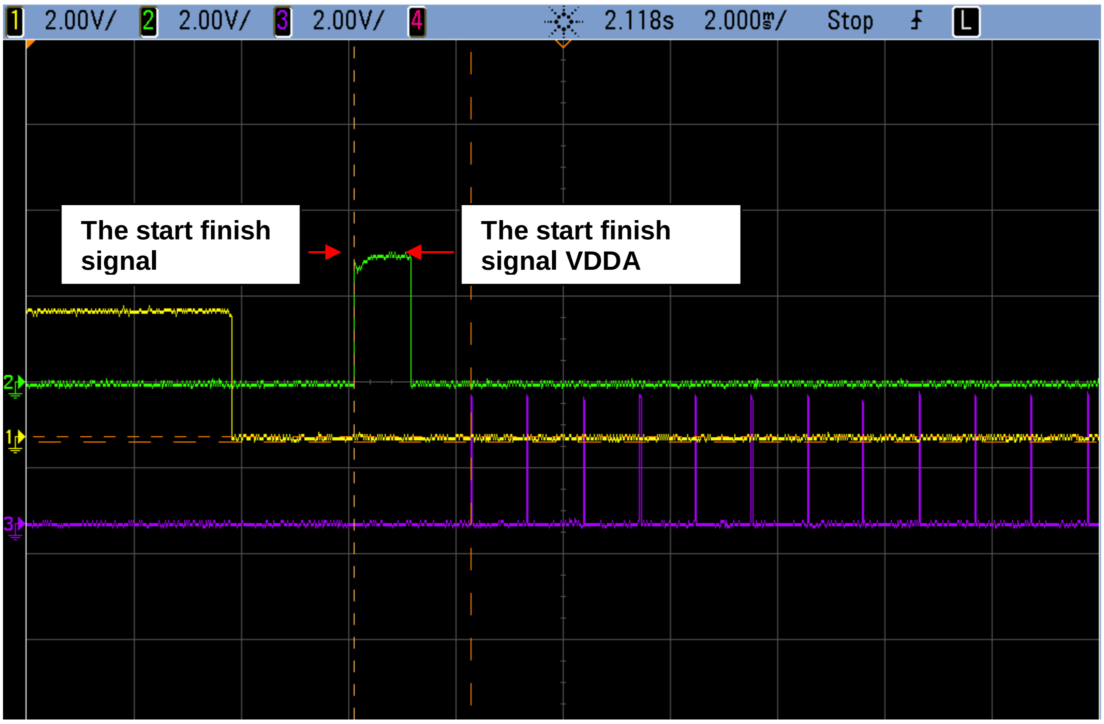


Figure 8 VDDA Start Delay Is About 0.5mS

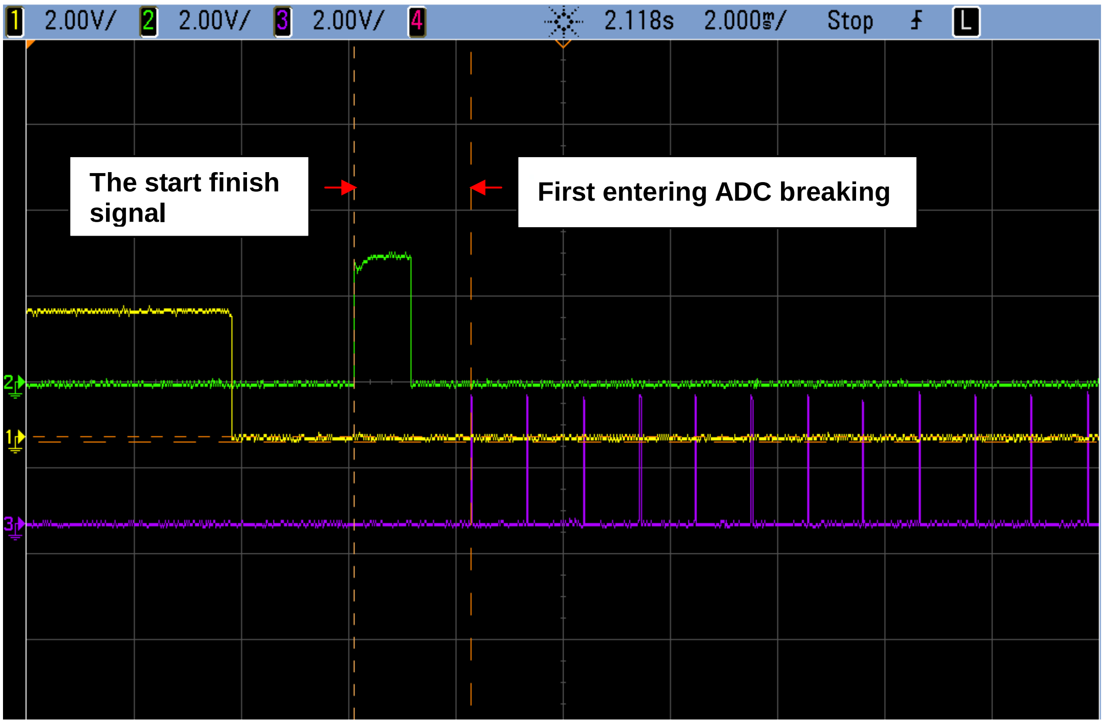


Figure 9 The time of the first time entering the ADC breaking after CPU starting, △T=1.52mS

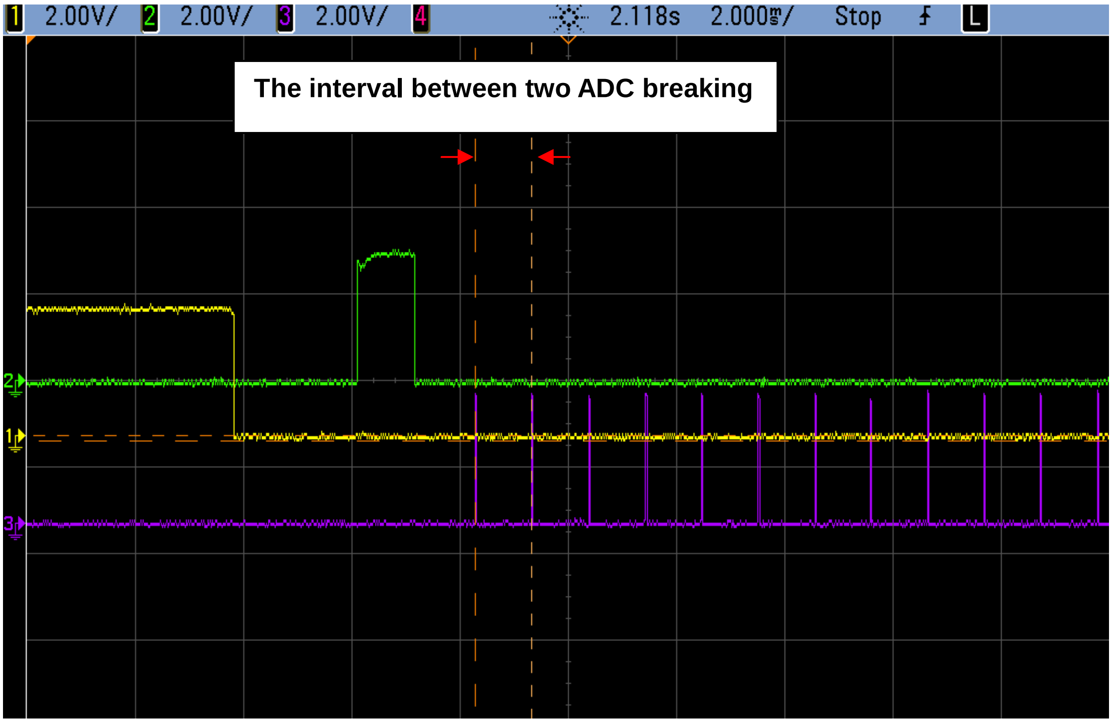


Figure 10 The Interval of Every ADC Value Producing, △T=1.02mS

7. Testing Program

7.1. Start Zero Change Judgment

For details of the procedure, please see the enclosed documents in the program.

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7.2. The Bug Patching Program for Zero Inconsistent in ADC Starting

For details of the procedure, please see the enclosed documents in the program.

ADC OFFSET 測試.rar

8. Revision Record

Major differences are stated thereinafter:

Date	Version	Page	Revision Summary
2009/04/30	V01	ALL	First edition