HY11P13

Application Note

3000 Counts Pricing Scale

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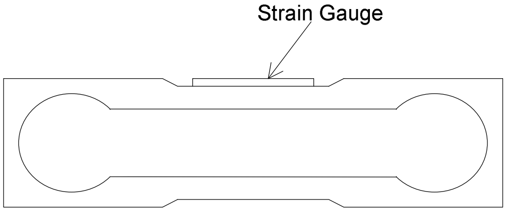
1. Brief Introduction

Not only the characteristics of peripheral components should meet the requirements but also the measurement IC must achieve the specification due to pricing scale needs to be strictly certified, including temperature, precision, resolution and anti-interference capability (ESD & EMI) was requested as well. Therefore, simplifying peripheral passive components (resistors) could reduce temperature impact on measuring. It is more cost saving and has significant improvement of anti-interference ability.

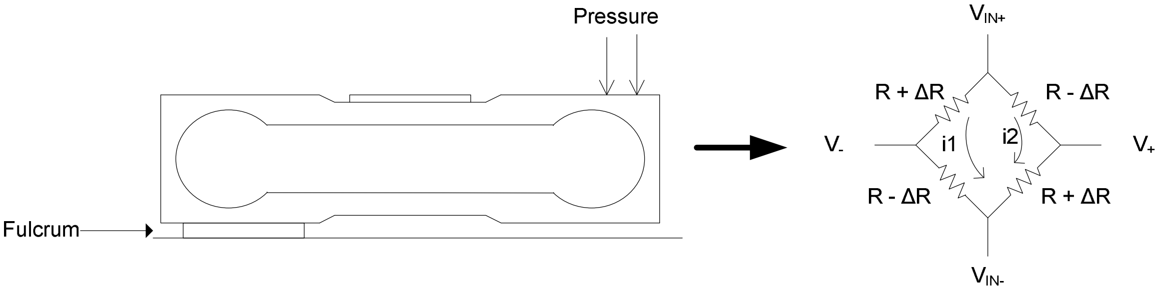
2. Theory

2.1 Sensor Components

The theory of load cell is to stick strain gauge, which is made of bridge resistors on the aluminum pan. It is the so called “strain gauge".



Strain gauge resistance generates ΔR change value when the aluminum pan was distorted from the pressure.



The ΔR change value that generated from the two signal sides is:

$$V_+ - V_- = \left(\frac{(R+\Delta R)}{(R-\Delta R)+(R+\Delta R)} \times (V_{IN+} - V_{IN-}) \right) - \left(\frac{(R-\Delta R)}{(R-\Delta R)+(R+\Delta R)} \times (V_{IN+} - V_{IN-}) \right)$$

$$V_+ - V_- = \frac{\Delta R}{R} \times (V_{IN+} - V_{IN-})$$

A/D transformed the physical signals to digital signal and the results are shown on the display. The voltage change is approximately the same scale of mV voltage signal (due to ΔR change value is less than R). In order to realize a high precision scale, the ability to process 0.1uV signal is very necessary. On the contrary, if ADC performance is not good enough to achieve the target (noise processing), voltage signal must be amplified through OP so as to meet the precision requirement.

The factors are more complicated after OP amplifier. Not only OP capability should satisfy the request but the peripheral resistors must achieve the requirement of temperature change as well. The total cost will be relatively high under this kind of solution (through OP amplifier). Therefore, the accuracy of ADC is indeed critical and is the key element. If the signal that outputted from Load Cell must be transformed to digital signal, high resolution ADC, equipping with the ability to process 0.1uV signal, is in need. Only this way, a qualified scale can be accomplished.

Load Cell resistance of pricing scales is around 1KΩ and ΔR change value is only 1Ω maximally. Suppose the voltage of VIN+-VIN- is 3V, the output signal VIN+-VIN- is only 3mV. To realize kitchen scales of 3000 Count and internal/external resolution is 1:10, the minimum signal value should $\frac{3mV}{3000\times10}=0.1uV$

Determining whether ADC performance could achieve the specification depends on how to control and stabilize the resolution by RMS Noise. The internal resolution which people presumed by visual interpretation was usually one count rolling after the software processing. The full-scale represents the internal resolution and the signal of one count was on behalf of 2~3 times RMS Noise. With regards to the pricing scales which need to be certificated, the internal/external resolution ratio should reach 1:10 at least. As for the electrical scales without certification, in order to have the perfect performance, will try to improve the external resolution as much as possible and reduce the ratio of internal/external resolution. However, it is not easy to stabilize external value by regular software processing when the ratio is less than 1:3.

For developing electrical scales, the bottleneck of how to achieve the utmost internal resolution by the series of HY11PXX is not ADC resolution but Input RMS Noise. At the configuration of PGA=8, ADC Gain=16, OSR=32768, the Input RMS Noise is around 100nV while 8 datum out per second. Due to Input Noise of the series of HY11PXX is composed of thermal noise; we can further reduce the noise through average software method. (Other IC P/N's Input Noise is composed of Flick Noise. It cannot be reduced by average software.) According to our detailed experiment findings, if we averaged 8 datum, the Input RMS Noise could be decreased to 40nV. Moreover, if 16 data is averaged, the noise could be further reduced to 30nV, but it took 2 seconds at least to be stabled. In other words, averaging 16 datum took more time to stabilize the resolution.

Therefore, if we average 8 datum with the software, the Input RMS Noise is around 40nV. 3 times RMS Noise represents one count rolling(= 120nV). The full-scale 1mV/V Load Cell can reach 2.4mV when using Load Cell driving voltage of 2.4V. Under this circumstance, the internal resolution would have 20000 Counts.

2.2 Control IC

2.2.1 11P13 ADC Features

- Low Operating Voltage →ADC minimum operating voltage:2.4V
- ADC Gain →×1/4 ~ ×16
- Build-In Programmable Gain Amplifier (PGA) →×1 ~ ×8
- Reference Voltage Configure →×1/2 & ×1
- Offset Configure →0 , ±1/4Vref , ±1/2Vref , ±3/4Vref
- Build-In Input Signal Switch →V+ V- , V+ short, V- short ,V+ V- cross, 4 Switch Modules
- Multi-Channel Input Signal
- Various Output Rate Selection→ ADCK / 256 ~ ADCK / 32768
- High Resolution → 18-bit Output resolution
- Minimum Resolution Voltage → Minimum resolution voltage: 0.07uV
- Rail to Rail Signal Output → Minimum Input Signal: VSS – 0.2V, Maximum: VDDA
- Gain Low Temperature Drift Parameter →10 PPM/℃

2.2.2 11P13 IC Features

- Various System Oscillation Frequency Selection → Internal 32K, 2MHz, external 32K ~ 16MHz
- Low Power →Turn On ADC by internal 2MHz. Maximum power consumption<1mA
- Build-in LCD Driver → 4×20 display
- Low Voltage Detect → Multi-Step Power Voltage Detection
- Build-in multi-steps regulated output → 3.3V，2.93V，2.64V，2.4V
- SPI communication
- PWM/PDM output

3. Design Scheme

3.1 Hardware Illustration

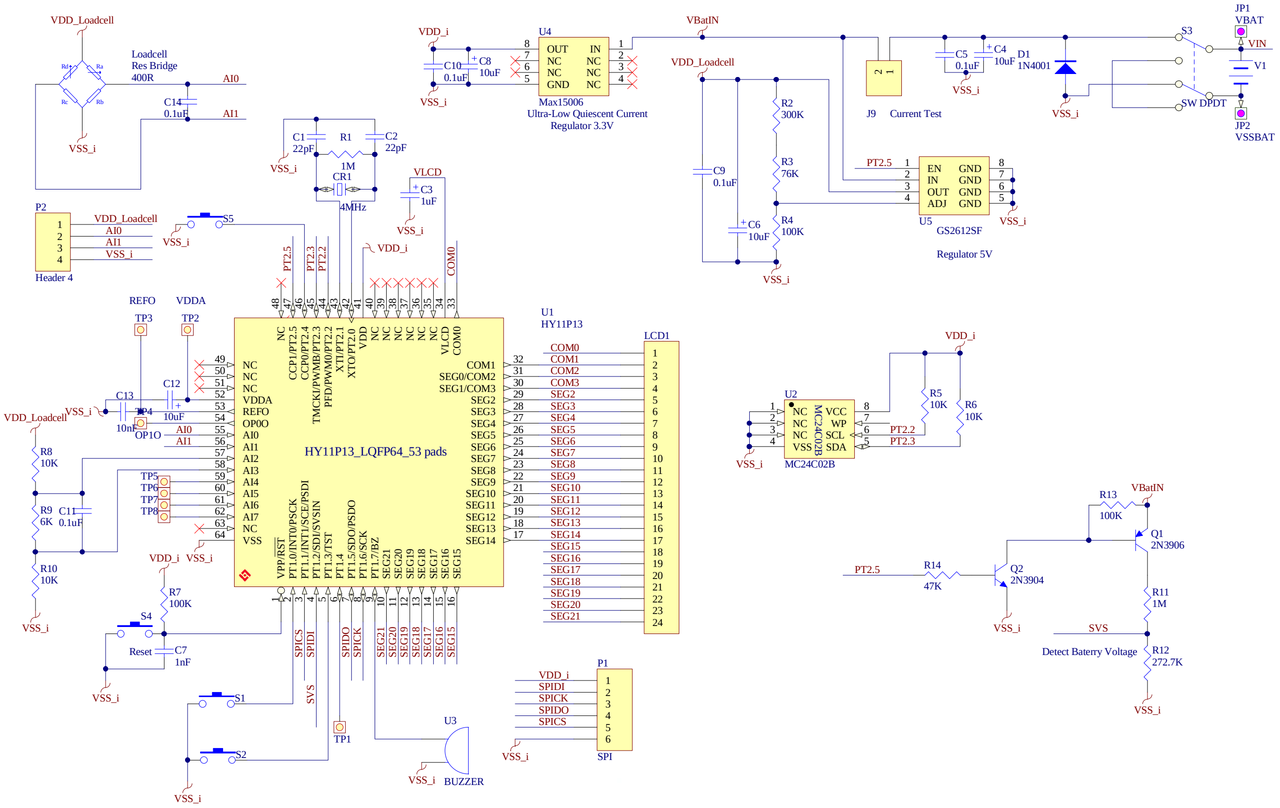


Figure 1

The whole circuit can be divided into 3 parts：

- ADC
- Low Voltage Detect Circuit
- Power and Peripheral Circuit

3.1.1 ADC

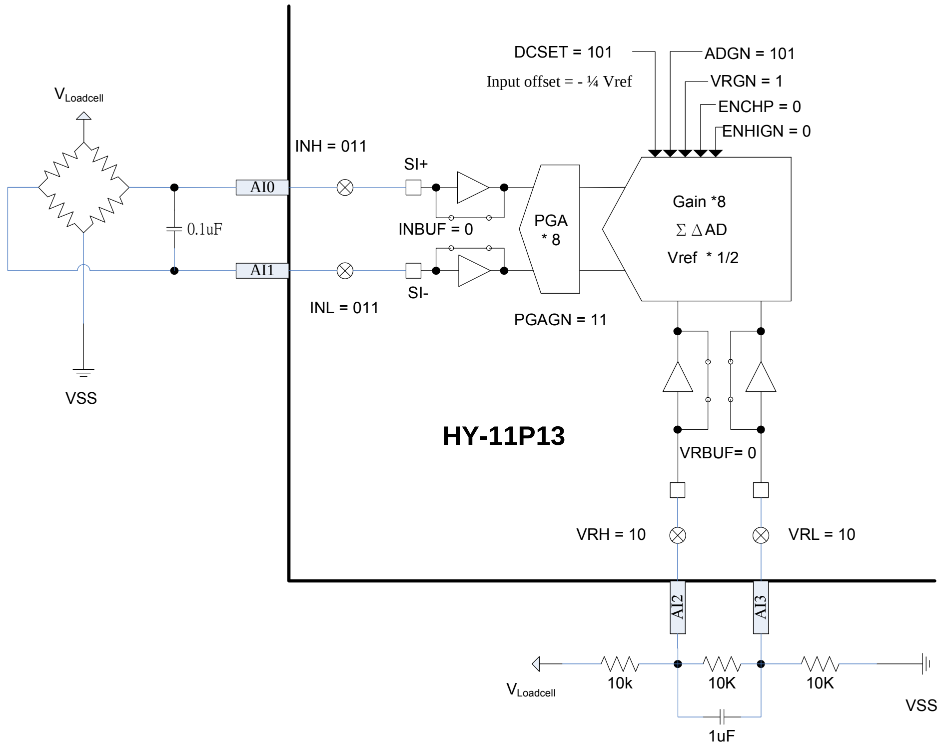


Figure 2

Output voltage of Load Cell was provided by 3.3V regulator. This voltage enables Load Cell to 2mV/V to have maximum output signal, 6.6mV. ADC internal PGA and Gain is configured as 8-amplification. If VRGN equals to 1(VREF x 1/2), it could fulfill the minimum resolution requirement, 0.02uV when ADC outputs ±15 bit. Since HY11P13 equips with good temperature characteristics and its general temperature curve is around ±10ppm, it only takes 2~3 low temperature drift resistances and Load Cell to accomplish the pricing scale certification request. When the temperature was changing, to make sure ADC had enough operating time, it's necessary and proposed to connect capacitors which were located at AI0-AI1& AI2-AI3.

3.1.2 Low Voltage Detect Circuit

Since VDD power output through the regulator, it is impossible to use VDD to implements low voltage detect. Battery voltage needs to be divided and input through SVSIN of HY11P13 internal power managing system. Battery voltage was divided to SVSIN through R1 & R2 while PT2.5 output high. SVSOP of HY11P13 power managing system would show 1 if SVSIN voltage lowers than 1.2V so that is can judge whether battery voltage is too low. Owning to the low temperature drift characteristic that HY11P13 internal ACM possessed; it is recommended to adopt low temperature coefficient R1 & R2 resistors so as to carry out precise low voltage judgment.

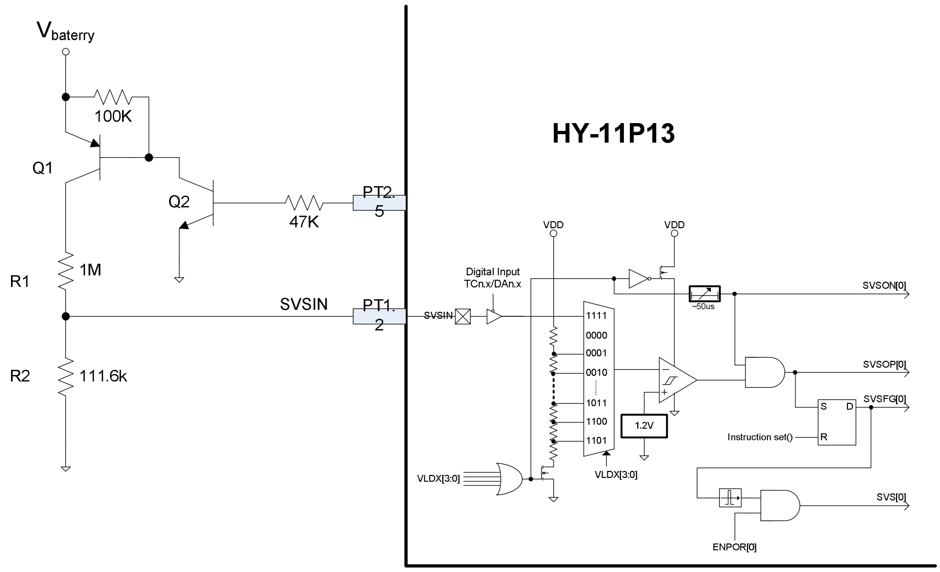


Figure 3

3.1.3 Power and Peripheral Circuit

Battery power was provided to VDD of HY11P13 through 3.3V regulator. Due to IC power consumption at Sleep Mode was less than 1uA, the power consumption of the whole system depended on the consumption of 3.3V regulator.

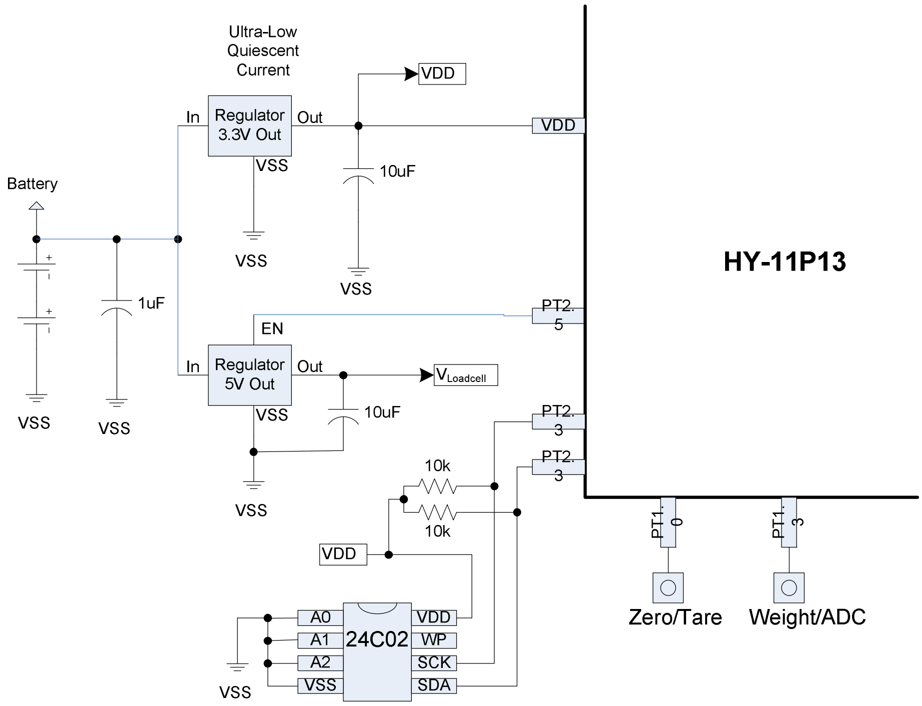


Figure 4

Output voltage of 5V regulator supported Load Cell and reference voltage.

3.2 Software Process

3.2.1 Increasing ADC Output Bit by Software Average

Since the small signal is amplified to 128 times, ADC output bit can reach ±15 bit. However, ADC resolution can increase 1~2 bit by software average method. Adding another 7 ADC buffer values to ADC new value and then divided it by 8. The value will be placed to ADC OUT (See Figure 4). This purpose of average 8 data is to scatter noise and increase the ADC output bit.

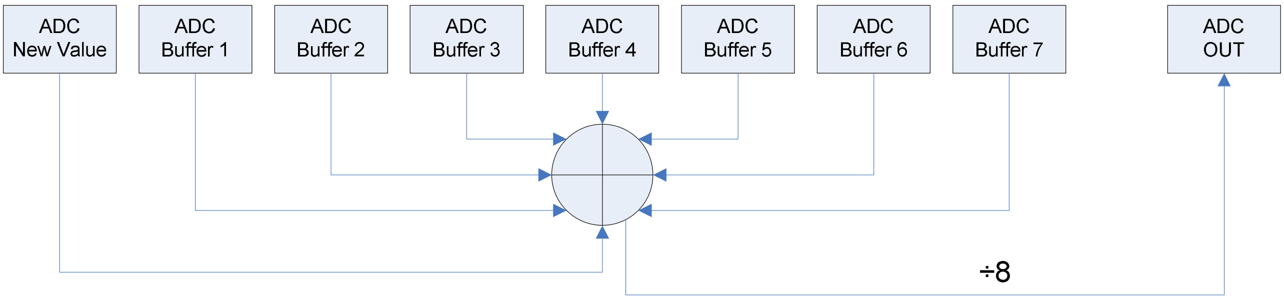


Figure 5

Once ADC new value is received, move it to Buffer 1, Buffer 1 to Buffer 2…, Buffer 6 to Buffer 7, as shown in Figure 6

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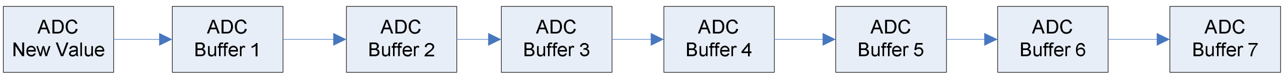


Figure 6

Due to the fact that reflection time of data average is slow, as indicated in Figure 4, it is necessary to skip this program when the process (see Figure 5) brings the greater ADC value. If ADC new value is greater than 0x200, just record it and it is needless to do any further operation. However, the next value is still greater than 0x200; it will substitute all of the ADC buffer values. On the contrary, once the next value is not over 0x200, the process of data average shall continue.

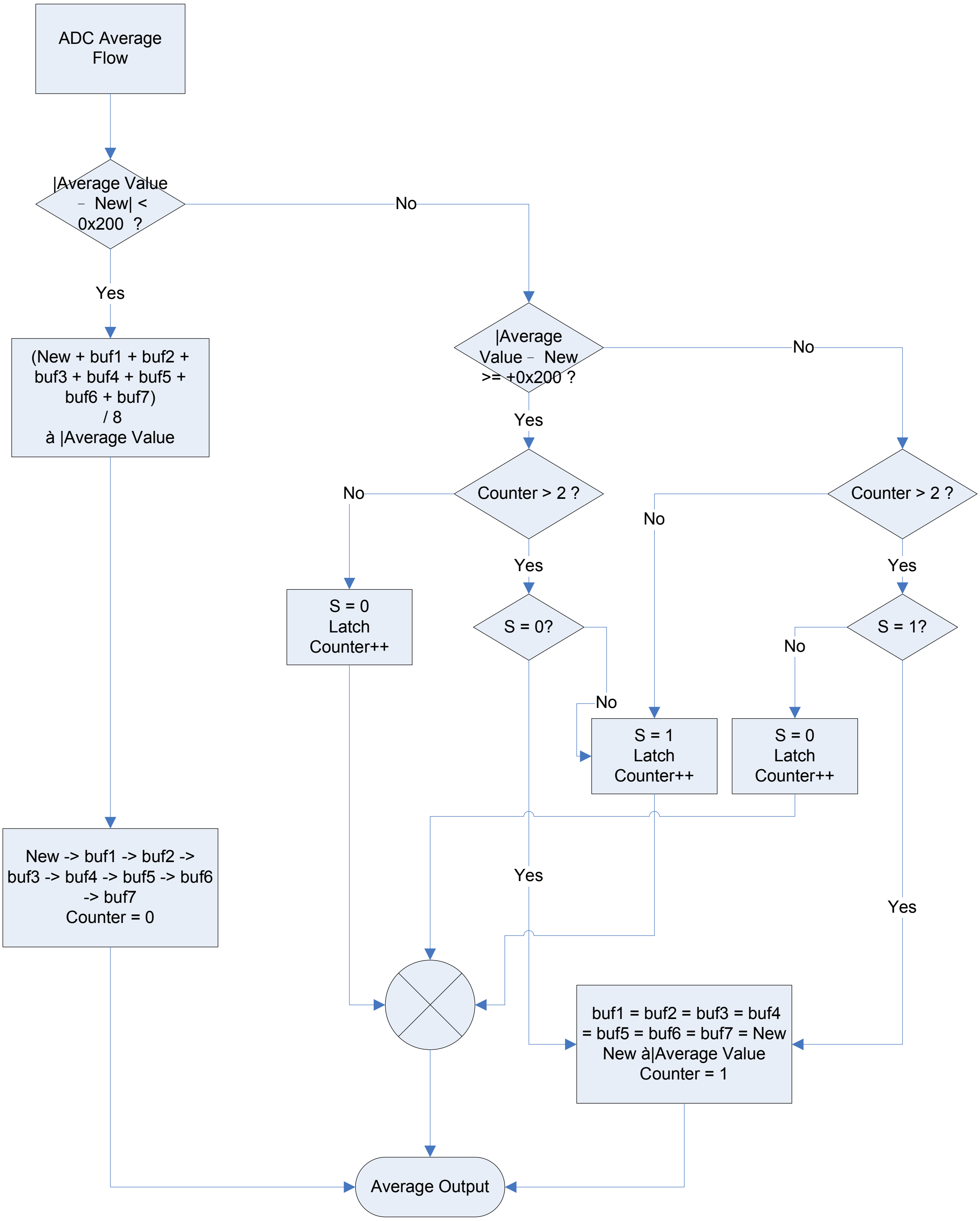

ADC Average Flow
|Average Value – New| < 0x200 ?
No
Yes
(New + buf1 + buf2 + buf3 + buf4 + buf5 + buf6 + buf7) / 8 à |Average Value
|Average Value – New >= +0x200 ?
No
Yes
Counter > 2 ?
No
Yes
Counter > 2 ?
No
Yes
S = 0 Latch Counter++
S = 0?
No
S = 1?
No
S = 1 Latch Counter++
S = 0 Latch Counter++
Yes
Yes
New -> buf1 -> buf2 -> buf3 -> buf4 -> buf5 -> buf6 -> buf7 Counter = 0
buf1 = buf2 = buf3 = buf4 = buf5 = buf6 = buf7 = New
New à|Average Value
Counter = 1
Average Output

Figure 7

4. Technical Specification

4.1 Test Result of Temperature Drift

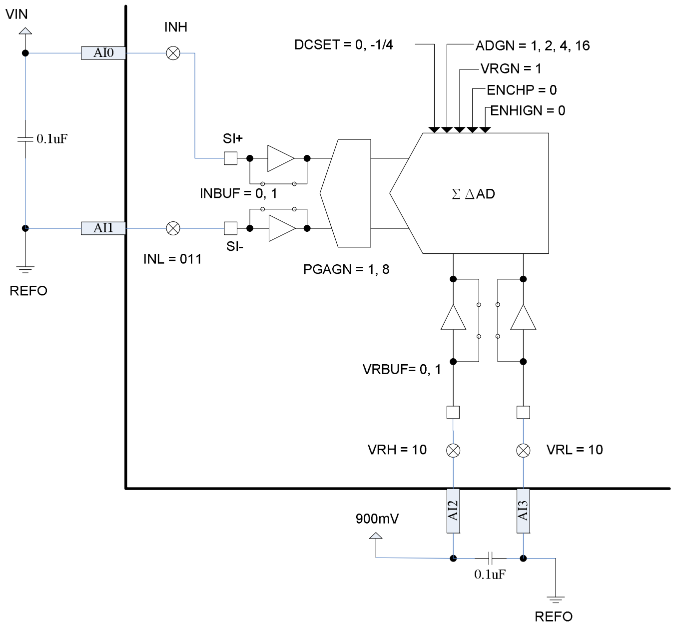


Figure 8 Test Circuit of Temperature Drift

Test result of Gain drift

Dither = 100 , Chopper clock = 101 , Chopper ON , OSR = 111 , ADC Clock=250KHz , VDD = 3V , VDDA = 2.4 Referance Voltage = 900mV				
Test Mode	-20℃ ~ 20℃	0℃ ~ 20℃	40℃ ~ 20℃	60℃ ~20℃
	PPM/℃			
Gain = 1*1，Offset = 0 ，AIN Buffer = Off， Ref Buffer = Off	-1.89	1.91	-0.95	-1.17
Gain = 1*1，Offset = 0 ，AIN Buffer = On， Ref Buffer = Off	-2.24	-0.42	-0.98	-1.57
Gain = 1*1，Offset = 0 ，AIN Buffer = Off， Ref Buffer = On	6.61	7.20	-7.45	-7.41
Gain = 1*1，Offset = 0 ，AIN Buffer = On， Ref Buffer = On	5.93	6.66	-6.70	-6.86
Gain = 1*2，Offset = 0 ，AIN Buffer = Off， Ref Buffer = Off	-1.55	-1.30	-1.15	-0.49
Gain = 1*2，Offset = 0 ，AIN Buffer = On， Ref Buffer = Off	-1.43	-1.18	-1.10	-0.66
Gain = 1*2，Offset = 0 ，AIN Buffer = Off， Ref Buffer = On	7.25	6.27	-6.24	-6.13
Gain = 1*2，Offset = 0 ，AIN Buffer = On， Ref Buffer = On	6.76	6.85	-7.21	-6.51
Gain = 1*4，Offset = 0 ，AIN Buffer = Off， Ref Buffer = Off	-0.90	-1.91	-1.16	-0.63
Gain = 1*4，Offset = 0 ，AIN Buffer = On， Ref Buffer = Off	-0.85	-1.78	-2.40	-0.88
Gain = 1*4，Offset = 0 ，AIN Buffer = Off， Ref Buffer = On	7.20	6.69	-6.86	-6.00
Gain = 1*4，Offset = 0 ，AIN Buffer = On， Ref Buffer = On	7.33	7.12	-7.45	-6.24
Gain = 1*16，Offset = 0	-0.73	-1.72	-1.12	-0.55
Gain = 8*4，Offset = 0	1.66	3.10	0.25	0.12
Gain = 8*16，Offset = 0	12.10	10.40	-6.90	-3.03
Gain = 1*1，Offset = -1/4Vref	1.32	0.82	-2.74	-2.83
Gain = 1*2，Offset =-1/4Vref	-0.81	-0.59	-0.87	-0.94
Gain = 1*4，Offset = -1/4Vref	-0.51	-0.74	-1.18	-0.87
Gain = 1*16，Offset =-1/4Vref	-0.10	-0.55	-1.19	-1.19
Gain = 8*4，Offset = -1/4Vref	0.57	1.57	-2.00	-1.33
Gain = 8*16，Offset = -1/4Vref	7.27	5.98	4.75	-1.31

The maximum parameter of Gain temperature drift is 12PPM/℃. To realize a scale of 3rd class certification, ±1.5 Degree drift parameter under -10℃~40℃ is equal to 20 PPM/℃.

Test result of OFFSET drift

Dither = 100 , Chopper clock = 101 , Chopper ON , OSR = 111 , ADC Clock = 250KHz , VDD = 3V , VDDA = 2.4				
Mode	-20 ~ 20	0 ~ 20	40 ~ 20	60 ~20
	nV/℃			
Gain = 1*1，Offset = 0 ，AIN Buffer = Off， Ref Buffer = Off	714.96	539.08	980.58	581.00
Gain = 1*1，Offset = 0 ，AIN Buffer = On， Ref Buffer = Off	-2388.04	-2204.52	-2106.70	-2333.95
Gain = 1*1，Offset = 0 ，AIN Buffer = Off， Ref Buffer = On	645.31	475.93	740.56	525.74
Gain = 1*1，Offset = 0 ，AIN Buffer = On， Ref Buffer = On	-2600.92	-2770.58	-2136.08	-2269.00
Gain = 1*2，Offset = 0 ，AIN Buffer = Off， Ref Buffer = Off	255.90	207.35	477.90	827.18
Gain = 1*2，Offset = 0 ，AIN Buffer = On， Ref Buffer = Off	-2923.29	-2914.77	-2261.80	-1938.61
Gain = 1*2，Offset = 0 ，AIN Buffer = Off， Ref Buffer = On	249.03	168.16	434.16	744.57
Gain = 1*2，Offset = 0 ，AIN Buffer = On， Ref Buffer = On	-2816.38	-2828.49	-2352.39	-2027.15
Gain = 1*4，Offset = 0 ，AIN Buffer = Off， Ref Buffer = Off	107.29	77.86	346.58	510.29
Gain = 1*4，Offset = 0 ，AIN Buffer = On， Ref Buffer = Off	-3097.09	-2967.50	-2487.59	-2347.65
Gain = 1*4，Offset = 0 ，AIN Buffer = Off， Ref Buffer = On	121.11	39.05	349.34	476.37
Gain = 1*4，Offset = 0 ，AIN Buffer = On， Ref Buffer = On	-3102.68	-3026.86	-2535.73	-2322.09
Gain = 1*16，Offset = 0	-108.32	-86.15	-102.67	-84.66
Gain = 8*4，Offset = 0	-16.00	1.58	13.07	28.88
Gain = 8*16，Offset = 0	-38.07	-27.90	-23.28	-29.65
Gain = 1*1，Offset = -1/4Vref	1542.99	1893.42	1861.54	1497.64
Gain = 1*2，Offset =-1/4Vref	858.06	967.18	1115.57	1294.97
Gain = 1*4，Offset = -1/4Vref	480.44	568.10	574.48	715.75
Gain = 1*16，Offset =-1/4Vref	-17.30	3.55	-38.61	-13.29
Gain = 8*4，Offset = -1/4Vref	32.75	60.18	49.19	60.29
Gain = 8*16，Offset = -1/4Vref	-21.29	-9.80	-23.14	-21.91

If the input voltage of Load Cell is 3.3V and output signal is 2mV/V, the maximum output voltage shall be 6.6mV (3000 Count). According to the standard of 3rd-class scale, the maximum offset drift cannot over ±1e/5℃(±0.2e/℃), which is smaller than 440nV/℃. Under -10℃~40℃ ambient temperature condition, the maximum Offset drift of HY11P13 when Gain=128 is 20nV/℃. Therefore, when choosing Load Cell, users must make sure the Gain drift is under 8 ~ 10PPM/℃ and Offset is lower than 400nV/℃ to conform to certified standard.

5. Conclusion

The maximum parameter of Gain temperature drift is 12PPM/℃. Realizing a scale of 3rd class certification, ±1.5 degree drift parameter under -10℃~40℃ is equal to 20 PPM/℃. According to the standard of 3rd class certification, the parameter of offset cannot over ±1e/5℃(±0.2e/℃) under -10℃~40℃ ambient temperature condition.

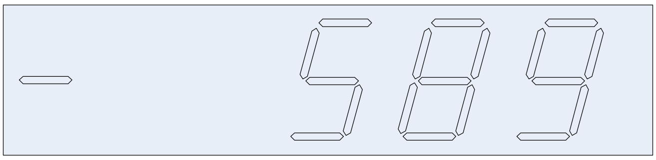
Standard of 3rd Class Certification	Chip : HY11P13
Offset parameter<±1e/5℃(±0.2e/℃) Ambient temperature : -10℃~40℃	**Application Condition :** 6.6mV(3000Count) (Max. Output Voltage) *Ex : Load Cell Input Voltage 3.3V X Max. Output Voltage 2mV/V=6.6mV(3000Count)* **Test Result :** Offset drift parameter about 20nV/℃ while Gain=128 **Conclusion:** <440nV/℃

6. Operation Description

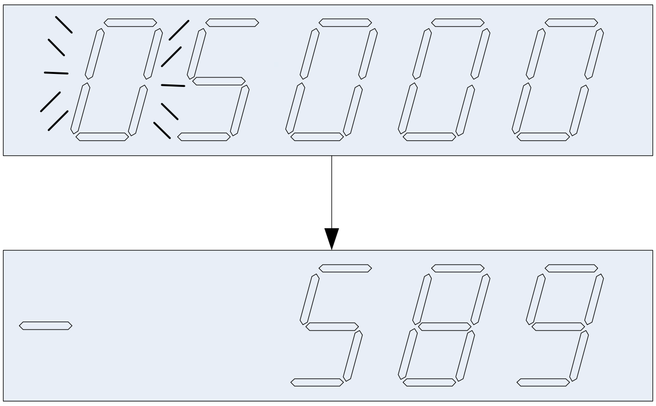
6.1 Usage

6.1.1 Calibration Description

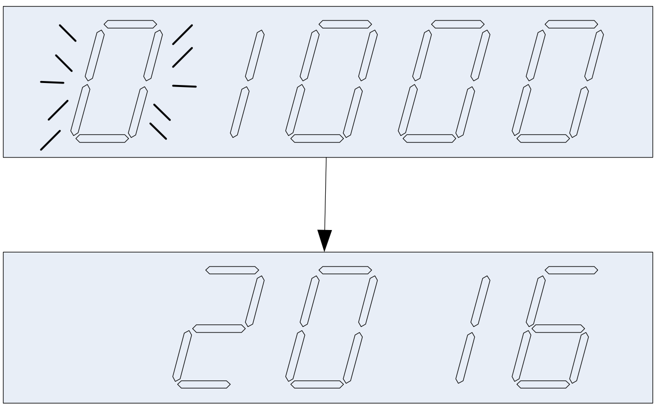
The program automatically enters into calibration mode if no calibration value exists in EEPROM. If there is a need to re-calibrate, click PT1.0 to turn the power on. After power on, let go PT1.0, ADC output code will be shown first in the calibration mode.



- Click PT1.0 to set the weight at full load (Max. Range of the measurement), key in the value on the blinking space. Click PT1.3 to ascend the value, from 0~9.
- Click PT1.0 to move right to the last space for going into zero point calibration procedure. At this point, it shows ADC output code, then re-click PT1.0 for saving zero value and go into next process.

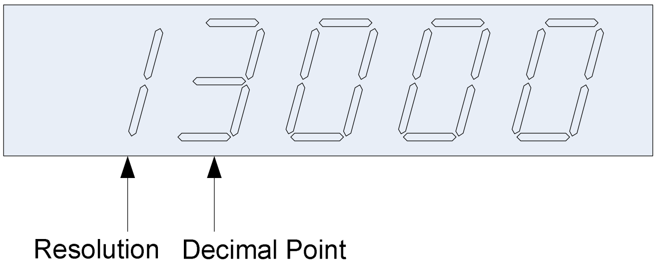


- After finishing zero point calibration, next is to adjust standard weight calibration.



- Click PT1.3, value ascends, from 0 to 9. Click PT1.0 to move right to the last space for going into standard weight calibration procedure. Put the counterpoise as the standard weight criterion, and then re-click PT1.0 for saving calibration value, and goes into the next process.

- After standard weight calibration, go into the process of selecting resolution and decimal digits. Click PT1.3, the value ascends from 0 to 9.
  Click PT1.0 to move right to the last space and then re-click PT1.0 to save all value to EEPROM. Finally, get access into the weighing mode.



6.1.2 Weighing Description

Before weighing, it is necessary to have calibration value in EEPROM. If not, it is impossible to weigh. If re-calibration is in need, click PT1.0→Zero or Tare Click PT1.0→ " Zero" or " Tare"

When the value is less than the one-tenth of the full load weight, PT1.0 is "Zero" function.

When the value is more than the one-tenth of the full load weight, PT1.0 is "Tare" function.

Click PT1.3→ switching display the ADC output code and weight value

6.1.3 Auto Zero

When the weight is within ± 1/4 div of zero point range and it lasts for 1 second, Auto Zero will be started. If Auto Zero is more than one-tenth of the full load weight, this function is disabled.