HYCON 紘康科技

HY11P33
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x20 LCD Driver
18-Bit ΣΔADC

HY11P33

Embedded 18-Bit ΣΔADC
8-Bit RISC-like Mixed Signal Microcontroller

Table of Content

Notes:

1. Improvements and contents to this user guide necessitated by improvements to equipment may be made by Hycon Technology at any time and without notice. You may download the most up to date version of this user guide at http://www.hycontek.com.

2. Under no circumstances will Hycon Technology be liable in any way for third party copyright problems concerning graphs and application circuits contained in this user guide.

3. Hycon Technology guarantees that features, typical applications and functions of this product are compliant with this user guide when being used in stand-alone situation. Hycon Technology does not make the same guarantee when this product is used together with your finished goods or equipment. Hycon Technology advises you to conduct comprehensive evaluations and tests.

4. You, and not Hycon Technology, are responsible for making sure that the internal power consumption of IC is within limits given in this user guide by following the using conditions of input voltage, output voltage, and load current. Under no circumstances will Hycon Technology be liable in any way for damage caused by your using this product, even for a very short period of time, in conditions exceeding limits specified in this user guide.

5. In spite of embedded static protection circuit of this product Hycon Technology advises you do not apply static that is over protection circuit capacity.

6. Hycon Technology advises you not to use this product in mission critical circuits or components of mission critical circuits unless authorized with prior written permission. This may include, but not limited to, health and medical equipment, disaster prevention equipment, vehicles, automotive equipment, aviation equipment, and equipment and devices that may affect human body.

7. Hycon Technology strives to improve quality and reliability of this product. However every semiconductor will fail at certain probability and this may cause personal injury and/or fire. Hycon Technology advises you to pay special attention to redundancy and safety level in designing your end product. This may prevent incidents and accidents from happening.

8. Transfer and reproduction of part or all of the contents in this user guide in any format without the prior permission of Hycon Technology is prohibited.

1. Features

- 8-bit RISC, 66 instructions included.
- Operating voltage range: 2.2V to 3.6V, operation temperature range: -40℃~85℃.
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
  - Active Mode 300uA@2MHz
  - Standby Mode 3uA@28KHz
  - Sleep Mode 1uA
- 4K Word OTP (One Time Programmable) Type Program Memory, 256 Byte Data Memory
- Brownout detector and Watch Dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D)
  - Built-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x、multiple input signal gain selection.
  - Built-in Input zero point adjustment can increase measurement range according to different application.

- Conversion rate up to ~1.95ksps
- 1.0V internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function.
- Analog voltage source, VDDA equips with 10mA low dropout regulator function
- 4x20 LCD Driver
  - 1/4 Duty, 1/3 Bias
  - Built-in Charge Pump regulated circuit, providing 4 LCD Bias voltage
- 8-bit Timer A
- 8-bit Timer C module can generate PWM/PFD function.
- Built-in EPROM (BIE)
- Support 6 stack level

## 2. Pin Definition

2.1 HY11P33 LQFP64 Pin Diagram
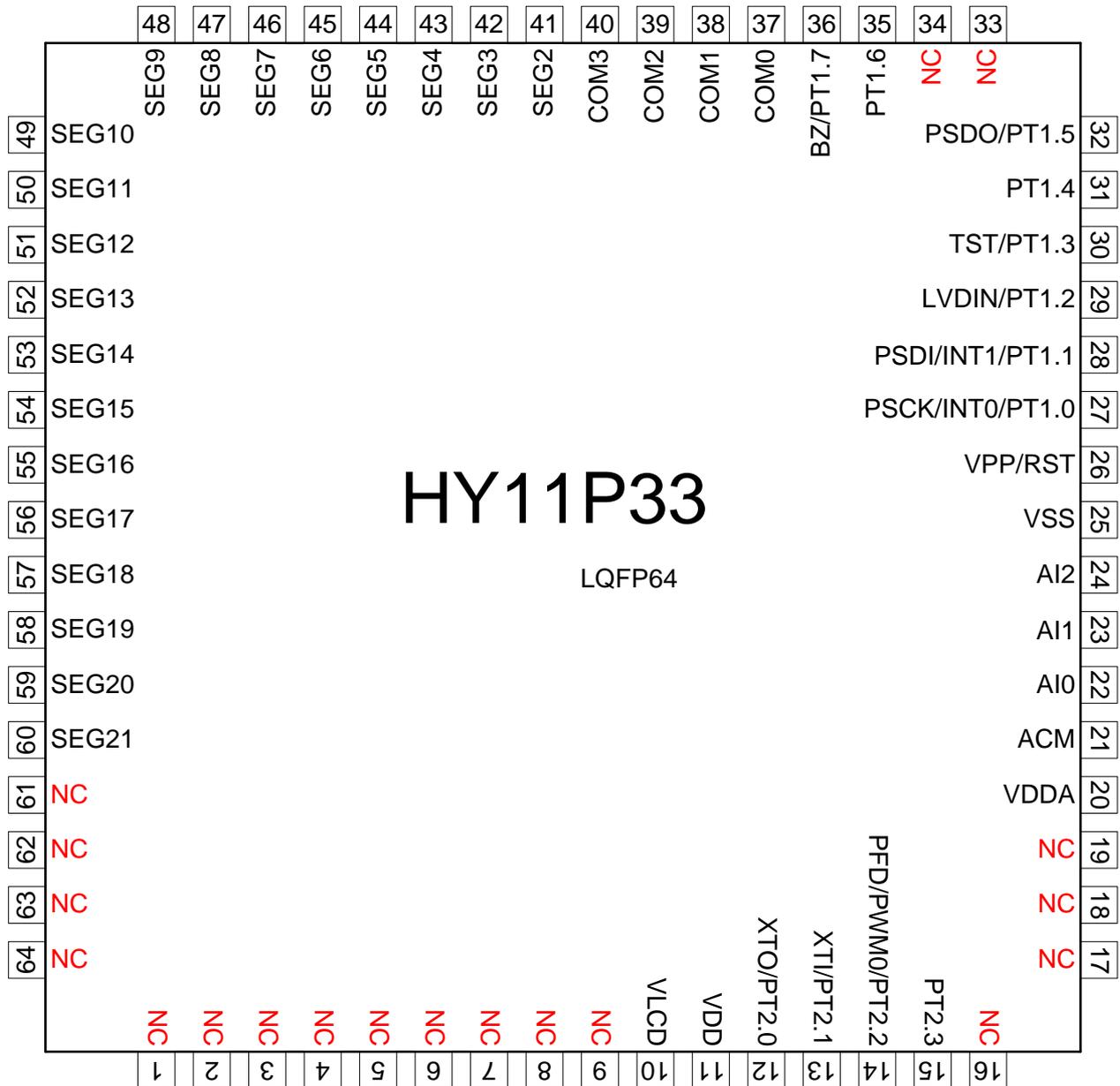
Figure 2-1 HY11P33 LQFP64 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 is not configured as external pin button, it can help to enhance the anti-interference ability

2.2 HY11P33 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

No.	Pin Name	Pin Characteristics		Function Description
	HY11P33	Pin Type	Buffer Type	
1	NC	O	A	Segment output for LCD
2	NC	O	A	Segment output for LCD
3	NC	O	A	Segment output for LCD
4	NC	O	A	Segment output for LCD
5	NC	O	A	Segment output for LCD
6	NC	O	A	Segment output for LCD
7	NC	O	A	Segment output for LCD
8	NC	O	A	Segment output for LCD
9	NC	-	-	Unused
10	VLCD	P	P	Power supply for LCD
11	VDD	P	P	Power supply for IC operation
12	PT2.0/XTO	I/O	S	Digital I/O
		A	A	External Oscillator input pin
13	PT2.1/XTI	I/O	S	Digital I/O
		A	A	External Oscillator input pin
14	PT2.2/PWM0/PFD	I/O	C	Digital I/O
		O	C	PWM output port
		O	C	PFD output port
15	PT2.3	I/O	S	Digital I/O
16	NC	-	-	Unused
17	NC	-	-	Unused
18	NC	-	-	Unused
19	NC	-	-	Unused
20	VDDA	P	P	Regulator output, analog circuit power
21	ACM	P	P	Common ground pin for internal analog circuit
22	AI0	A	A	Analog input channel
23	AI1	A	A	Analog input channel

24	AI2	A	A	Analog input channel
25	VSS	P	P	Ground pin of IC operation power supply.
26	RST/VPP	I P	S P	Reset IC EPROM programming voltage input
27	PT1.0/INT0/PSCK	I I I	S S S	Digital input Interrupt input INT0 OTP programming interface SDI
28	PT1.1/INT1/PSDI	I I I	S S S	Digital input Interrupt input INT1 OTP programming interface SDI
29	PT1.2/LVDIN	I A	S A	Digital input LVD external signal input pin
30	PT1.3/TST	I I	S S	Digital input Test Mode input pin (invalid)
31	PT1.4	I/O	S	Digital I/O
32	PT1.5/PSDO	I/O O	S C	Digital I/O OTP programming interface SDO
33	NC	-	-	Unused
34	NC	-	-	Unused
35	PT1.6	I/O	S	Digital I/O
36	PT1.7/BZ	I/O O	S C	Digital I/O Buzzer input pin
37	COM0	O	A	COM segment output for LCD
38	COM1	O	A	COM segment output for LCD
39	COM2	O	A	COM segment output for LCD
40	COM3	O	A	COM segment output for LCD
41	SEG2	O	A	Segment output for LCD

42	SEG3	O	A	Segment output for LCD
43	SEG4	O	A	Segment output for LCD
44	SEG5	O	A	Segment output for LCD
45	SEG6	O	A	Segment output for LCD
46	SEG7	O	A	Segment output for LCD
47	SEG8	O	A	Segment output for LCD
48	SEG9	O	A	Segment output for LCD
49	SEG10	O	A	Segment output for LCD
50	SEG11	O	A	Segment output for LCD
51	SEG12	O	A	Segment output for LCD
52	SEG13	O	A	Segment output for LCD
53	SEG14	O	A	Segment output for LCD
54	SEG15	O	A	Segment output for LCD
55	SEG16	O	A	Segment output for LCD
56	SEG17	O	A	Segment output for LCD
57	SEG18	O	A	Segment output for LCD
58	SEG19	O	A	Segment output for LCD
59	SEG20	O	A	Segment output for LCD
60	SEG21	O	A	Segment output for LCD
61	NC	O	A	Segment output for LCD
62	NC	O	A	Segment output for LCD
63	NC	O	A	Segment output for LCD
64	NC	O	A	Segment output for LCD

Table 2-1 Pin Definition and Function Description

# 3. Application Circuit

3.1 Bridge Sensor Ⅰ
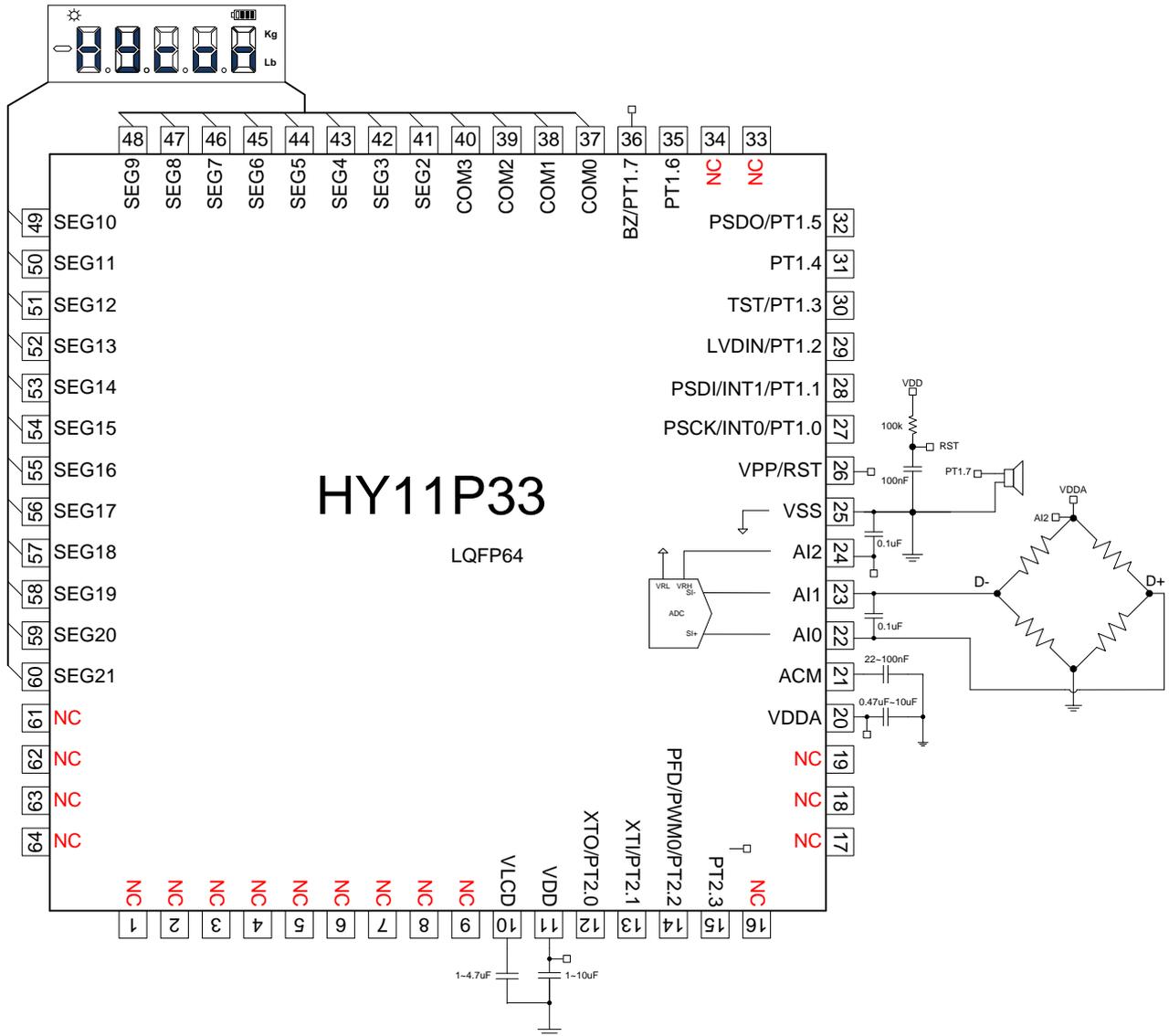
Figure 3-1 Application Circuit of Bridge Sensor

Note 1：DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

4. Function Description

4.1 Internal Block Diagram
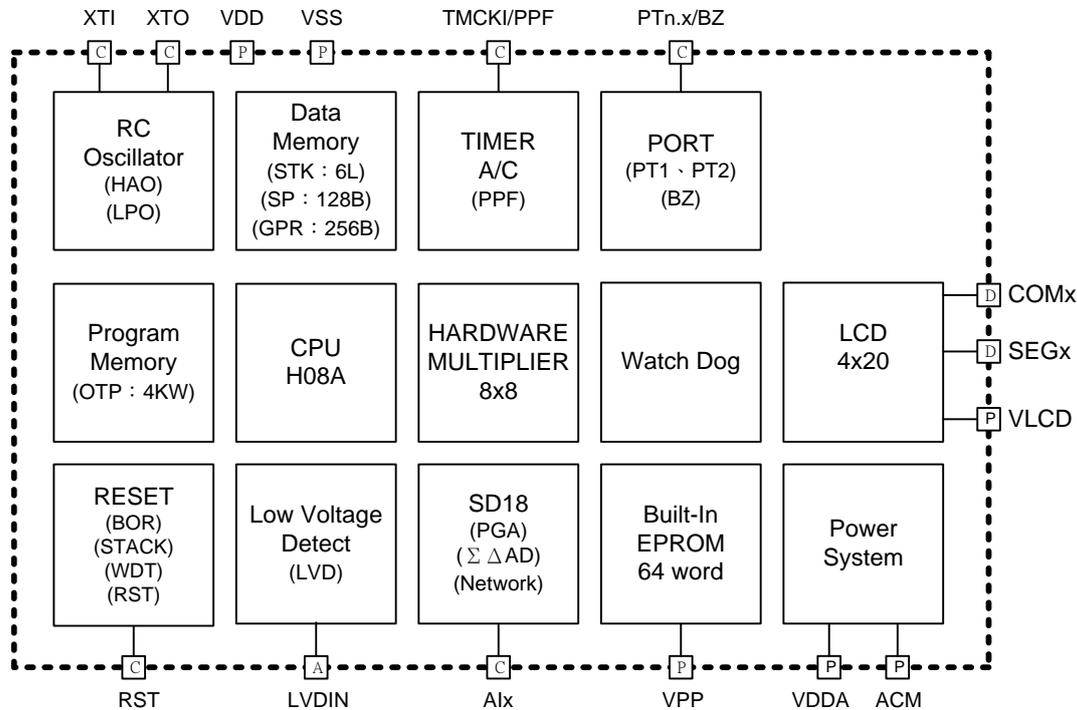
Figure 4-1 HY11P33 Internal Block Diagram

4.2 Related Description and Supporting Documents

IC Function Related Operating Instruction

DS-HY11P33-Vxx	HY11P33 Datasheet
UG-HY11S14-Vxx	HY11Pxx Series User's Manual
APD-CORE002-Vxx	H08A Instruction Description

Development Tool Related Operating Instruction

APD-HYIDE006-Vxx	HY11xxx Series Development Tool Software Instruction Manual
APD-HYIDE005-Vxx	HY11xxx Series Development Tool Hardware Instruction Manual
APD-OTP001-Vxx	OTP Products Programming Pin Manual

Product Production Related Operating Instruction

|	
APD-HYIDE004-Vxx	HY1xxxx Series Production Line Specialized Programmer Manual
BDI-HY11P33-Vxx	HY11P33 Individual Product Die Bonding Information

4.3 SD18 Network
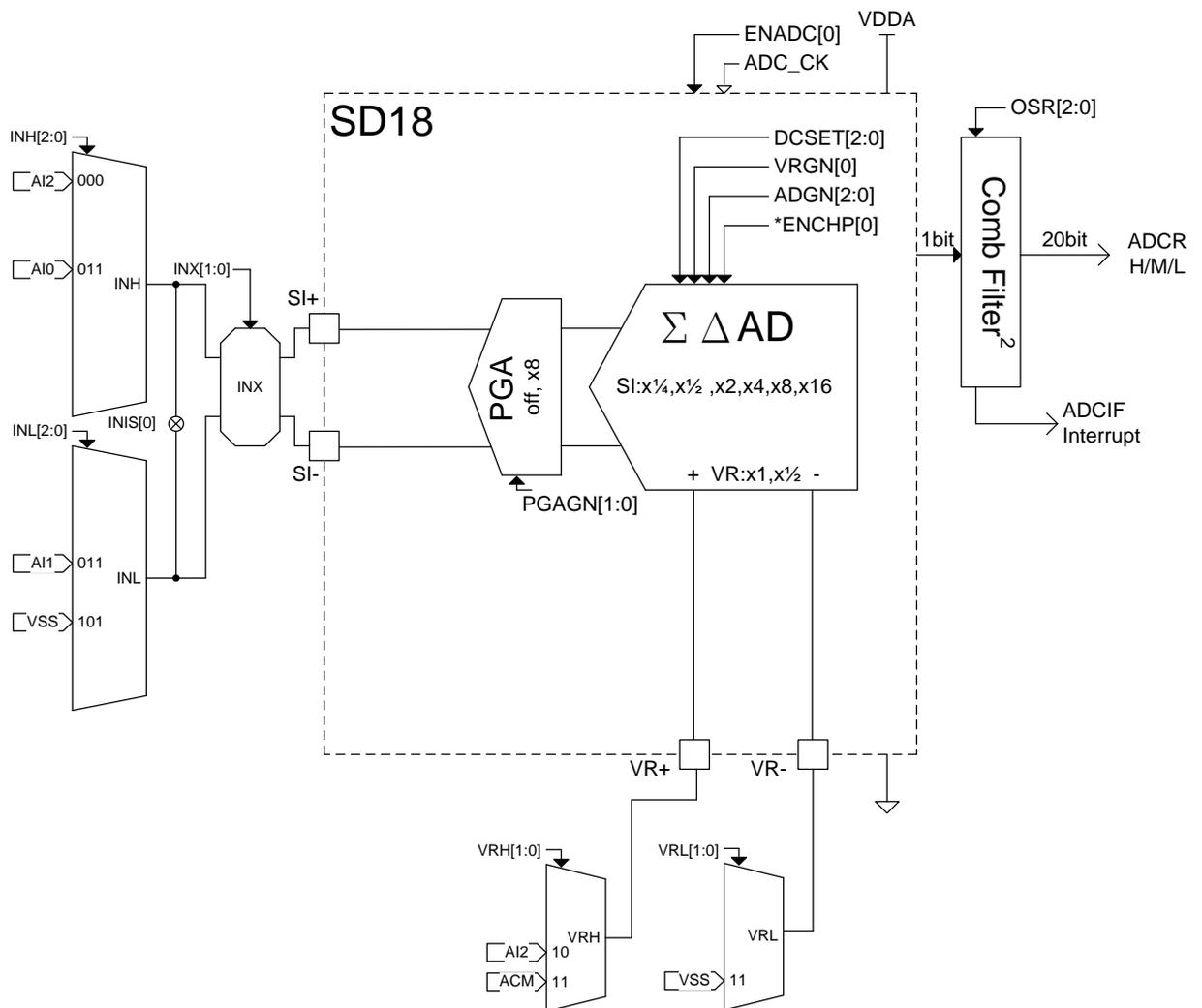
Figure 4-2 SD18 Network

5. Register List

										A-RESET	i-RESET	R/W
								"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1				
								"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition				
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W
00H	INDF0	Contents of FSR0 to address data memory· value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
01H	POINC0	Contents of FSR0 to address data memory· value of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
02H	PODEC0	Contents of FSR0 to address data memory· value of FSR0 post-decremented								N/A	N/A	·,·,·,·,·,·,·,·
03H	PRINC0	Contents of FSR0 to address data memory· value of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
04H	PLUSW0	Contents of FSR0 to address data memory· value of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
05H	INDF1	Contents of FSR1 to address data memory· value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
06H	POINC1	Contents of FSR1 to address data memory· value of FSR0 post-incremented								N/A	N/A	·,·,·,·,·,·,·,·
07H	PODEC1	Contents of FSR1 to address data memory· value of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
08H	PRINC1	Contents of FSR1 to address data memory· value of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
09H	PLUSW1	Contents of FSR1 to address data memory· value of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
0FH	FSR0H								FSR0[8]	x	....u	-,-,-,- -,-,-,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
11H	FSR1H								FSR1[8]	x	....u	-,-,-,- -,-,-,*
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
16H	TOSH					TOS[11]	TOS[10]	TOS[9]	TOS[8]	 0000	 0000	-,-,-,-,*,*,*,*
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV			STKPRT[2:0]			000. .000	000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH					PC[11]	PC[10]	PC[9]	PC[8]	 0000	 0000	-,-,-,-,*,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1DH	TBLPTRH					TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	 0000	 0000	-,-,-,-,*,*,*,*
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1FH	TBLDH	Program Memory Table Latch High Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
21H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
22H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
23H	INTE1	GIE	ADCIE	TMCIE		TMAIE	WDTIE	E1IE	E0IE	000. 0000	000. 0000	*,*,*,*,*,*,*,*
26H	INTF1		ADCIF	TMCIF		TMAIF	WDTIF	E1IF	E0IF	.00. 0000	.00. 0000	-,*,*,-,*,*,*,*
29H	WREG				Working Register					xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2AH	BSRCN								BSR[0]	0	0	-,-,-,- -,-,-,*
2BH	STATUS				C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
2CH	PSTATUS	PD	TO	IDLEB	BOR		SKERR			000d d..	uduu d..	rw0,rw0,rw0,- -,rw0,-,-
2DH	LVDCN		LVDFG	LVD	LVDON		VLDX[3:0]			.000 0000	.000 0000	-,*,*,r,*,*,*,*
30H	PWRCN	ENVDDA	VDDAX[1:0]=11		ENACM					0xx0	0xx0	*,-,-,*,-,-,-,-
31H	MCKCN1	ADCS[2:0]			ADCCK	XTHSP	XTSP	ENXT	ENHAO	0000 0001	0000 0001	*,*,*,*,*,*,*,*
32H	MCKCN2			LSCK	HSCK	HSS[1:0]		CPUCK[1:0]		..00 0000	..00 0000	-,-,*,*,*,*,*,*
33H	MCKCN3	LCDS[2:0]				PERCK	BZS[2:0]			000. 0000	000. 0000	*,*,*,-,*,*,*,*
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte			0	0	0	0		xxxx 0000	uuuu 0000	r,r,r,r r0,r0,r0,r0
3CH	ADCCN1	ENADC		ENCHP	PGAGN[1:0]		ADGN[2:0]			0.00 0000	0.00 0000	*,-,*,*,*,*,*,*
3DH	ADCCN2			INBUF=0	VRBUF=0	VREGN	DCSET[2:0]			..xx 0000	..xx 0000	-,-,*,*,*,*,*,*
3EH	ADCCN3	OSR[2:0]					OSR[3]			000. ..0.	000. ..0.	*,*,*,-,-,*,-,-
3FH	AINET1	INH[2:0]=XX0 or XX1(AI2 or AI0)			INL[2:0]=0XX or 1XX(AI1 or VSS)			INIS		xx00 xx0x	xx00 xx0x	-,-,*,*,-,-,*,-
40H	AINET2	VRH[1:0]=X0 or X1(AI2 or ACM)		INX[1:0]		VRL[1:0]=11(VSS)				xx00 xx0x	xx00 xx0x	-,-,*,*,-,-,*,*
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,*,w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
46H	TMCCN	ENTMC	TMCCK[1:0]			TMCS1[2:0]			TMCS0[1:0]		0000 0000	0000 0000	*,*,*,*,*,*,*,*
47H	PRC	TimerC programmable register								1111 1111	1111 1111	*,*,*,*,*,*,*,*
48H	TMCR	TimerC register								0000 0000	0000 0000	r,r,r,r r,r,r,r
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]						0000	0000	*,*,*,*,-,-,-,-
51H	PWMR	PWM MSB Byte register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	LCDBI[1:0]=10			0000 0xxx	0000 0xxx	*,*,*,*,*,-,-,-
53H	LCDCN2	LCDBL	LCDMX[1:0]=11							0xxx xxxx	0xxx xxxx	-,-,-,-,*,-,-,-
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5AH	LCD6	Segment SEG14@[3:0] and SEG15@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5BH	LCD7	Segment SEG16@[3:0] and SEG17@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5CH	LCD8	Segment SEG18@[3:0] and SEG19@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5DH	LCD9	Segment SEG20@[3:0] and SEG21@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,* r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000	0000	*,*,*,*,-,-,-,-
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		 0000	 0000	-,-,-,-,*,*,*,*
72H	PT1M2		PM1.7[0]							.0..	.0..	-,*,-,- -,-,-,-
74H	PT2					PT2.3	PT2.2	PT2.1	PT2.0	 xxxx	.... uuuu	-,-,-,-,*,*,*,*
75H	TRISC2					TC2.3	TC2.2	TC2.1	TC2.0	 0000	 0000	-,-,-,-,*,*,*,*
77H	PT2PU					PU2.3	PU2.2	PU2.1	PU2.0	 0000	 0000	-,-,-,-,*,*,*,*
78H	PT2M1			PM2.2[1]	PM2.2[0]					..00	..00	-,-,*,*,-,-,-,-
80H ~ FFH	GPR0	General Purpose Register as 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
100H~17FH	GPR1	General Purpose Register as 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

Table 5-1(a) HY11P33 Register List

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W
									"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1			
									"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition			
195H	BIECTRL					VPP_HIGH		BIEWR	BIERD	1000 d000	1000 d000	-,-,-,- *,r0,*,*
197H	BIEPTRL	0	0	BIE_ADDR[5:0]						0000 0000	0000 0000	w0,w0,*,* *,*,*,*
198H	BIEDH	BIE_DATA[15:8]								xxxx xxxx	xxxx xxxx	*,*,*,* *,*,*,*
199H	BIEDL	BIE_DATA[7:0]								xxxx xxxx	xxxx xxxx	*,*,*,* *,*,*,*

Table 5-1(b) HY11P33 Register List (Continued)

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V$_{DD}$ to V$_{SS}$ . . . . **−0.2 V to 4.0 V**

Voltage applied to any pin . . . . **−0.2 V to V$_{DD}$ + 0.3 V**

Voltage applied to RST/VPP pin . . . . **−0.2 V to 6.9 V**

Voltage applied to TST/PT1.3 pin . . . . **−0.2 V to V$_{DD}$ + 1 V**

Diode current at any device terminal . . . . **±2 mA**

Storage temperature, Tstg: (unprogrammed device) . . . . **−55℃ to 150℃**

(programmed device) . . . . **−40℃ to 85℃**

Total power dissipation. **0.5w**

Maximum output current sink by any PORT1 to PORT2 I/O pin. **25mA**

6.1 Recommended Operating Conditions

T$_A$ = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter			Test Conditions		Min.	Typ.	Max.	unit
V$_{DD}$	Supply Voltage			All digital peripherals and CPU		2.2		3.6	V
				Analog peripherals		2.4		3.6	
V$_{SS}$	Supply Voltage					0		0	
XT	External Oscillator Frequency	Watch crystal		V$_{DD}$ = 2.2V, ENXT[0]=1	XTSP[0]=0, XTHSP[0]=0		32.768K		Hz
		Ceramic resonator			XTSP[0]=1, XTHSP[0]=0	450K		8M	
		Crystal			XTSP[0]=1, XTHSP[0]=0	1M		8M	

6.2   Internal RC Oscillator

$T_A = 25°C, V_{DD} = 3.0V$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.6	2.0	2.4	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz
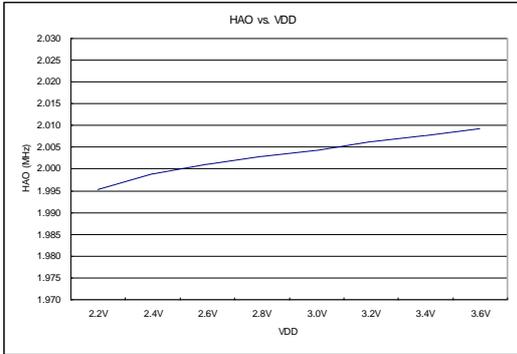
Figure 6.2-1 HAO vs. VDD
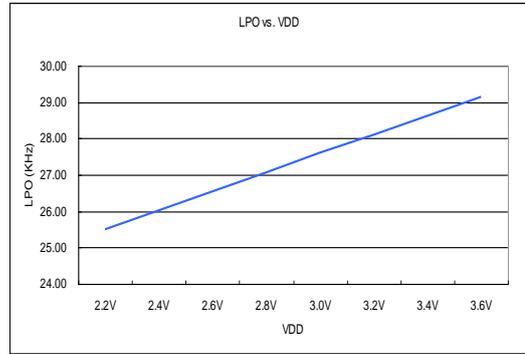
Figure 6.2-2 LPO vs. VDD
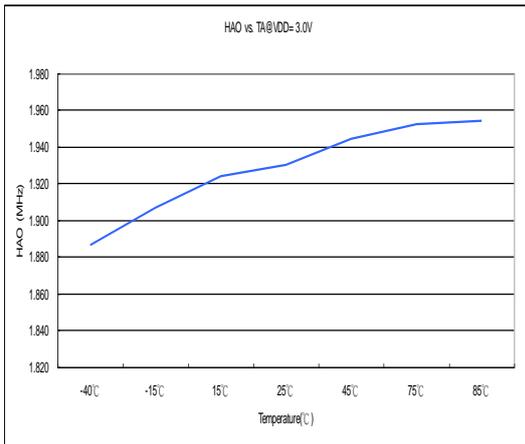
Figure 6.2-3 HAO vs. Temperature
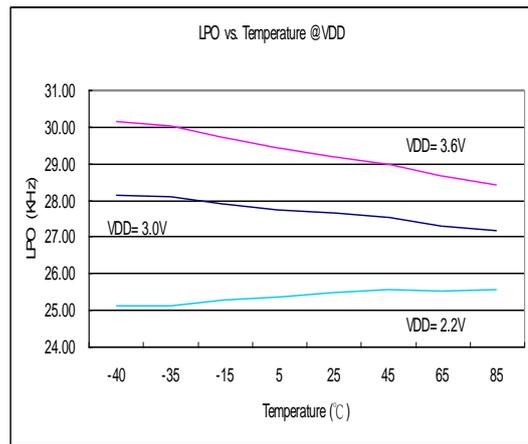
Figure 6.2-4 LPO vs. Temperature

6.3 Supply Current into VDD excluding Peripherals Current

$T_A = 25℃, V_{DD} = 3.0V, OSC\_LPO = 28KHz,$ unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1.2	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.32	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.18	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.
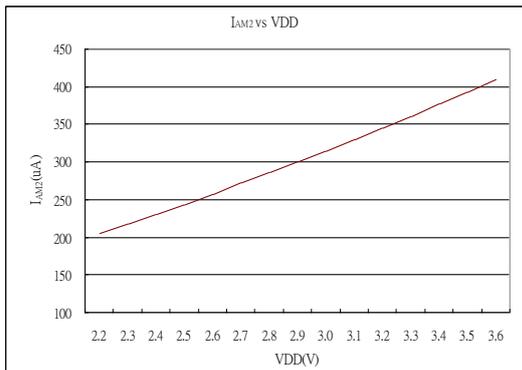
Figure 6.3-1 I_{AM2} vs. VDD
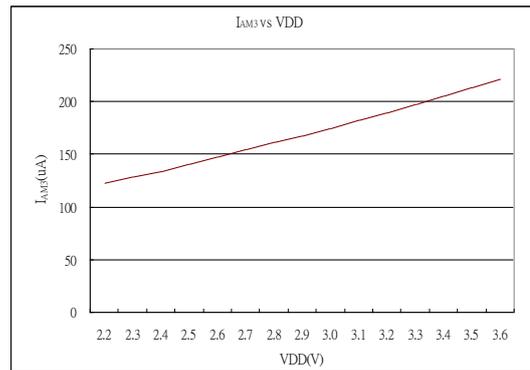
Figure 6.3-2 I_{AM3} vs. VDD
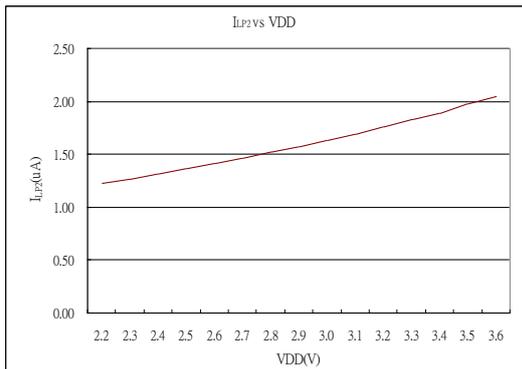
Figure 6.3-3 I_{LP2} vs. VDD
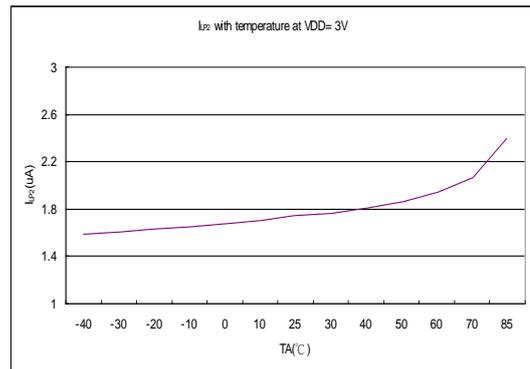
Figure 6.3-4 I_{LP2} vs. Temperature
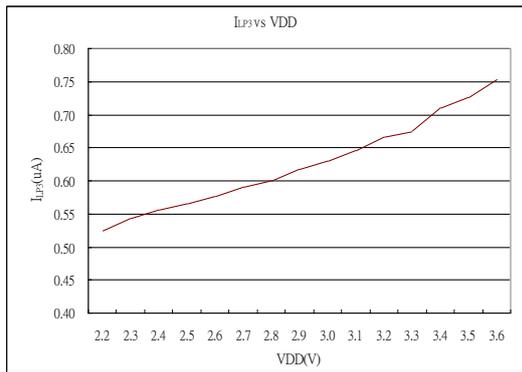
Figure 6.3-5 I_{LP3} vs. VDD
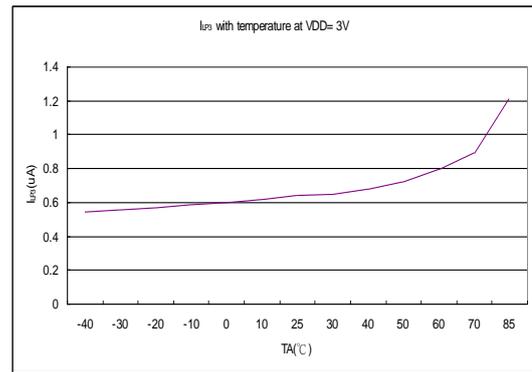
Figure 6.3-6I_{LP3} vs. Temperature

6.4 Port1~2

$T_A = 25℃, V_{DD} = 3.0V$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	
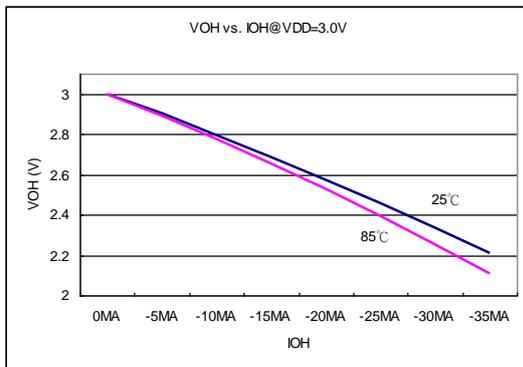
Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V
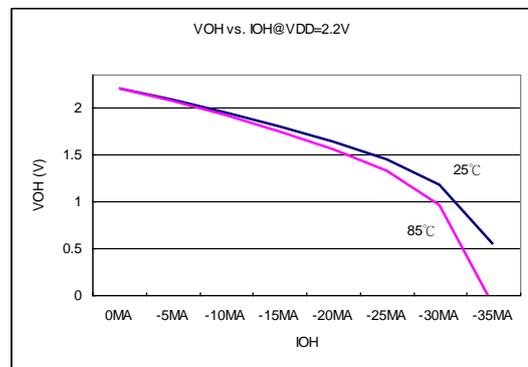
Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V
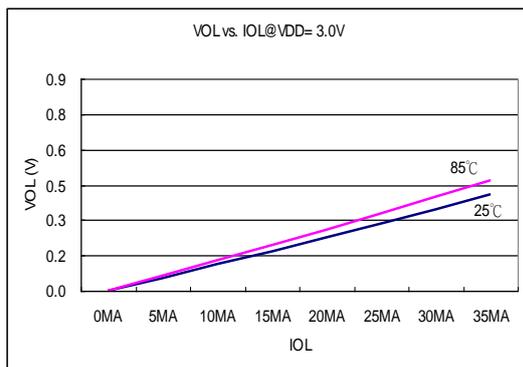
Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V
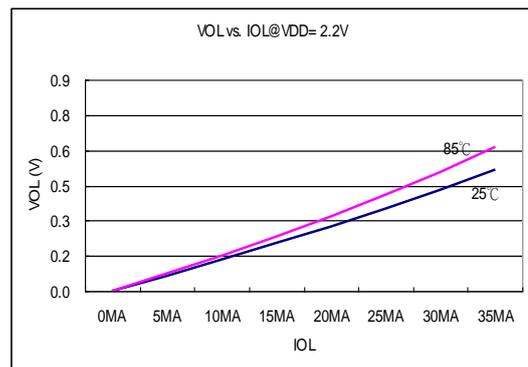
Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5 Reset(Brownout, External RST pin, Low Voltage Detect)

$T_A = 25°C, V_{DD} = 3.0V$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	$T_A = -40°C \sim 85 °C$		100		ppm/°C
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin
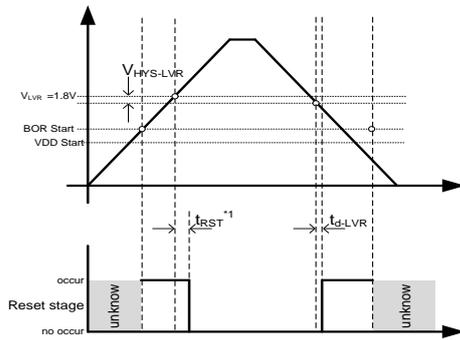
Figure 6.5-1 BOR Reset diagram
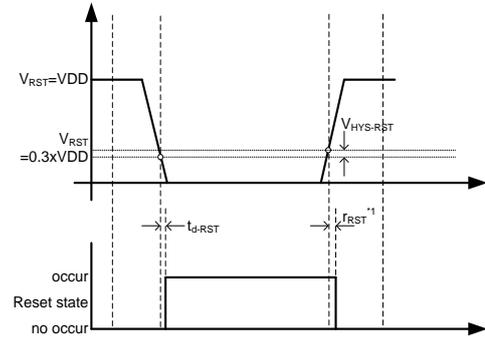
Figure 6.5-2 RST Reset diagram

[*1] r$_{RST}$：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).
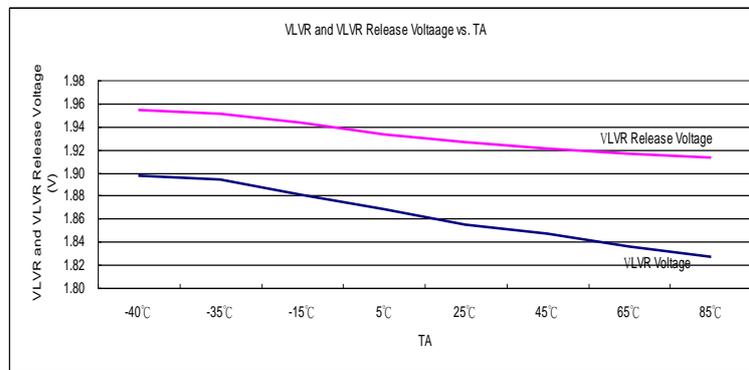
Figure 6.5-3 LVR vs. Temperature

6.6 Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧ VDDA+0.25V	VDDAX [1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX [1:0]=11b		250		mV
	Temperature drift	VDDAX [1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1,	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift	I_L = 10uA			100		uV/V

VDDA：Adjust Voltage Regulator

ACM：Analog Common Mode Voltage
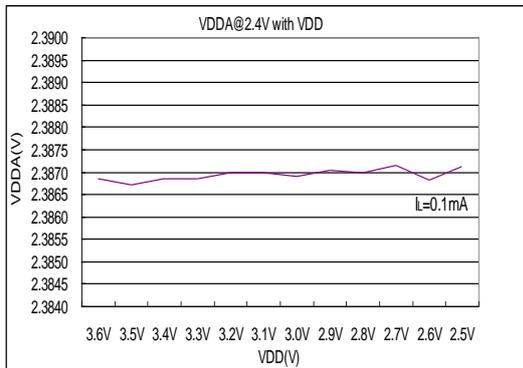
Figure 6.6-1 VDDA I_L=0.1mA vs. VDD
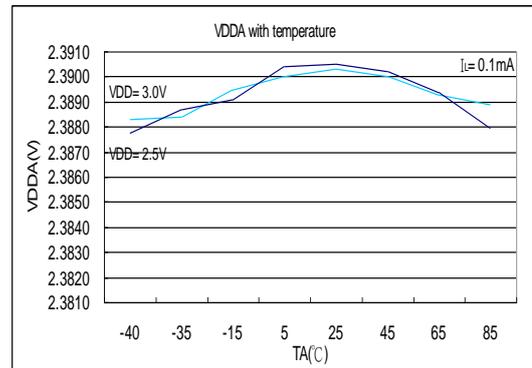
Figure 6.6-2 VDDA I_L=0.1mA vs. Temperature
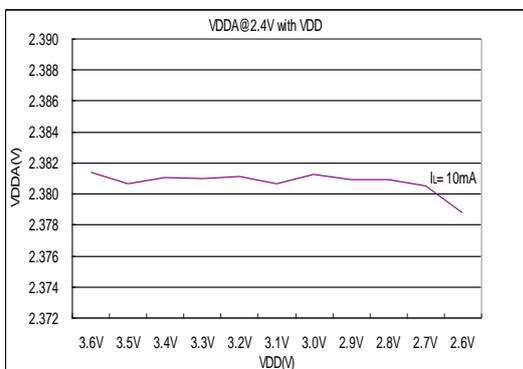
Figure 6.6-3 VDDA I_L=10mA vs. VDD
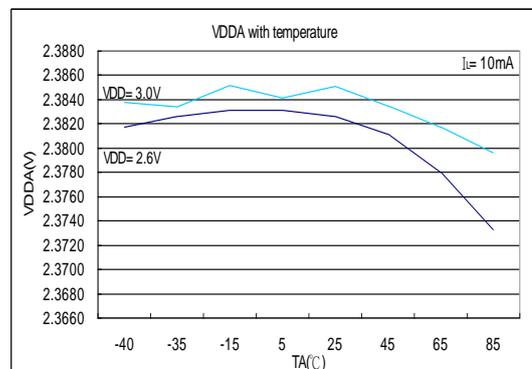
Figure 6.6-4 VDDA I_L=10mA vs. Temperature
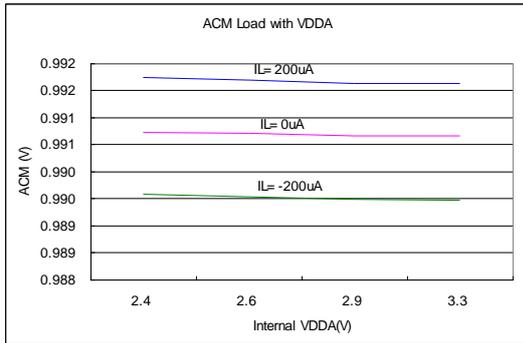
Figure 6.6-5 ACM Load vs. VDDA
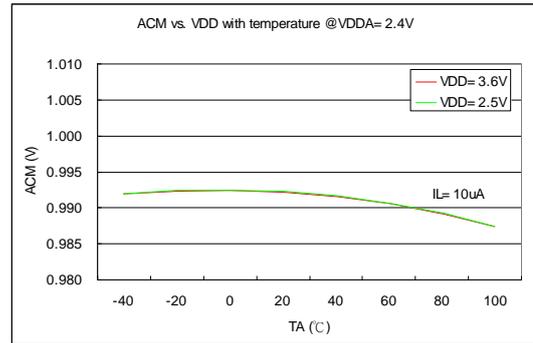

Figure 6.6-6 ACM vs. Temperature

6.7 LCD

$T_A = 25°C, V_{DD} = 3.0V, C_{VLCD} = 4.7uF$, unless otherwise noted.

| Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	V_{DD} = 2.2V		10		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =4.7uF	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
			VLCDX[1:0]=00b	2.97	3.3	3.63	
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ
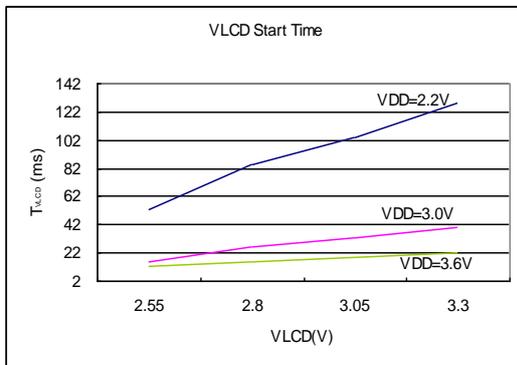
Figure 6.7-1 LCD Start Time
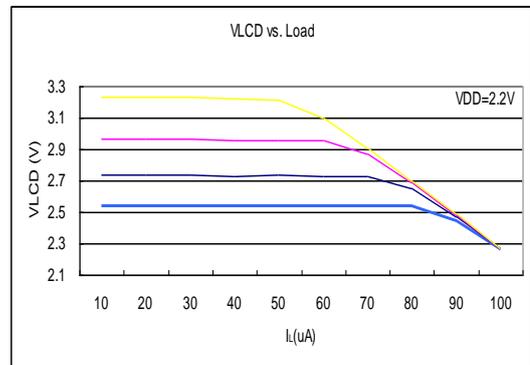
Figure 6.7-2 VLCD vs. I_L @VDD=2.2V
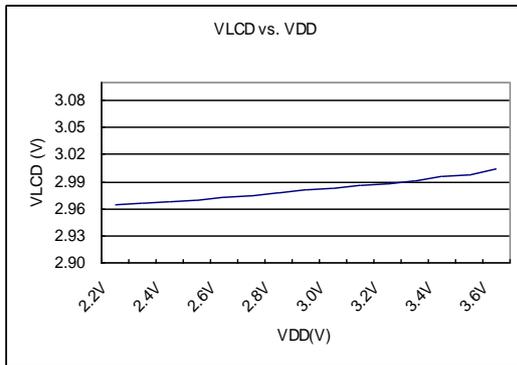

Figure 6.7-3 VLCD vs. VDD
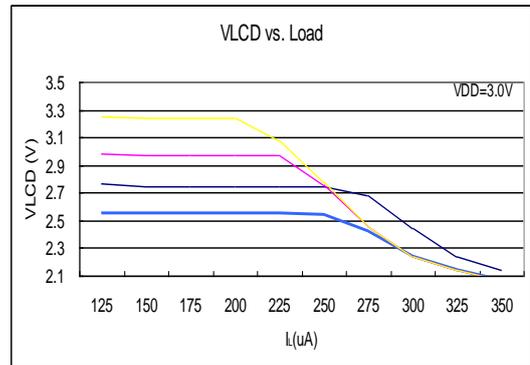

Figure 6.7-4 VLCD vs. I_L @VDD=3.0V

6.8 SD18, Power Supply and Recommended Operating Conditions

$T_A = 25℃, V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted$

Sym.	Parameter	Test Conditions			Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0			2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK				25	250	300	KHz
	Over Sample Ratio, OSR				128 [*1]		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz			120		uA

*1, OSR=128, setting by ADCCN3[OSR3] bit.

  OSR[3:0]=1010b, OSR=128; OSR[3:0]=0xxx, OSR=256 ~ 32768

  OSR[3:0]=1xxxb can't set by user

6.8.1 PGA, Power Supply and Recommended Operating Conditions

$T_A = 25℃, V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted$

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<11>			320		uA
G_{PGA}	Gain temperature drift	$T_A = -40℃~ 85℃$	GAIN=128		15		ppm/℃

6.8.2 SD18, PerformanceⅡ(fSD18=250KHz)

$T_A = 25℃, V_{DD} = 3.0V, VDDA=2.9V, V_{VR}=1.0V, GAIN=1$ without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions			Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV				±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV						
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b			19			Bits
G_{SD18}	Temperature drift **Gain 1~x16 (INBUF[0]=0b,)**	INBUF[0]=0b,VRBUF[0]=0b		$T_A = -40℃~ 85℃$		10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short		Gain=2			1	%FSR
	Offset error temperature drift with chopper without PGA			GAIN=1		2		uV/℃
				GAIN=2		1		
				GAIN=4		0.5		
				GAIN=16		0.15		

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

| Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
CM$_{SD18}$	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16		75		
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI}=1.2V,	GAIN=1 PGA=off		75		dB
			GAIN=16 PGA=8				
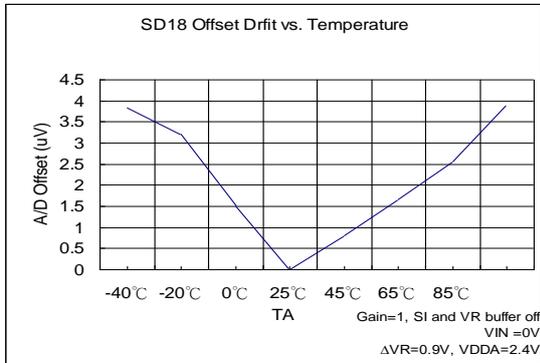

Figure 6.8-1(a) SD18 Offset Temperature Drift
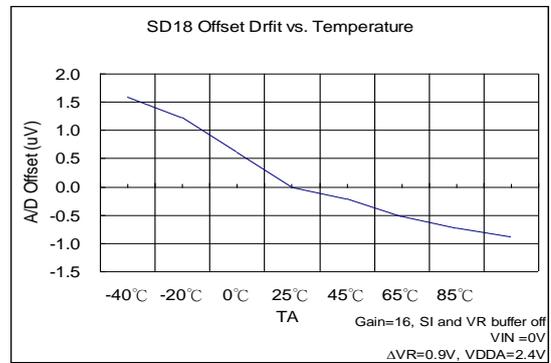
Figure 6.8-1(b) SD18 Offset Temperature Drift
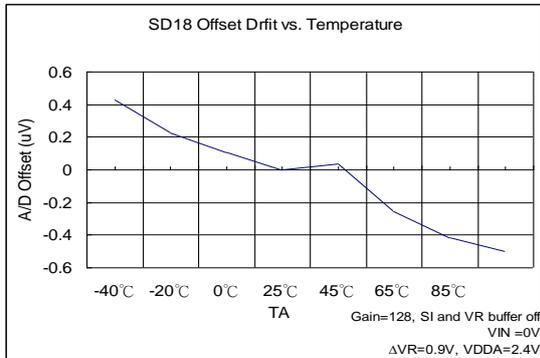
Figure 6.8-1(c) SD18 Offset Temperature Drift
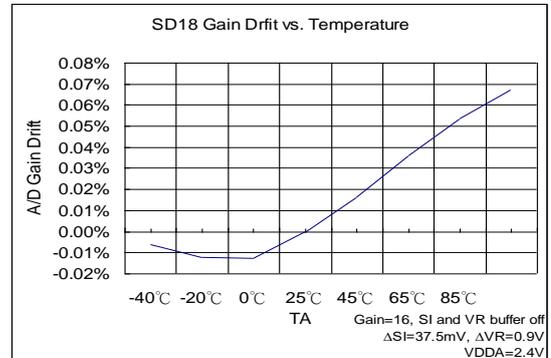

Figure 6.8-2(a) SD18 Gain Drift with Temperature
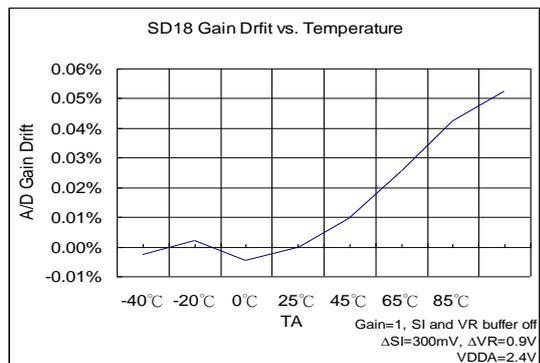

Figure 6.8-2(b) SD18 Gain Drift with Temperature
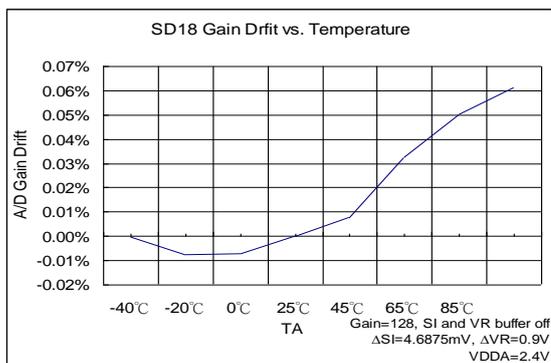
Figure 6.8-2(c) SD18 Gain Drift with Temperature

6.8.3 SD18 Noise Performance

$T_A = 25℃, V_{DD} = 3.0V$, VDDA=2.4V,unless otherwise noted

HY11P33 provides important input noise specification that aims at SD18. Table 6.8-3(a) and Table 6.8-3(b) lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

Max. Vin(mV) =0.9*VREF [(1)]	OSR					128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					1953	977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN									
±2400	0.25	=	1	×	0.25	14.43	16.07	17.20	17.86	18.29	18.66	18.98	19.13	19.30
±2160	0.5	=	1	×	0.5	14.34	16.05	17.13	17.84	18.26	18.62	18.90	19.13	19.27
±1080	1	=	1	×	1	14.38	16.06	17.11	17.72	18.13	18.53	18.88	19.05	19.22
±540	2	=	1	×	2	14.40	15.98	16.96	17.59	18.01	18.45	18.79	19.01	19.17
±270	4	=	1	×	4	14.39	15.88	16.82	17.39	17.85	18.28	18.65	18.95	19.13
±135	8	=	1	×	8	14.27	15.75	16.58	17.15	17.60	18.04	18.45	18.78	19.02
±68	16	=	1	×	16	14.14	15.51	16.18	16.73	17.21	17.70	18.15	18.52	18.83
±8	128	=	8	×	16	13.04	13.83	14.32	14.87	15.38	15.86	16.36	16.84	17.28

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.8-3(a) SD18 ENOB Table

Max. Vin(mV) =0.9*VREF	OSR					128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					1953	977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN									
±2400	0.25	=	1	×	0.25	362.92	139.77	64.33	40.65	30.04	23.35	18.70	16.75	14.92
±2160	0.5	=	1	×	0.5	193.22	70.82	33.83	20.60	15.37	12.00	9.86	8.38	7.61
±1080	1	=	1	×	1	94.14	35.38	17.16	11.17	8.40	6.34	5.01	4.44	3.92
±540	2	=	1	×	2	46.23	18.59	9.48	6.13	4.57	3.35	2.66	2.28	2.05
±270	4	=	1	×	4	23.37	9.98	5.20	3.51	2.54	1.89	1.46	1.18	1.05
±135	8	=	1	×	8	12.66	5.47	3.06	2.06	1.51	1.11	0.84	0.67	0.56
±68	16	=	1	×	16	6.93	3.23	2.02	1.38	0.99	0.70	0.51	0.40	0.32
±8	128	=	8	×	16	1.86	1.29	0.91	0.63	0.44	0.32	0.22	0.16	0.12

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V

Table 6.8-3(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \frac{\ln\left(\dfrac{FSR}{RMS\ Noise}\right)}{\ln(2)}$$

$$RMS\ Noise = \frac{\left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right)}{2^{23}}$$

Where FSR (Full - Scale Range) = $2 \times VREF / Gain$.

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$
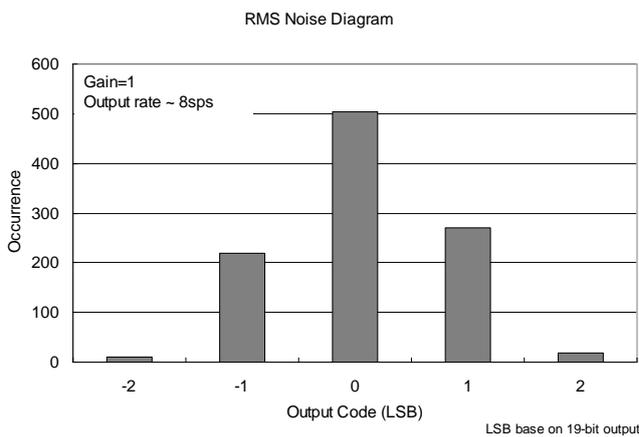
Figure 6.8-3(a) RMS Noise Diagram
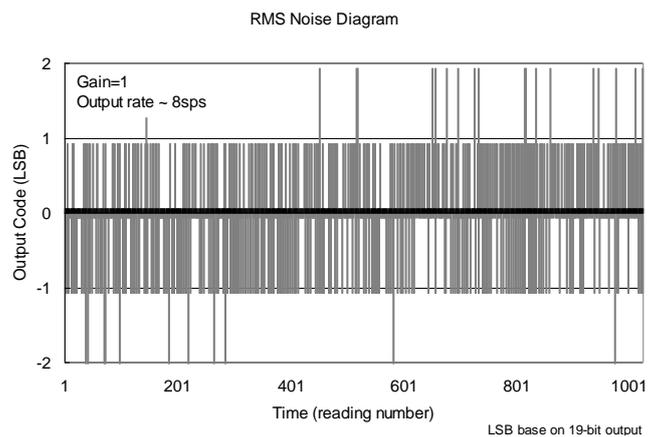

Figure 6.8-3(b) Output Code Diagram
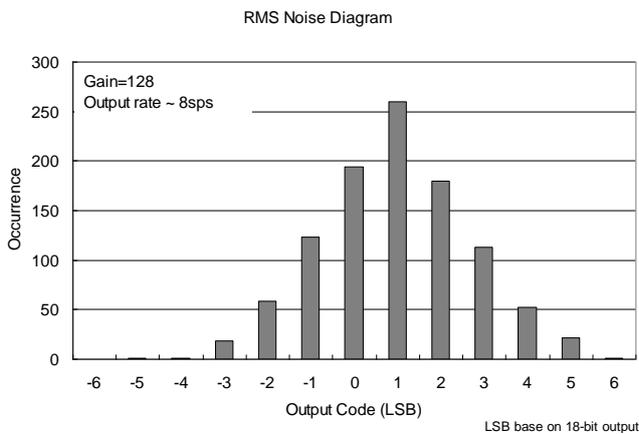
Figure 6.8-3(c) RMS Noise Diagram
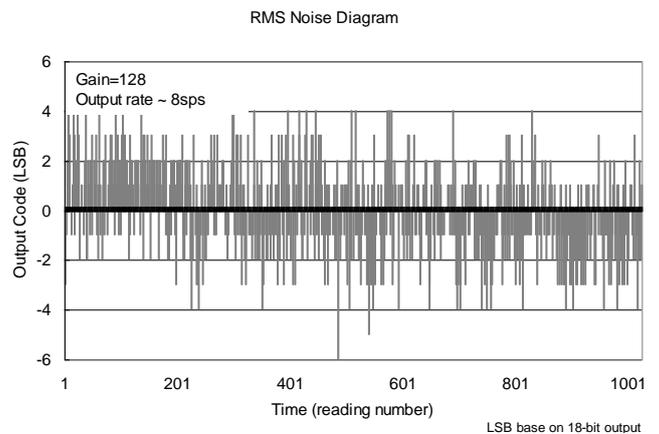
Figure 6.8-3(d) Output Code Diagram

6.9 Built-In EPROM (BIE)

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage			6.0	6.5	V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY11P33-D000	Die	-	D	000	000	-	200	Green[4]	-
HY11P33-L064	LQFP	64	L	064	000	Tray	250	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code** (Blank Code/ Standard/ Customized Programming Code)

    Ex: You request blank code in die package and the model No. is HY11P33.
        The device No. will be HY11P33-D000.

    Ex: Your customized programming code is 008, the model No. is HY11P33 and you
        require die shipment. The device No. will be HY11P33-D000-008.

    Ex: You request blank code in LQFP 64 package and the model No. is HY11P33.
        The device No. will be HY11P33-L064.
        And please clearly indicate the shipment packing type when placing orders.

    Ex: Your customized programming code is 009, the model No. is HY11P33 and you
        require products in LQFP 64 package.
        The device No. will be HY11P33-L064-009.
        And please clearly indicate the shipment packing type when placing orders.

[2] **Code:**

    "001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

    The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] **Green (RoHS & no Cl/Br):**

    HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%

8. Package Information

8.1 LQFP64(L064)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
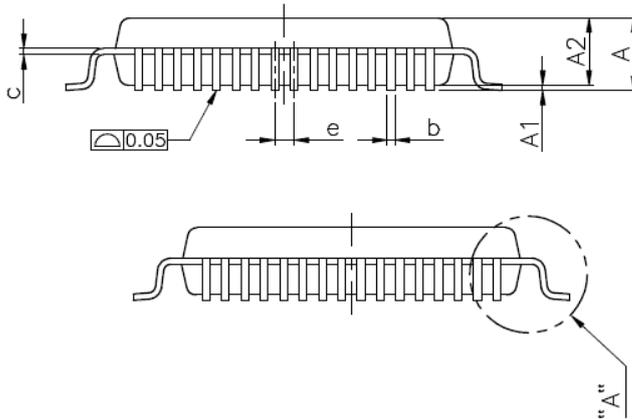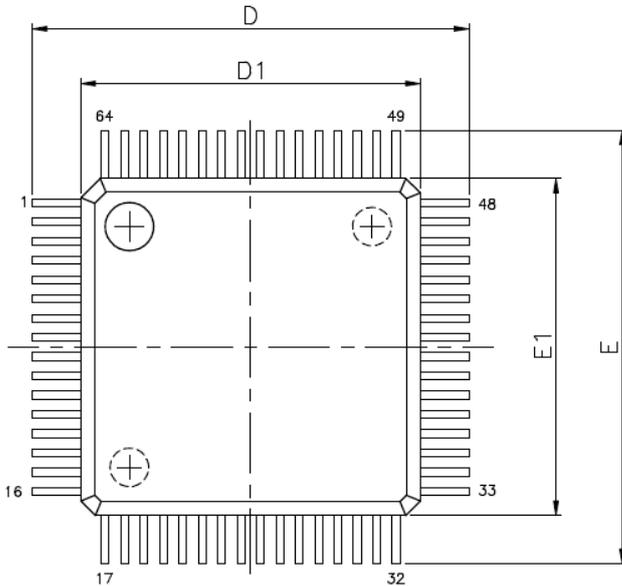
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)
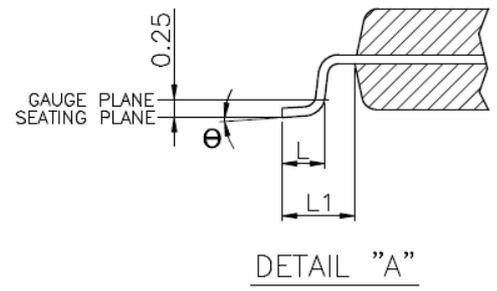
JEDEC MS-026 compliant

9. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V01	ALL	First Edition
V02	ALL	Entire content revision
V04	5	Revise product features
	12	Revise SD18 Network

Preliminary
DS-HY11P33-V04_EN
Page 32