HYCON TECHNOLOGY

HY11P52/HY11P52B

Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x12 LCD Driver
18-Bit ΣΔADC

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1. Features

- 8-bit RISC, 46 instructions included.
- Operating voltage range: 2.2V to 3.6V, operation temperature range: -40℃~85℃.
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
  - Active Mode 300uA@2MHz
  - Standby Mode 3uA@28KHz
  - Sleep Mode 1uA
- 2K Word OTP (One Time Programmable) Type Program Memory, 128 Byte Data Memory
- Brownout detector and Watch dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D)
  - Built-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x，10 input signal gain selection
  - Built-in Input zero point adjustment can increase measurement range according to different application.
  - Diverse data output rate. Max. 1.95KSPS
- 1.0V internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function
- Analog voltage source, VDDA equips with 10mA low dropout regulator function, fast start function.
- 4x12 LCD Drive
  - 1/4 Duty、1/3 Bias
  - Built-in Charge Pump regulated circuit, providing 4 LCD Bias voltage
- 8-bit Timer A
- Built-In EPROM (BIE), 3.05V low voltage programming control circuit (HY11P52); 2.75V low voltage programming control circuit (HY11P52B).
- PFM control circuit
- Support 6 stack level

2. Pin Definition

2.1. Pin Diagram LQFP48

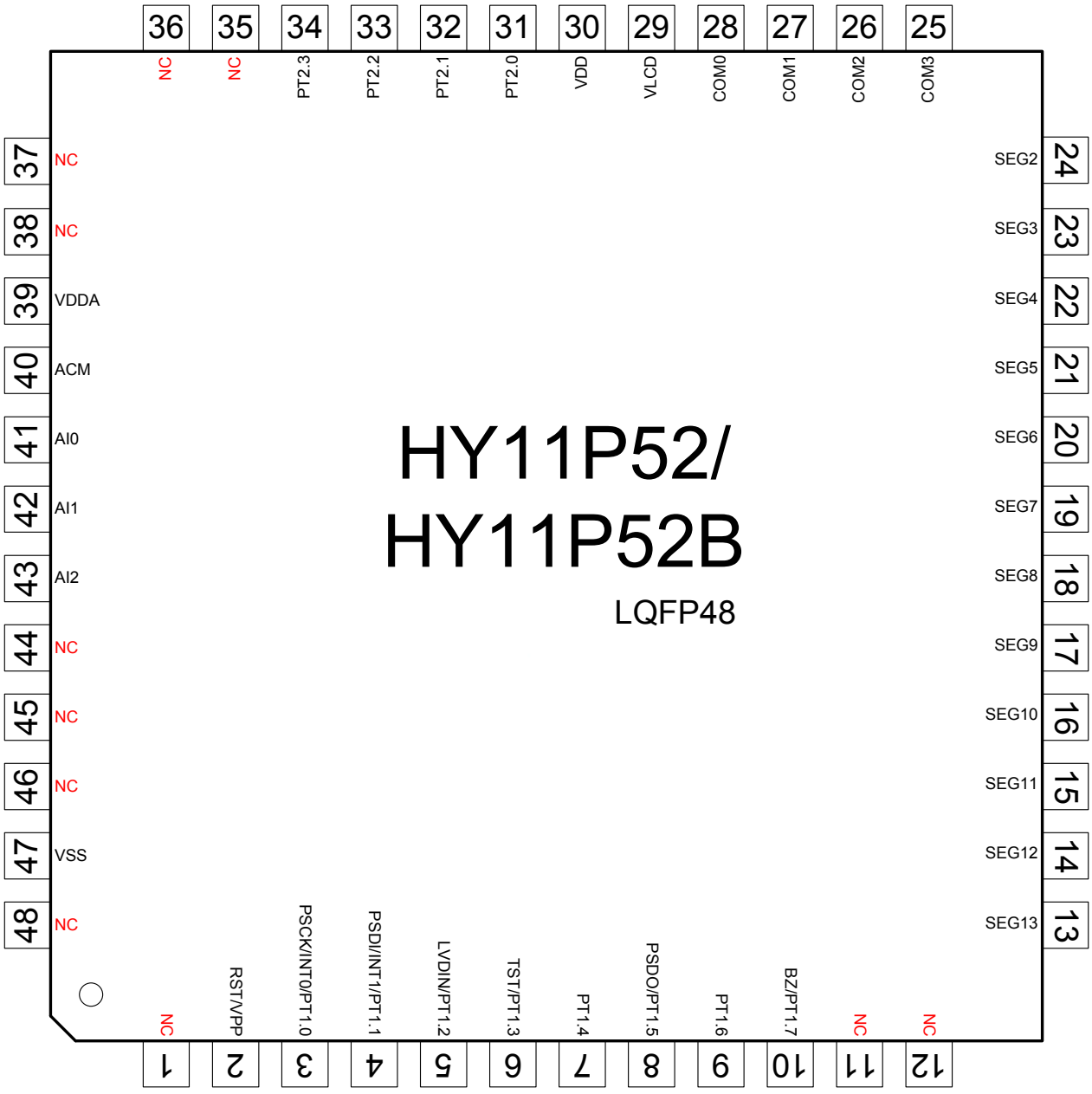


Figure 2-1 HY11P52/HY11P52B LQFP48 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 is not configured as external pin button, it can help to enhance the anti-interference ability.

2.2. I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

NO.	Pin Name	Pin Characteristic		Description
		Type	Buffer	
1	NC	-	-	Unused
2	RST/VPP			
	RST	I	S	Reset IC
	VPP	P	P	EPROM read/write voltage source
3	PT1.0/INT0/PSCK			
	PT1.0	I	S	Digital input
	INT0	I	S	Interrupt input INT0
	PSCK	I	S	SCK port of OTP read/write
4	PT1.1/INT1/PSDI			
	PT1.1	I	S	Digital input
	INT1	I	S	Interrupt input INT1
	PSDI	I	S	SDI port of OTP read/write
5	PT1.2/LVDIN/FB			
	PT1.2	I	S	Digital input
	LVDIN	A	A	LVD external signal input port
	FB	A	A	Feedback control port of back light constant current
6	PT1.3/TST			
	PT1.3	I	S	Digital input
	TST	I	S	Test Mode input pin (invalid)
7	PT1.4	I/O	S	Digital I/O
8	PT1.5/PSDO			
	PT1.5	I/O	S	Digital I/O
	PSDO	O	C	SDO port of OTP read/write
9	PT1.6/FS			
	PT1.6	I/O	S	Digital I/O
	FS	O	C	Output port of back light constant current control
10	PT1.7/BZ			
	PT1.7	I/O	S	Digital I/O
	BZ	O	C	Buzzer output
11	NC	-	-	Unused
12	NC	-	-	Unused

13	SEG13	O	A	LCD Segment Output
14	SEG12	O	A	LCD Segment Output
15	SEG11	O	A	LCD Segment Output
16	SEG10	O	A	LCD Segment Output
17	SEG9	O	A	LCD Segment Output
18	SEG8	O	A	LCD Segment Output
19	SEG7	O	A	LCD Segment Output
20	SEG6	O	A	LCD Segment Output
21	SEG5	O	A	LCD Segment Output
22	SEG4	O	A	LCD Segment Output
23	SEG3	O	A	LCD Segment Output
24	SEG2	O	A	LCD Segment Output
25	COM3	O	A	LCD COM Output
26	COM2	O	A	LCD COM Output
27	COM1	O	A	LCD COM Output
28	COM0	O	A	LCD COM Output
29	VLCD	P	P	LCD voltage source
30	VDD	P	P	IC operation voltage source
31	PT2.0	I/O	S	Digital I/O
32	PT2.1	I/O	S	Digital I/O
33	PT2.2	I/O	C	Digital I/O
34	PT2.3	I/O	S	Digital I/O
35	NC	-	-	Unused
36	NC	-	-	Unused
37	NC	-	-	Unused
38	NC	-	-	Unused
39	VDDA	P	P	Regulator output, analog circuit voltage souce
40	ACM	P	P	Internal analog circuit common ground pin
41	AI0	A	A	Analog input channel
42	AI1	A	A	Analog input channel
43	AI2	A	A	Analog input channel
44	NC	-	-	Unused
45	NC	-	-	Unused
46	NC	-	-	Unused
47	VSS	P	P	IC operation voltage source ground

				pin
48	NC	-	-	Unused

Table 2-1 Pin Definition and Function Description

3. Application Circuit

3.1. Bridge Sensor I (HY11P52)

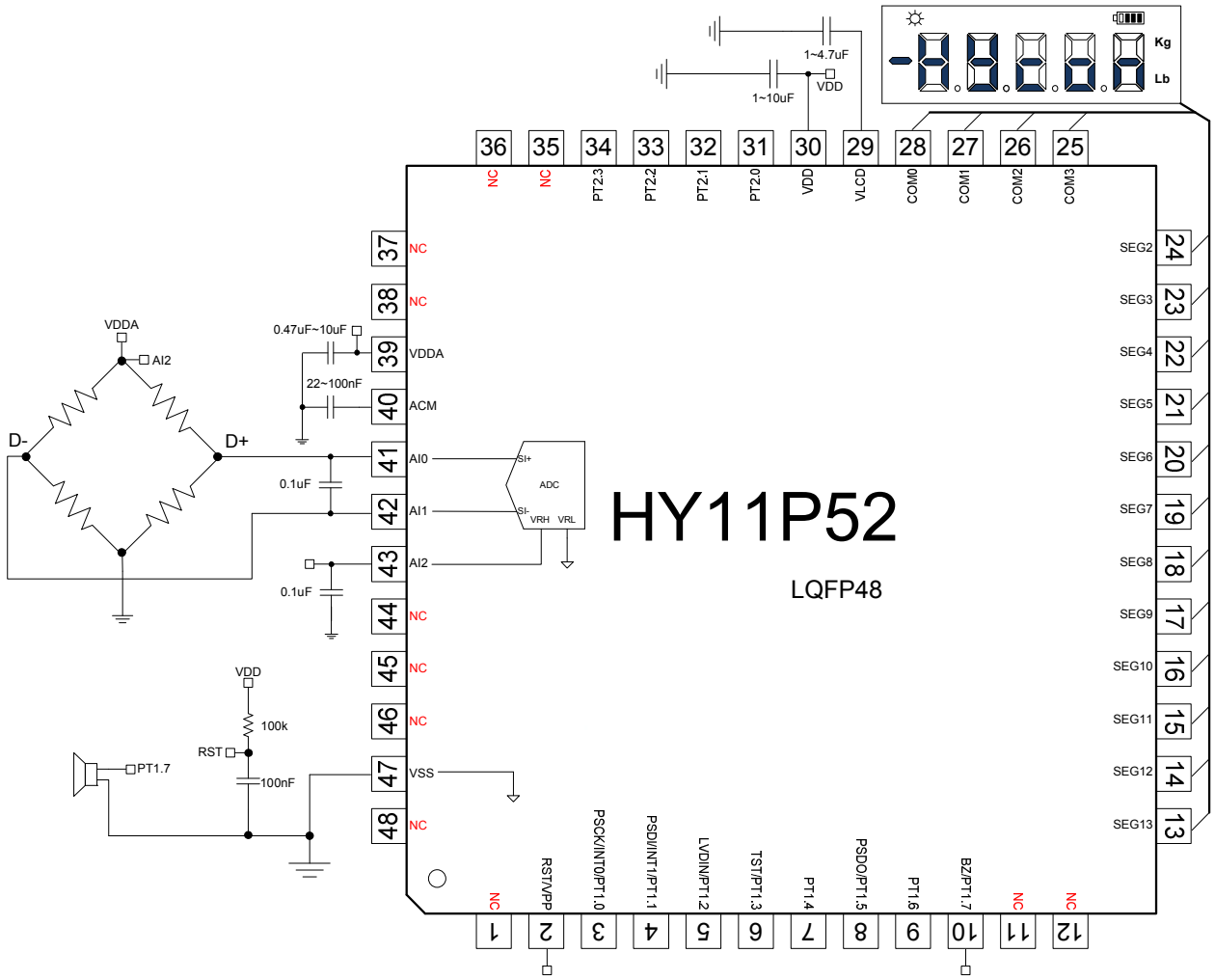


Figure 3-1 Bridge Sensor Application Circuit

Note 1：DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

3.2. Bridge Sensor II (HY11P52B)

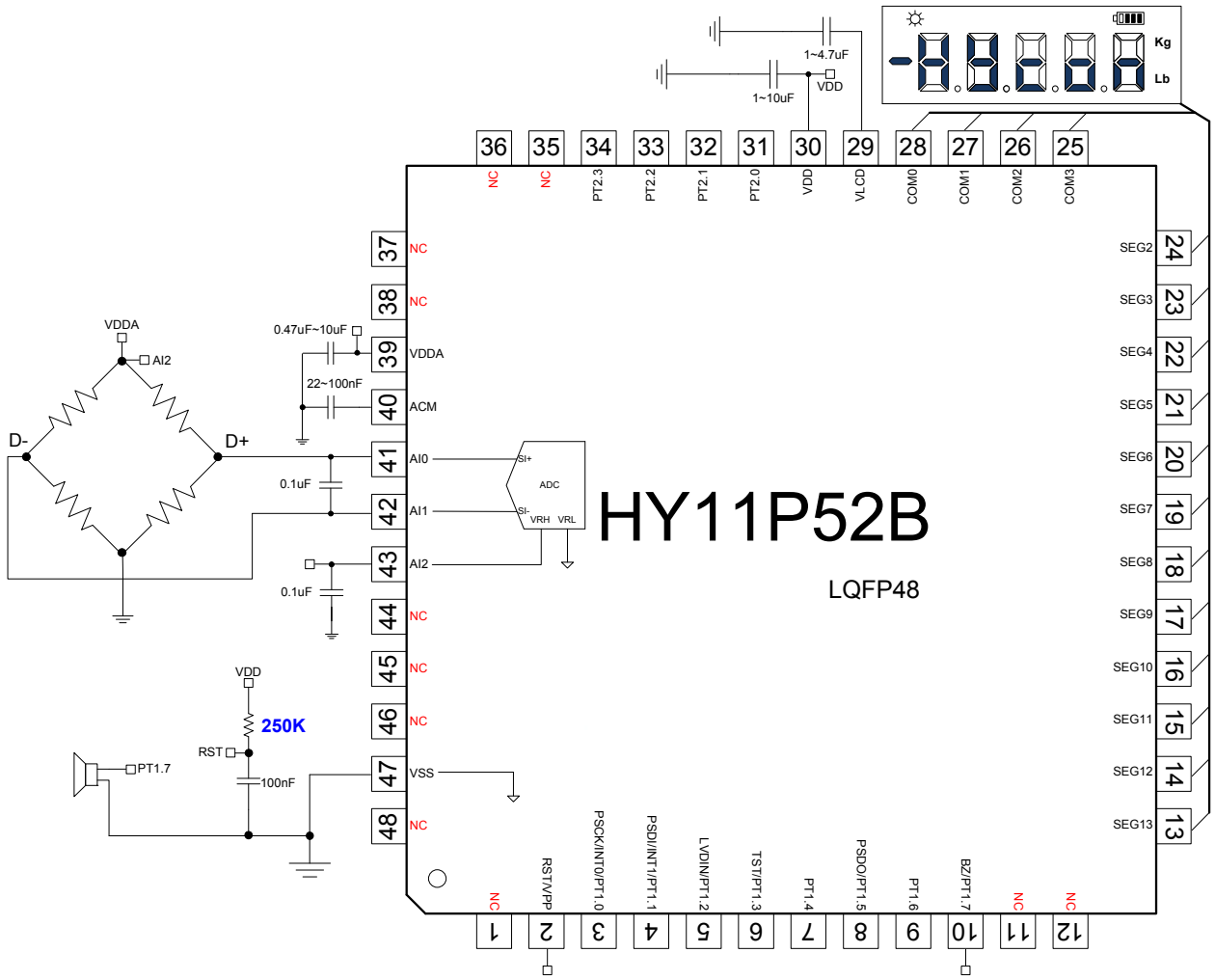


Figure 3-1 Bridge Sensor Application Circuit

Note 1：DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address.

Note 2：RST pin pull up resistor is enhanced by built-in 2.75V low programming voltage control function. The resistor value of HY11P52B is 250KΩ.

4. Function Outline

4.1. Internal Block Diagram

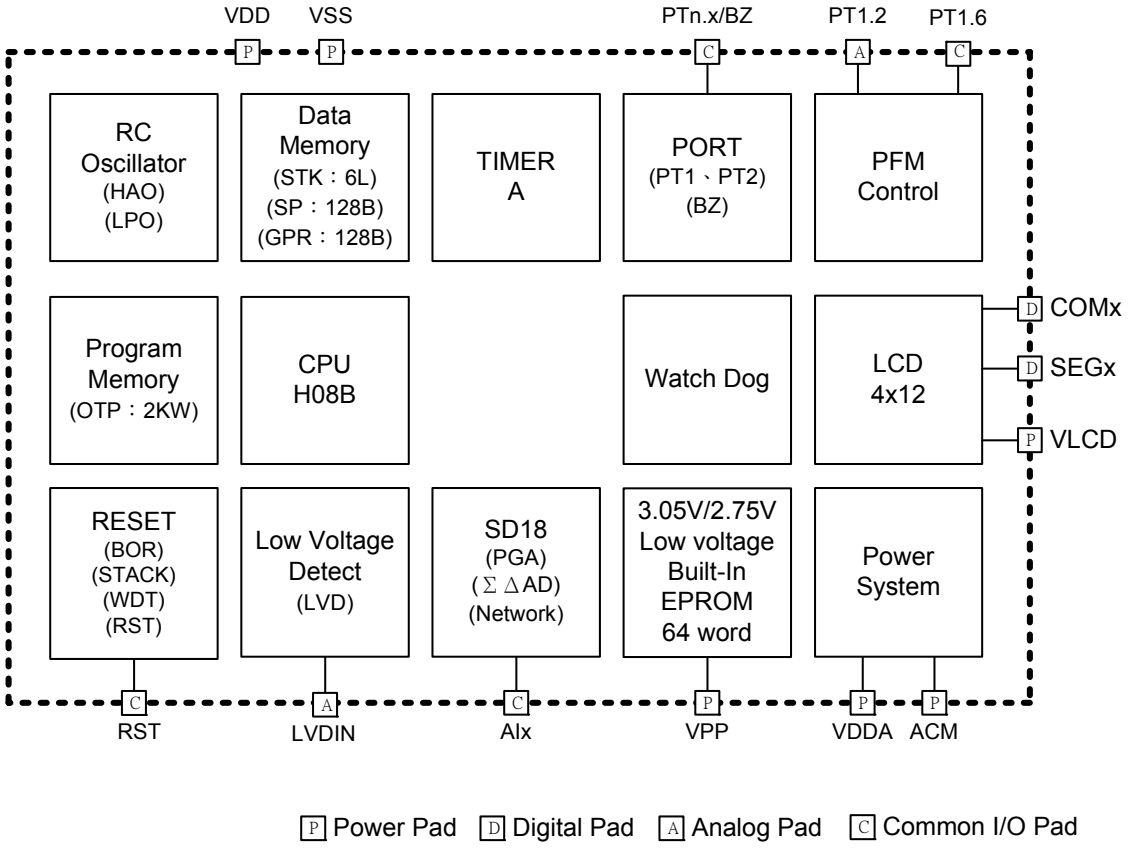


Figure 4-1 HY11P52/HY11P52B Internal Block Diagram

4.2. Related Description and Supporting Documents

IC Function Related Operating Instruction

DS-HY11P52	HY11P52/HY11P52B Datasheet
UG-HY11S14	HY11Pxx Series Users' Manual
APD-CORE003	H08B Instruction Description

Development Tool Related Operating Instruction

APD-HYIDE001	HY11xxx Series Development Tool Software Instruction Manual
APD-HYIDE002	HY11xxx Series Development Tool Hardware Instruction Manual
APD-OTP001	OTP Products Programming Pin Manual

Product Production Related Operating Instruction

APD-ICE001	HY11P52 Low voltage programming/look-up-table/PFM application note
APD-ICE003	HY11P52B Low voltage programming/look-up-table/PFM application note
APD-HYIDE004	HY1xxxx Series Production Line Specialized Programmer Manual
BDI-HY11P32	HY11P52 Individual Product Die Bonding Information

4.3. SD18 Network

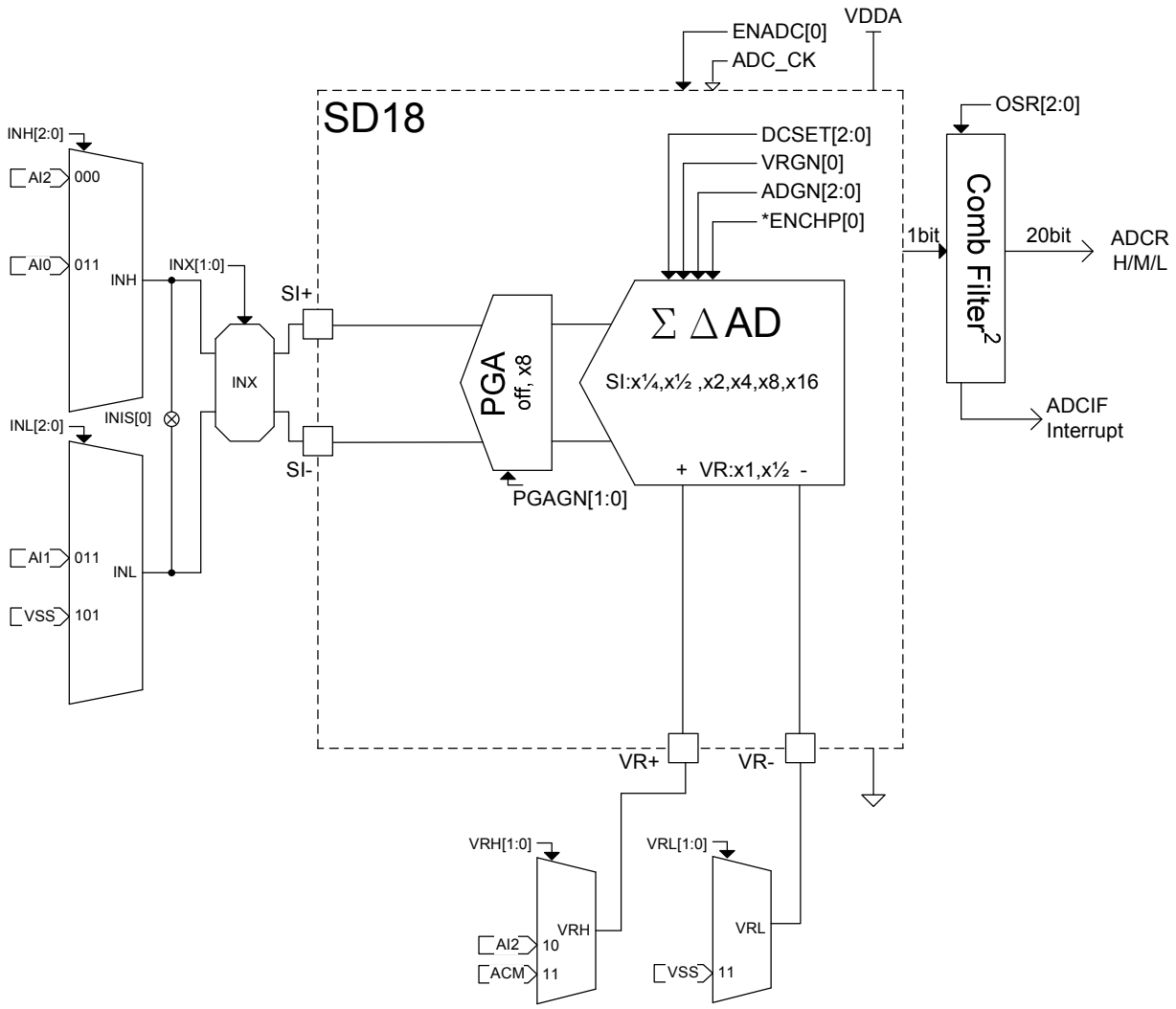


Figure 4-2 SD18 Network

5. Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV			STKPRT[2:0]			000. .000	000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH						PC[10]	PC[9]	PC[8]	.... .000	.... .000	-,-,-,- -,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1CH	BIECTRL					VPP_HIGH		BIEWR	BIERD	1000 d000	1000 d000	-,-,-,- *,r0,*,*
1DH	BIEPTRH	**BIESEL**					**BIE_ADDR[10:8]**			0000 0000	0000 0000	*,-,-,- -,*,*,*
1EH	BIEPTRL	**BIE_ADDR[7:6]**		BIE_ADDR[5:0]						0000 0000	0000 0000	*,*,*,*,*,*,*,*
1FH	BIEDH	BIE_DATA[15:8]								xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
20H	BIEDL	BIE_DATA[7:0]								xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
23H	INTE1	GIE	ADCIE			TMAIE	WDTIE	E1IE	E0IE	0000 0000	0000 0000	*,*,r0,r0 *,*,*,*
26H	INTF1		ADCIF			TMAIF	WDTIF	E1IF	E0IF	.000 0000	.000 0000	-,*,r0,r0 *,*,*,*
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2BH	STATUS				C				Z	xxxx xxxx	xxxx xxxx	-,-,-,* -,-,-,*
2CH	Pstatus	PD	TO	IDLEB	BOR					000d xxxx	000d xxxx	rw0,rw0,rw0,rw0 x,x,x,x
2DH	LVDCN		LVDFG	LVD	LVDON	**VLDX[3:0]**				x000 0000	x000 0000	x,*,r,r *,*,*,*
30H	PWRCN	ENVDDA	**VDDAX[1:0]=11**		ENACM			**ENLEDP**		0xx0 xx00	0xx0 xxuu	*,r,r,* -,-,*,*
31H	MCKCN1	ADCS[2:0]			ADCCK			ENXT=0	ENHAO	0000 0001	0000 0001	*,*,*,* r0,r0,r0,*
32H	MCKCN2			**LSCK=0**	**HSCK=0**	**HSS[1:0]=00**		CPUCK[1:0]		..00 0000	..00 0000	r0,r0,r0,r0 r0,r0,*,*
33H	MCKCN3	LCDS[2:0]				PERCK	BZS[2:0]			000. 0000	000. 0000	*,*,*,r0 *,*,*,*
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r0,r0,r0,r0
3CH	ADCCN1	ENADC		ENCHP	**PGAGN[1:0]=00 or 11**		ADGN[2:0]			0000 0000	0000 0000	*,r0,*,*,*,*,*,*
3DH	ADCCN2			INBUF=0	VRBUF=0	VREGN	DCSET[2:0]			0000 0000	0000 0000	r0,r0,r0,r0 *,*,*,*
3EH	ADCCN3	OSR[2:0]						**OSR[3]**		000x xx0x	000u uu0u	*,*,*,- -,-,*,-
3FH	AINET1	**INH[2:0]=XX0 or XX1(AI2 or AI0)**			**INL[2:0]=0XX or 1XX(AI1 or VSS)**			INIS		xx00 xx0x	xx00 xx0x	x,x,*,* x,x,*,x
40H	AINET2		**VRH[1:0]=X0 or X1(AI2 or ACM)**		INX[1:0]		**VRL[1:0]=11(VSS)**			xx00 0xxx	xx00 0xxx	x,x,*,* *,x,x,x
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,* w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	**LCDBI[1:0]=10**			0000 0xxx	0000 0xxx	*,*,*,* *,x,x,x
53H	LCDCN2	LCDBL	**LCDMX[1:0]=11**							0xxx xxxx	0xxx xxxx	*,x,x,x x,x,x,x
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD0								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD1								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD2								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD3								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD4								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD5								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,* r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000 0000	0000 0000	*,*,*,* r0,r0,r0,r0
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		0000 0000	0000 0000	r0,r0,r0,r0 *,*,*,*
72H	PT1M2		PM1.7[0]							0000 0000	0000 0000	r0,*,r0,r0 r0,r0,r0,r0
74H	PT2					PT2.3	PT2.2	PT2.1	PT2.0	 xxxx	.... uuuu	x,x,x,x *,*,*,*
75H	TRISC2					TC2.3	TC2.2	TC2.1	TC2.0	 0000	 0000	x,x,x,x *,*,*,*
77H	PT2PU					PU2.3	PU2.2	PU2.1	PU2.0	 0000	 0000	x,x,x,x *,*,*,*
80H ~ FFH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

Figure 5-1 HY11P52/HY1P52B Register List

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . . −0.2 V to 4.0 V

Voltage applied to any pin . . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.3 pin . . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT2 I/O Pin. 25mA

6.1 Recommended Operating Conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.4		3.6	
V_{SS}	Supply Voltage		0		0	

6.2 Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.6	2.0	2.4	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

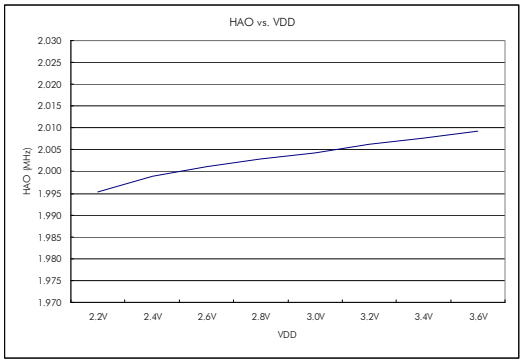


Figure 6.2-1 HAO vs. VDD

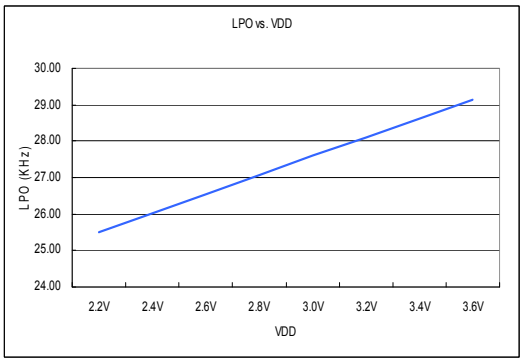


Figure 6.2-2 LPO vs. VDD

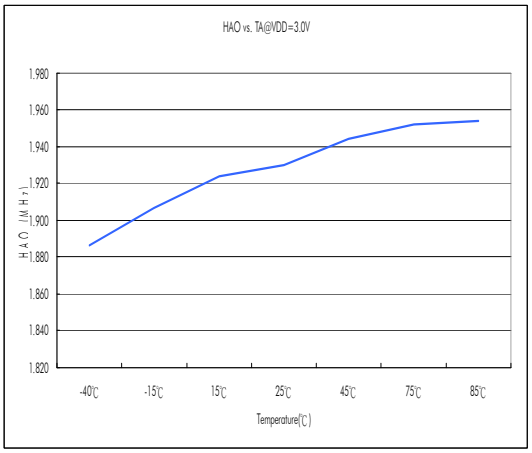


Figure 6.2-3 HAO vs. Temperature

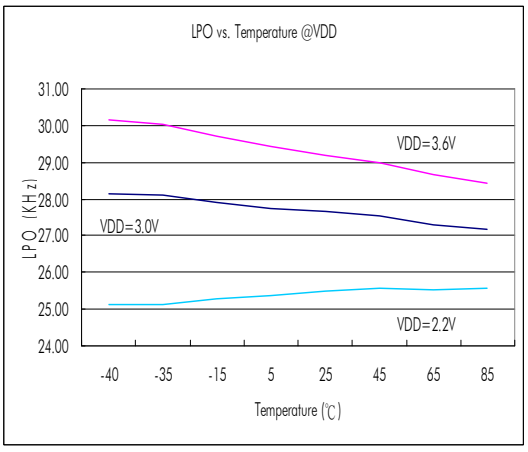


Figure 6.2-4 LPO vs. Temperature

6.3 Supply Current into VDD Excluding Peripherals Current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 28KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.28	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.165	0.3	mA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

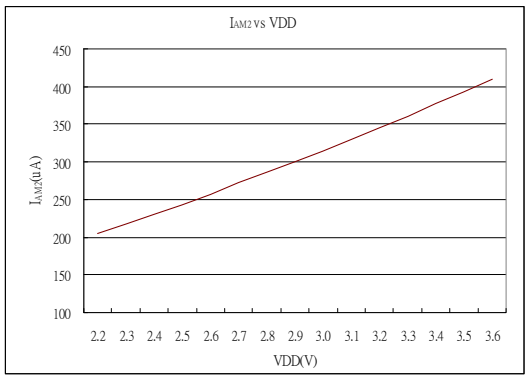


Figure 6.3-1 IAM2 vs. VDD

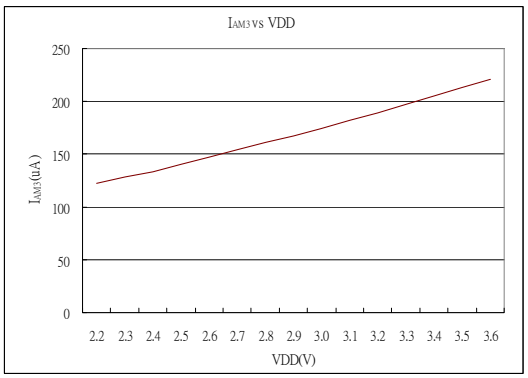


Figure 6.3-2 IAM3 vs. VDD

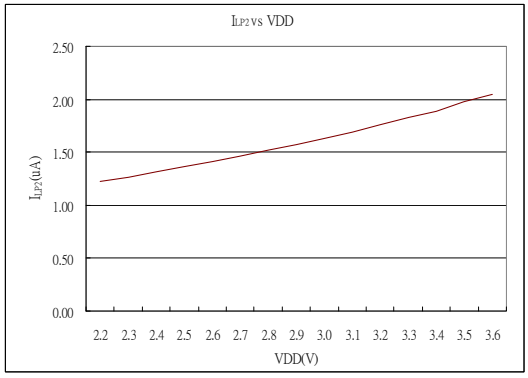


Figure 6.3-3 ILP2 vs. VDD

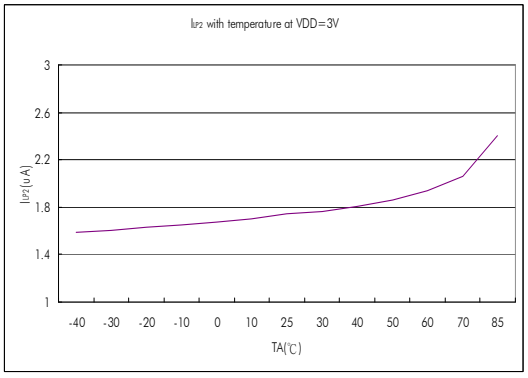


Figure 6.3-4 ILP2 vs. Temperature

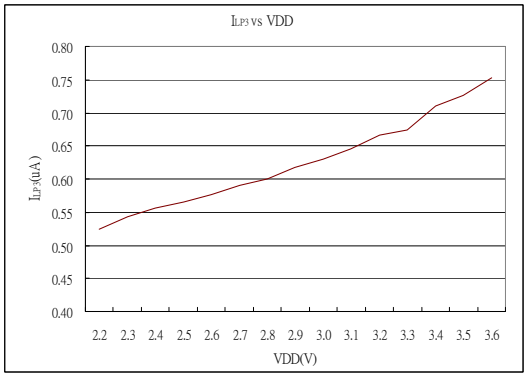


Figure 6.3-5 ILP3 vs. VDD

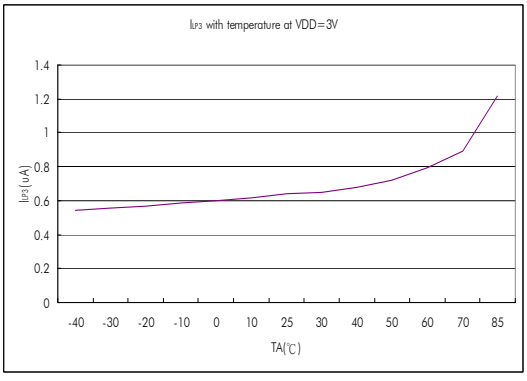


Figure 6.3-6ILP3 vs. Temperature

6.4 Port 1~2

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

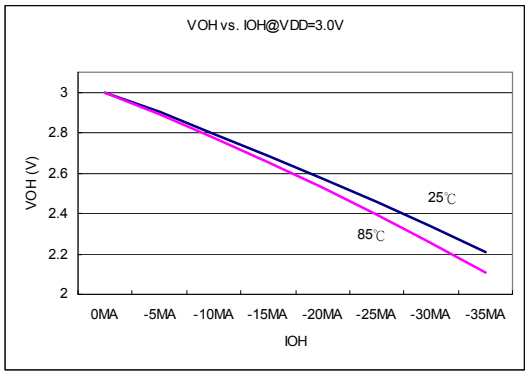


Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

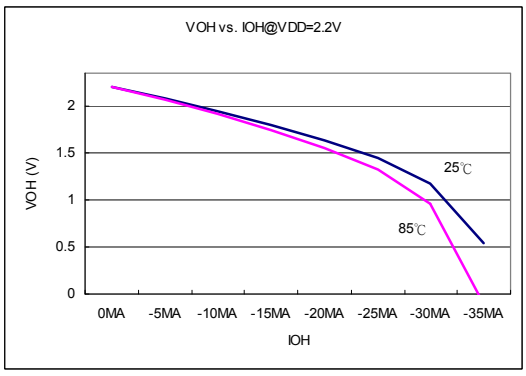


Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

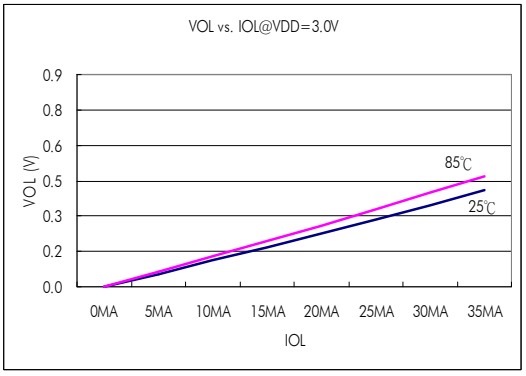


Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

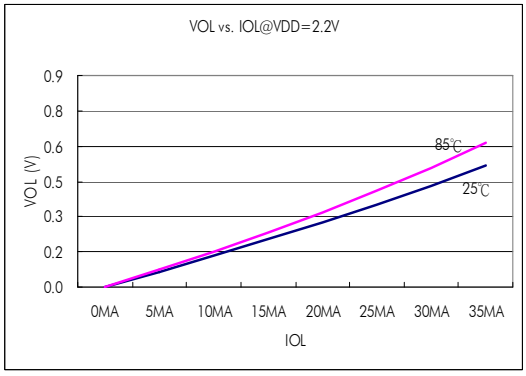


Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5 Reset (Brownout, External RST pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		100		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

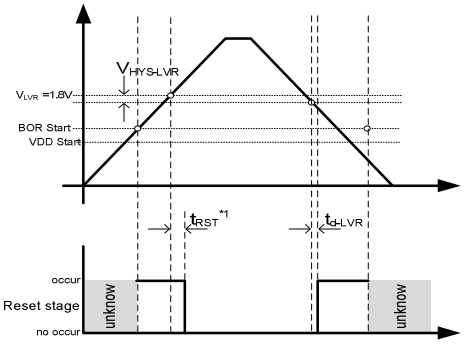


Figure 6.5-1 BOR Reset Diagram

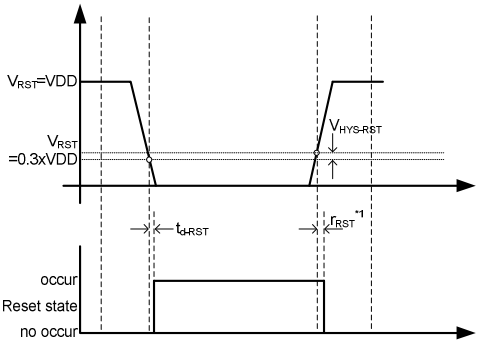


Figure 6.5-2 RST Reset Diagram

*1 r_{RST}：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14)

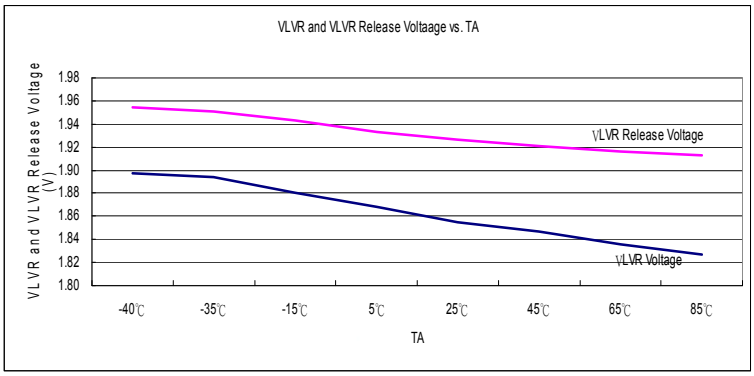


Figure 6.5-3 LVR vs. Temperature

6.6 Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.25V	VDDAX [1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX [1:0]=11b		250		mV
	Temperature drift	VDDAX [1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1,	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift	I_L = 10uA			100		uV/V

VDDA：Adjust Voltage Regulator

ACM：Analog Common Mode Voltage

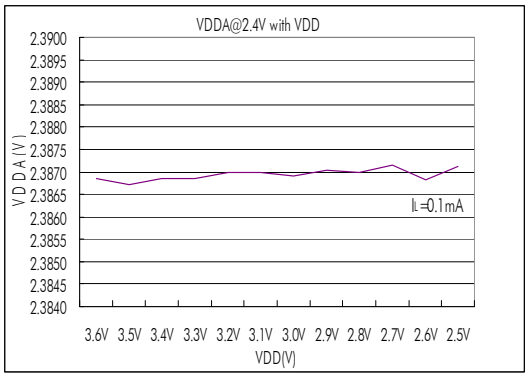


Figure 6.6-1 VDDA IL=0.1mA vs. VDD

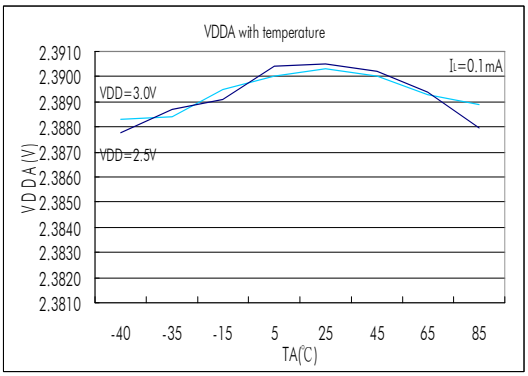


Figure 6.6-2 VDDA IL=0.1mA vs. Temperature

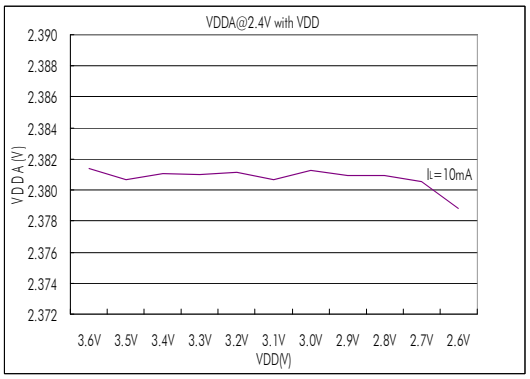


Figure 6.6-3 VDDA IL=10mA vs. VDD

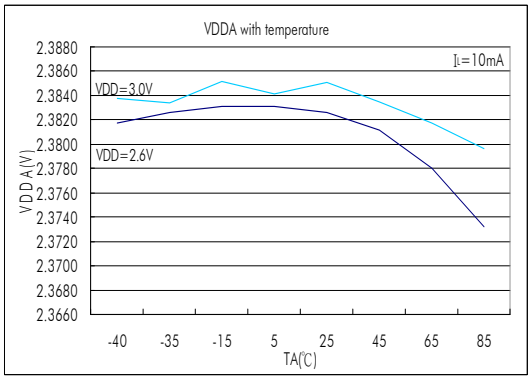


Figure 6.6-4 VDDA IL=10mA vs. Temperature

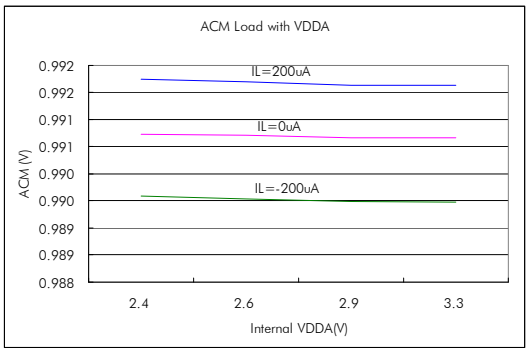


Figure 6.6-5 ACM Load vs. VDDA

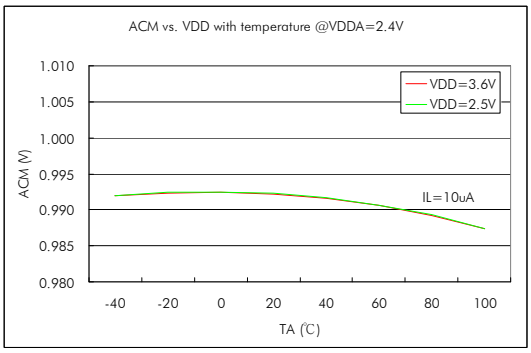


Figure 6.6-6 ACM vs. Temperature

6.7 LCD

T_A = 25℃,V_{DD} = 3.0V, C_{VLCD} =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on) (HY11P52)	LCDPR[0]=1	V_{DD} = 2.2V		10		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =4.7uF	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
			VLCDX[1:0]=00b	2.97	3.3	3.63	
Z_{LCD}	Output impedance with LCD buffer (HY11P52)	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ
I_{LCD1}	Operation supply current without output buffer.(all segment turn on) (HY11P52B)	LCDPR[0]=1	V_{DD} = 2.2V		8		uA
			V_{DD} = 3.0V				
Z_{LCD1}	Output impedance with LCD buffer (HY11P52B)	f_{LCD} =128Hz,VLCD=3.05V			20		kΩ

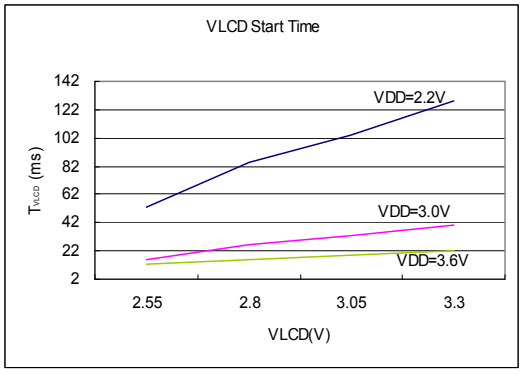


Figure 6.7-1 LCD start time

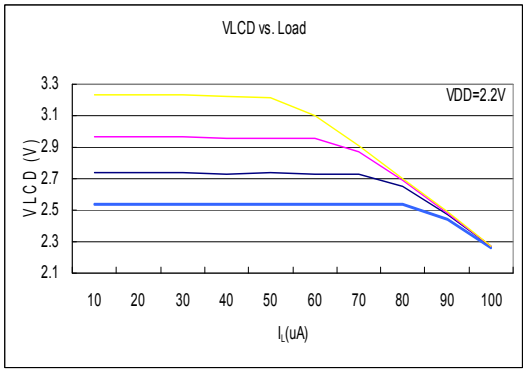


Figure 6.7-2 VLCD vs. I_L @VDD=2.2V

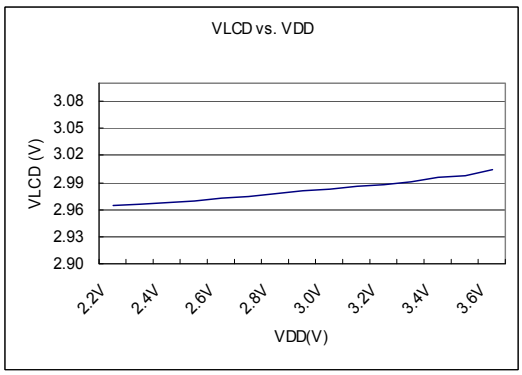


Figure 6.7-3 VLCD vs. VDD

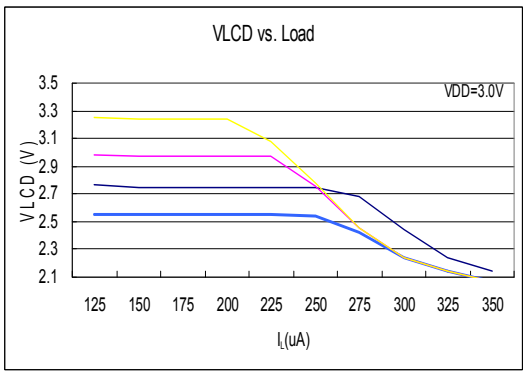


Figure 6.7-4 VLCD vs. I_L @VDD=3.0V

6.8 SD18, Power Supply and Recommended Operating Conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			128 *1		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1	GAIN =4, ADC_CK=250KHz		120		uA
*1, OSR=128, setting by ADCCN3[OSR3] bit. OSR[3:0]=1010b, OSR=128; OSR[3:0]=0xxx, OSR=256 ~ 32768 OSR[3:0]=1xxxb can't set by user							

6.8.1 PGA, Power Supply and Recommended Operating Conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<11>			320		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		15		ppm/℃

6.8.2 SD18, Performance II (fSD18=250KHz)

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions			Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV				±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV						
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b			19			Bits
G_{SD18}	Temperature drift **Gain 1~x16** **(INBUF[0]=0b,)**			T_A = -40℃~ 85℃		10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short		Gain=2			1	%FSR
	Offset error temperature drift with chopper without PGA			GAIN=1		2		uV/℃
				GAIN=2		1		
				GAIN=4		0.5		
				GAIN=16		0.15		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V,		V_{SI}=0V,		90		dB

		V_{VR}=1.0V,without PGA	GAIN=1		
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16	75	
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16 PGA=8		

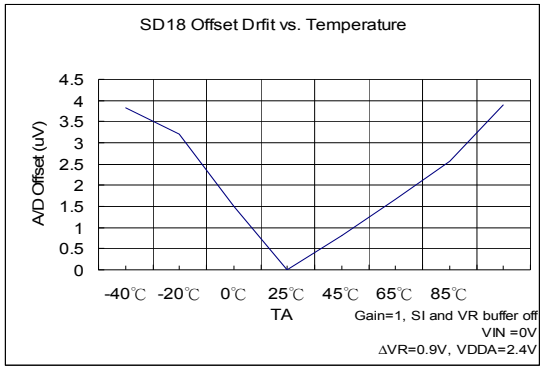


Figure 6.8-1(a) SD18 Offset Temperature Drift

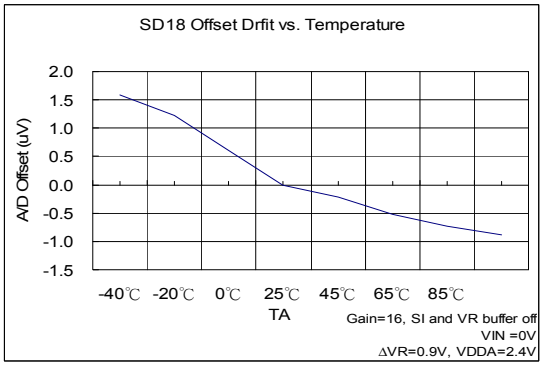


Figure 6.8-1(b) SD18 Offset Temperature Drift

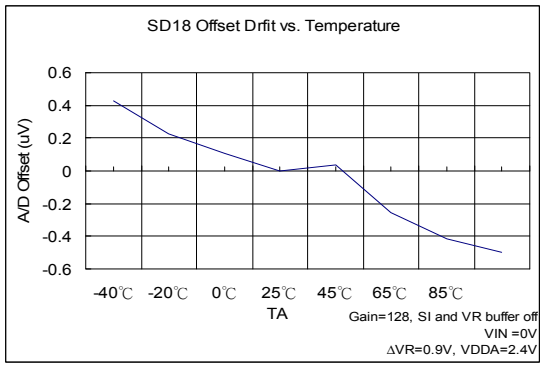


Figure 6.8-1(c) SD18 Offset Temperature Drift

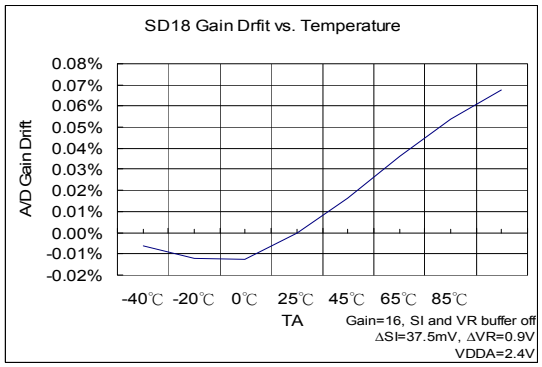


Figure 6.8-2(a) SD18 Gain Drift with Temperature

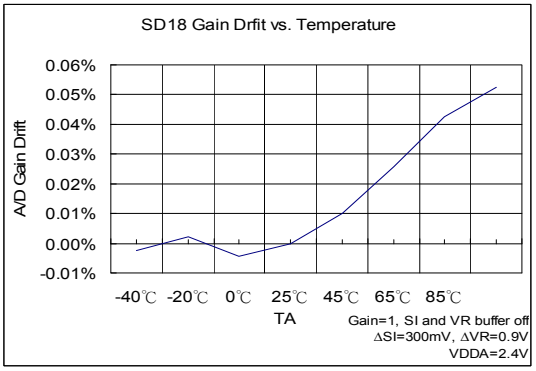


Figure 6.8-2(b) SD18 Gain Drift with Temperature

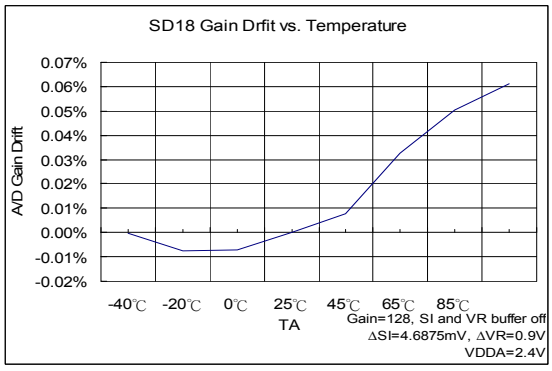


Figure 6.8-2(c) SD18 Gain Drift with Temperature

6.8.3 SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P52/HY11P52B provides important input noise specification that aims at SD18. Table 6.8-4(a) and Table 6.8-4(b) lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF (1)	OSR					128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					1953	977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN									
±2400	0.25	=	1	×	0.25	14.43	16.07	17.20	17.86	18.29	18.66	18.98	19.13	19.30
±2160	0.5	=	1	×	0.5	14.34	16.05	17.13	17.84	18.26	18.62	18.90	19.13	19.27
±1080	1	=	1	×	1	14.38	16.06	17.11	17.72	18.13	18.53	18.88	19.05	19.22
±540	2	=	1	×	2	14.40	15.98	16.96	17.59	18.01	18.45	18.79	19.01	19.17
±270	4	=	1	×	4	14.39	15.88	16.82	17.39	17.85	18.28	18.65	18.95	19.13
±135	8	=	1	×	8	14.27	15.75	16.58	17.15	17.60	18.04	18.45	18.78	19.02
±68	16	=	1	×	16	14.14	15.51	16.18	16.73	17.21	17.70	18.15	18.52	18.83
±8	128	=	8	×	16	13.04	13.83	14.32	14.87	15.38	15.86	16.36	16.84	17.28

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.8-3(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF	OSR					128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					1953	977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN									
±2400	0.25	=	1	×	0.25	362.92	139.77	64.33	40.65	30.04	23.35	18.70	16.75	14.92
±2160	0.5	=	1	×	0.5	193.22	70.82	33.83	20.60	15.37	12.00	9.86	8.38	7.61
±1080	1	=	1	×	1	94.14	35.38	17.16	11.17	8.40	6.34	5.01	4.44	3.92
±540	2	=	1	×	2	46.23	18.59	9.48	6.13	4.57	3.35	2.66	2.28	2.05
±270	4	=	1	×	4	23.37	9.98	5.20	3.51	2.54	1.89	1.46	1.18	1.05
±135	8	=	1	×	8	12.66	5.47	3.06	2.06	1.51	1.11	0.84	0.67	0.56
±68	16	=	1	×	16	6.93	3.23	2.02	1.38	0.99	0.70	0.51	0.40	0.32
±8	128	=	8	×	16	1.86	1.29	0.91	0.63	0.44	0.32	0.22	0.16	0.12

Table 6.8-3(b) SD18 RMS Noise Table

The RMS noise is referred to the input. The Effective Number of Bits (ENOB (RMS Bit)) is defined as:

$$ENOB(RMS) = \ln\left(\frac{FSR}{RMS\,Noise}\right) \Big/ \ln(2)$$

$$RMS\,Noise = \left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right) \Big/ 2^{23}$$

$$Where\ FSR\ (Full\text{-}Scale\ Range) = 2 \times VREF/Gain.$$

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$

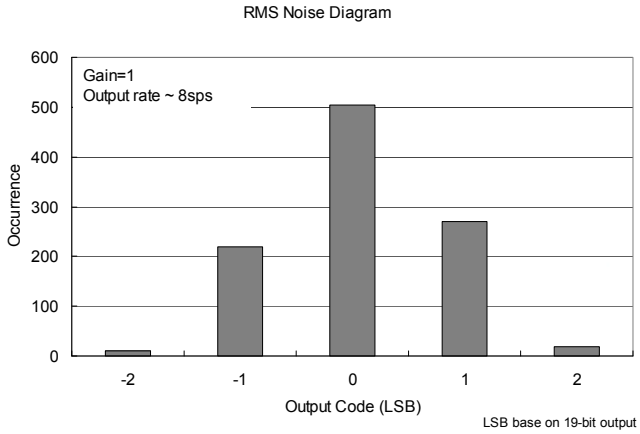


Figure 6.8-3(a) RMS Noise Diagram

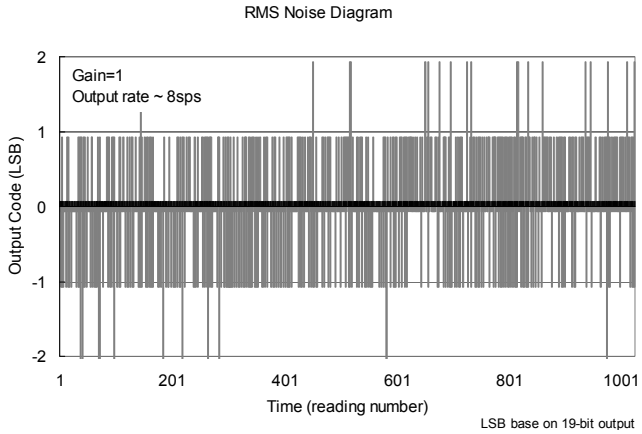


Figure 6.8-3(b) Output Code Diagram

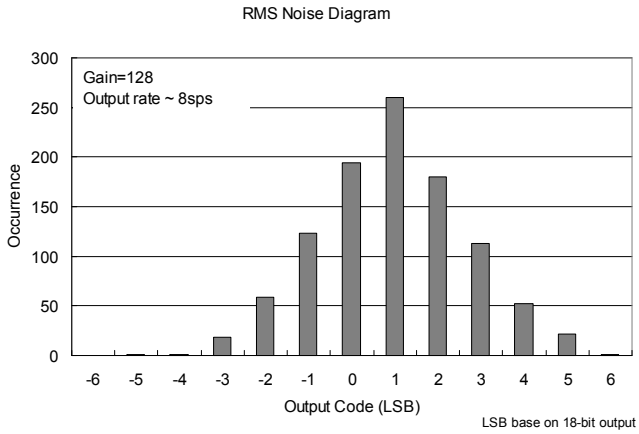


Figure 6.8-3(c) RMS Noise Diagram

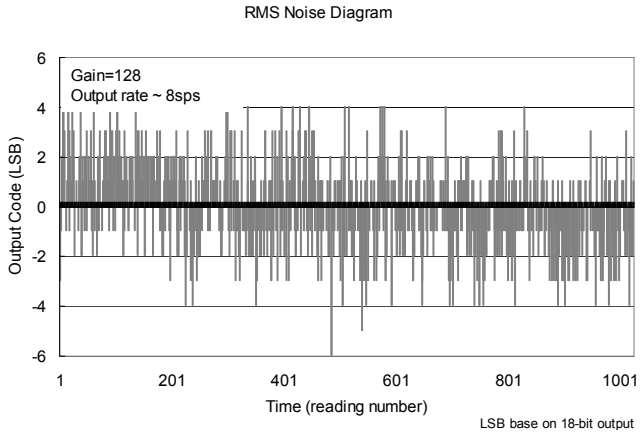


Figure 6.8-3(d) Output Code Diagram

6.9 Built-in EPROM (BIE)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage			6.0	6.5	V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V
When using external VBIE power to write BIE zone, one word can be written in a time via instruction in BIE zone.						

6.10 Built-in EPROM (BIE)_Low Voltage Control Circuit (HY11P52)

T_A=25℃, V_{DD} = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		3.05		3.4	V
V_{SS}	Supply Voltage			0		V
When HY11P52 starts 3.05V low programming voltage control circuit, it is not necessary to connect V_{BIE} power to program BIE zone.						

6.11 Built-in EPROM (BIE)_ Low Voltage Control Circuit (HY11P52B)

T_A=25℃, V_{DD} = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		2.75		3.6	V
V_{SS}	Supply Voltage			0		V
When HY11P52B starts 2.75V low programming voltage control circuit, it is not necessary to connect V_{BIE} power to program BIE zone.						

6.12 PFM Control Circuit

T_A = 25℃,V_{DD} = 3.3V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_S	PFM Switching Frequency		F_S		125	
F_B	Feedback Reference Voltage		F_B		0.2	
Activate PFM control loop: PWRCN[ENLEDP] =1b; using this control loop, PT1.2 needs to be set as input pin and PT1.6 as output pin						

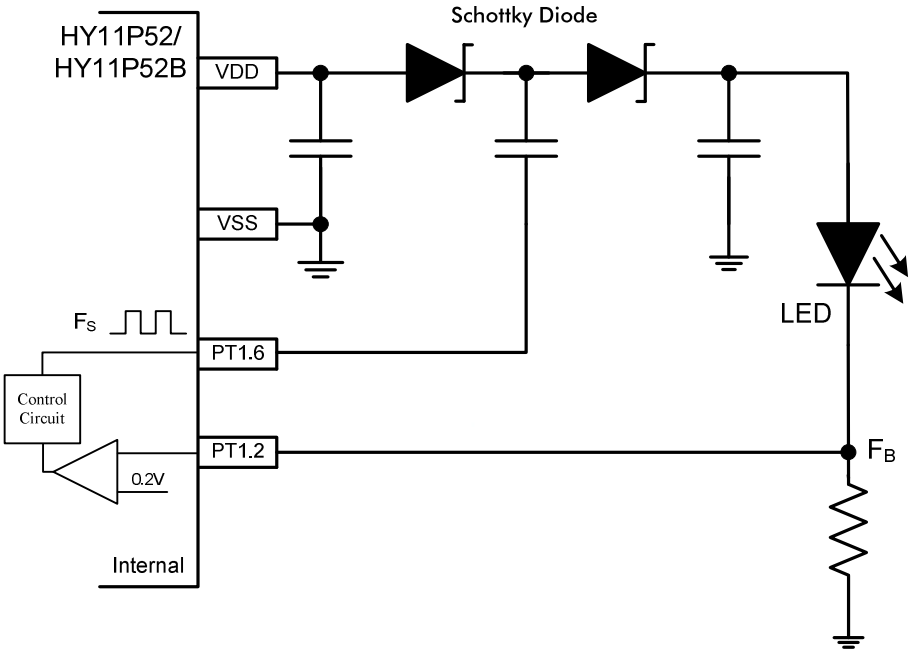


Figure 6.11 PFM Typical Application for LED Applications

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY11P52-D000	Die	-	D	000	000	-	250	Green[4]	-
HY11P52B-D000	Die	-	D	000	000	-	250	Green[4]	-
HY11P52-L048	LQFP	48	L	048	000	Tray	250	Green[4]	MSL-3
HY11P52B-L048	LQFP	48	L	048	000	Tray	250	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code** (Blank Code/ Standard/ Customized Programming Code)

Ex: Your HY11P52B customized programming code is 008 and you require die type.
The device No. will be HY11P52B-D000-008

Ex: You request HY11P52B blank code in die package.
The device No. will be HY11P52B-D000

Ex: You request HY11P52B blank code in LQFP48 package. The device no will be HY11P52B-L048. And please clearly indicate the shipment packing type as Tray type when placing orders.

Ex: Your HY11P52B customized programming code is 009 and you require LQFP48 package. The device no will be HY11P52-L048-009.
And please clearly indicate the shipment packing type when placing orders.

[2] **Code**

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

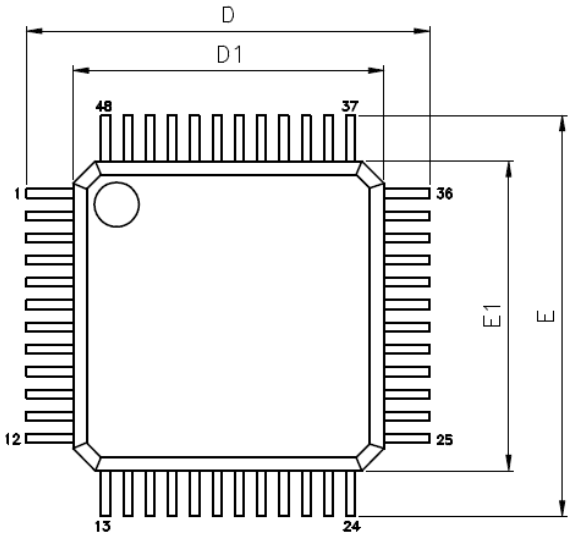
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%)

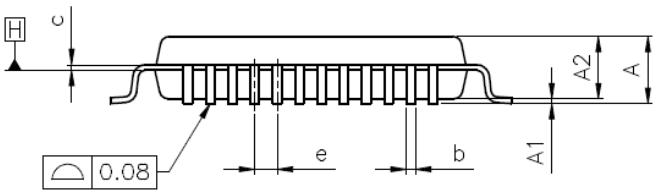
8. Package Information

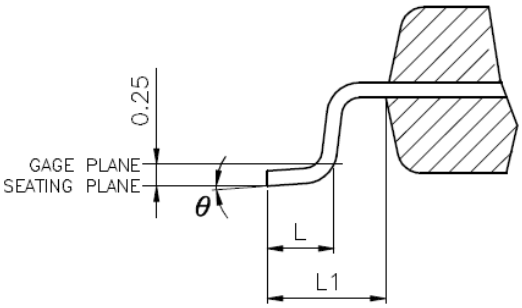
8.1. LQFP48(L048)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°





JEDEC MS-026 compliant

9. Appendix A

9.1. Difference of Simulator

When using HY11P series simulator (HY11S14-DK02), part of HY11P52/HY11P52B IC's new function cannot be simulated on existed simulator. Users can refer to HY11P52 low voltage programming/Look-up-table/PFM Application Note (APD-ICE001) and HY11P52B low voltage programming/Look-up-table/PFM Application Note to learn new function and operation setup. There are some design and programming differences under different models. Below table marks out major differences:

TA = 25℃,VDD = 3.0V, unless otherwise noted

Item	HY11P52	HY11P52B	HY11S14-DK02
LCD Module Current Consumption (I_{LCD})	10uA	8uA	20uA
VDDA Dropout Voltage (I_L=10mA)	250mV	250mV	180mV
VDDA Start up time (I_L=10mA)	1msec	1msec	5msec
ADC Over Sample Ratio (OSR)	128~32768	128~32768	256~32768
16Bits Look-up-table Instruction	Through BIE Look-up-table	Through BIE Look-up-table	Unsupportive
BIE Low Programming Voltage Control	Support VDD≧3,05V	Support VDD≧2.75V	Unsupportive
PFM Control Circuit	Supportive	Supportive	Unsupportive

Table A-1 Major Differences of HY11P52 and HY11P52B in Simulator

9.2. Difference of Current Consumption

Typical value of LCD module current consumption is around 20uA of HY11P series simulator (HY11S14-DK02) while that of HY11P52 IC's LCD module is reduced to only a half, 10uA remaining. HY11P52B has better LCD module current consumption, lowering than HY11P52, only 8uA remaining. Users can verify this in real IC after product development.

9.3. Difference of VDDA Power Source

VDDA Dropout Voltage (VDDA=2.4V, IL=10mA) of HY11P series simulator (HY11S14-DK02) has typical value around 180mV while HY11P52/HY11P52B IC's VDDA Dropout Voltage is enhanced to around 250 mV. Users can reserve VDDA Dropout voltage at product development stage, as to achieve best performance of VDDA power.
VDDA Start up time (VDDA=2.4V, IL=10mA, VDDA Cap: 1uF) of HY11P series simulator (HY11S14-DK02) has typical value around 5msec while HY11P52/HY11P52B IC's VDDA power support fast start up function. Its VDDA power regulation capacitor can reduce to

0.47uF and VDDA Start up time (VDDA=2.4V, IL=10mA, VDDA Cap: 0.47uF) reduce to around 1msec. Users can verify this function by adjusting VDDA power stabilization time to perform fast start up advantage in real IC after product development.

9.4. Difference of ADC OSR

ADC Over Sample Ratio (OSR) configurations of HY11P series simulator (HY11S14-DK02) can only select from 256~32768 while HY11P52/HY11P52B chip, ADC supports faster output rate options. It's ADC Over Sample Ratio (OSR) can be configured from 128~32768, equivalent to ADC output rate being enhanced from 1Ksps to 2Ksps, more applicable to applications that require faster ADC speed and 12-bit resolution. Users can set add in the program configuration and verify it in real IC.

9.5. Difference of 16Bits Look-up-table Instruction

When HY11P series simulator (HY11S14-DK02) programming data to BIE block, an external VDD=3V, VPP=6V voltage must be connected to implement BIE programming function.

HY11P52/HY11P52B has a new feature of BIE low programming voltage control. Users only need to connect VDD=3.05V voltage instead of VPP=6V voltage to implement BIE block programming function. Detailed description please refer to APD-ICE001 (HY11P52 Low Voltage Programming/Look-up-table/PFM Application Note), APD-ICE003 (HY11P52B Low Voltage Programming/Look-up-table/PFM Application Note). This function cannot be simulated on HY11P series simulator (HY11S14-DK02), users must connect to external VPP=6V voltage to simulate normal BIE programming function (no need to add VPP voltage in actual chip).

9.6. Difference of BIE, Low Programming Voltage Control Function

When HY11P series simulator (HY11S14-DK02) programming data to BIE block, an external VDD=3V, VPP=6V voltage must be connected to implement BIE programming function.

HY11P52/HY11P52B has a new feature of BIE low programming voltage control. Users only need to connect VDD=3.05V voltage instead of VPP=6V voltage to implement BIE block programming function. Detailed description please refer to APD-ICE001 (HY11P52 Low Voltage Programming/Look-up-table/PFM Application Note), APD-ICE003 (HY11P52B Low Voltage Programming/Look-up-table/PFM Application Note). This function cannot be simulated on HY11P series simulator (HY11S14-DK02), users must connect to external VPP=6V voltage to simulate normal BIE programming function (no need to add VPP voltage in actual chip).

9.7. Difference of PFM Control Circuit

PFM (Pulse-Frequency Modulation) control circuit is a new feature of HY11P52/HY11P52B. HY11P series simulator (HY11S14-DK02) does not support this function. Detailed operations manual please refer to APD-ICE001 (HY11P52 low voltage programming/look-up-table/PFM application notel) & low voltage programming/look-up-table/PFM application notel). This function cannot be simulated on HY11P Series simulator (HY11S14-DK02), users must add in the program configuration and verify it in real IC.

9.8. Fast ADC Output Configuration

HY11P52/HY11P52B ΣΔADC provides fast output function, which can be configured by OSR[3:0]=1010b to achieve OSR=128, equivalent ADC output rate is around 2Ksps (fast output setup).

Software configurations are as follows:

```
MVL     01000010B
MVF     ADCCN3,1,0          ; Configure ΣΔADC output frequency around 2Ksps
```

10. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V03	All	First Edition
V06	All	Revise All