HYCON TECHNOLOGY

HY11P54
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x32 LCD Driver
Low Noise Amplifier
18-Bit ΣΔADC

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1. Features

- 8-bit RISC, 66 instructions included.
- Operating voltage range: 2.2V to 3.6V, operation temperature range: -40℃~85℃.
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
  - Active Mode 300uA@2MHz
  - Standby Mode 3uA@32KHz
  - Sleep Mode 1uA
- 8K Word OTP (One Time Programmable) Type program memory, 256 Byte Data Memory.
- Brownout detector and Watch dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D).
  - Build-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x input signal gain selection.
  - Build-in Input zero point adjustment can increase measurement range according to different application.
  - Diverse data output rate. Max. 1.95ksps.
- Ultra-Low input noise (<1uVpp) OPAMP provides high output impedance small signal amplification and low current voltage transformation.
- 1.0V low temperatures drift parameter internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detect configuration and external input voltage detectable function.
- VDDA 2.4V with 10mA low dropout regulator function.
- 4x32 LCD driver
  - 1/4 Duty 1/3 Bias.
  - Embedded Charge Pump Regulated Circuit with 4 LCD Bias Voltage.
- 8-bit Timer A.
- 8-bit Timer C Module generates PWM/ PFD waveform.
- Built-in EPROM (BIE), 3.05V low voltage programming control circuit.
- Serial Communication SPI and EUART Module.
- Support 6 stack level.

Model No.	ADC	Program Memory (word)	Data Memory (byte)	Build-IN EPROM (word)	OPAMP	TPS	RTC	I/O	LCD Segment	PWM	Serial Interface	Pin
HY11P54-L100	9-CH	8k	256	64,LV	1	-	Y	13xI + 12xIO	4x32	1-CH	EUART	LQFP 100
HY11P54-L064	7-CH	8k	256	64,LV	1	-	Y	10xI + 10xIO	4x30	1-CH	EUART	LQFP 64

2. Pin Definition

2.1. HY11P54 LQFP100 Pin Diagram

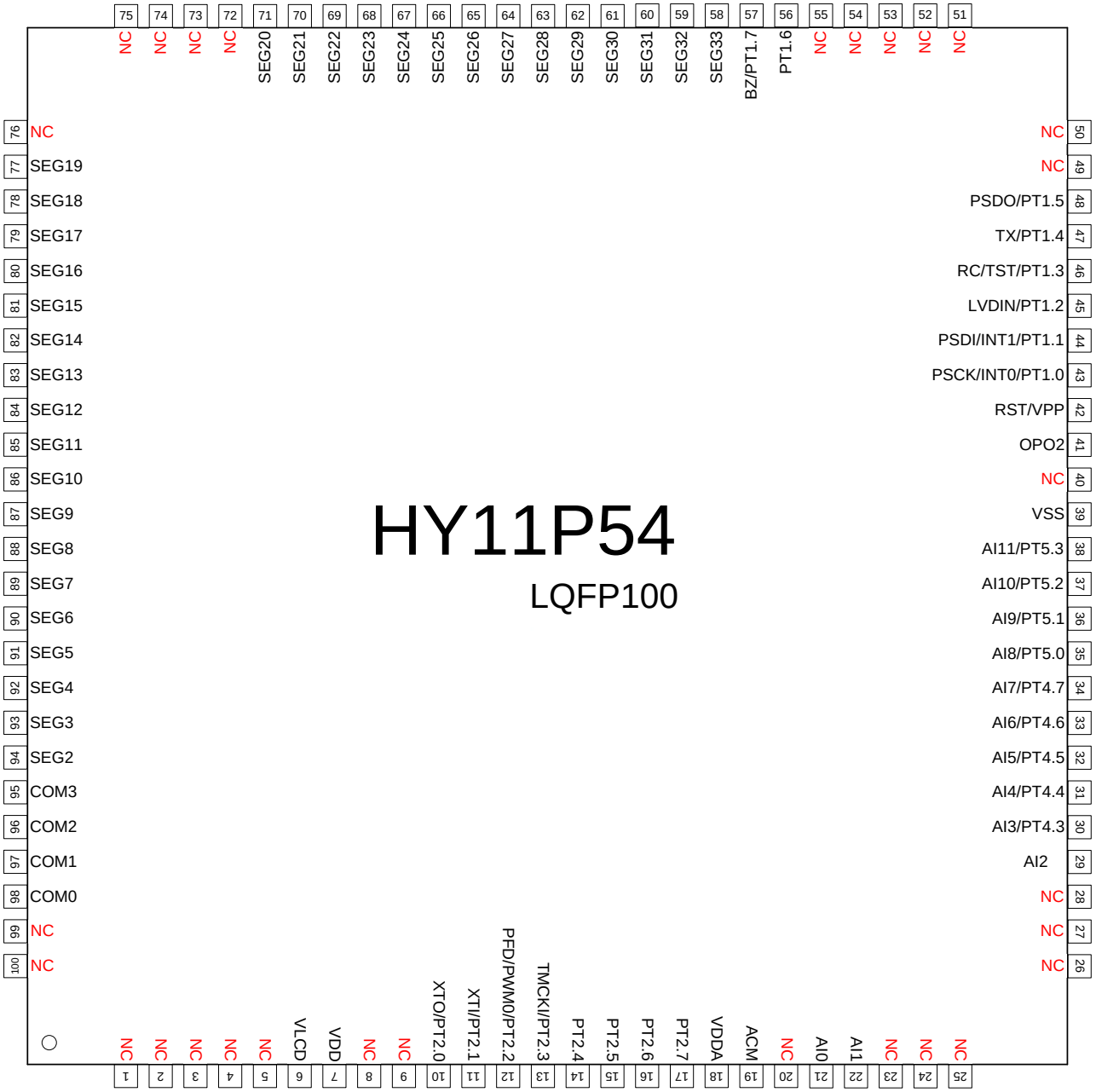


Figure 2-1 HY11P54 LQFP100 Pin Diagram

2.2. HY11P54 LQFP64 Pin Diagram

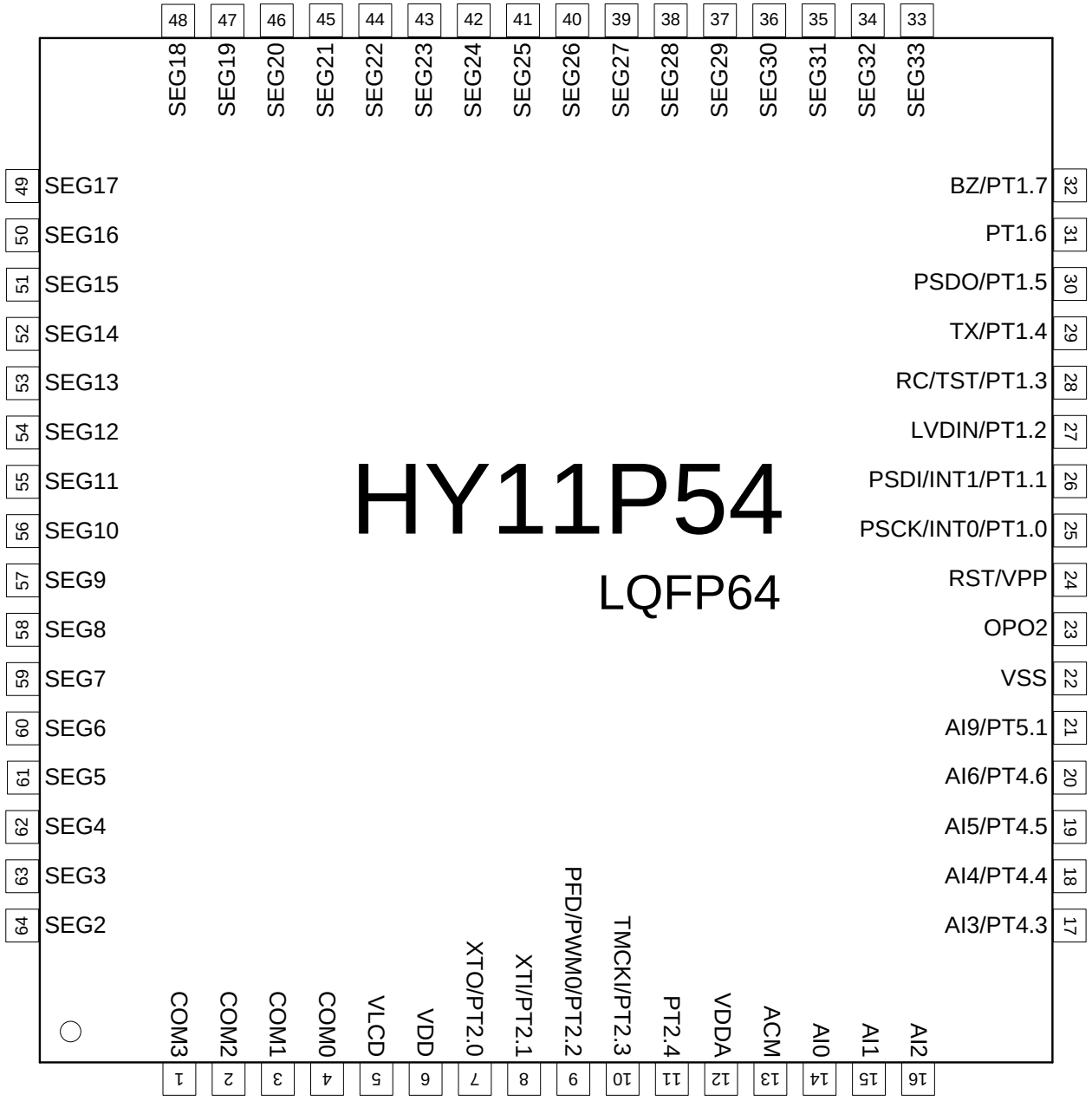


Figure 2-2 HY11P54 LQFP64 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 is not configured as external button pin, it will enhance the anti-interference ability.

2.3. HY11P54 I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

LQFP64 Pin NO.	LQFP100 Pin NO.	Pin Name	Pin Characteristic		Description
		HY11P54	Pin Type	Buffer Type	
5	6	VLCD	P	P	Power supply for LCD
6	7	VDD	P	P	Power supply for IC operation
7	10	PT2.0/XTO PT2.0 XTO	IO A	S A	Digital I/O External oscillator output
8	11	PT2.1/XTI PT2.1 XTI	I/O A	S A	Digital I/O External oscillator output
9	12	PT2.2/PWM0/PFD PT2.2 PWM0 PFD	I/O O O	C C C	Digital I/O PWM output PFD output
10	13	PT2.3/TMCKI PT2.3 TMCKI	I/O I	S S	Digital I/O TIMERC clock source input
11	14	PT2.4	I/O	S	Digital I/O
-	15	PT2.5	I/O	S	Digital I/O
-	16	PT2.6	I/O	S	Digital I/O
-	17	PT2.7	I/O	S	Digital I/O
12	18	VDDA	P	P	Regulator output, analog circuit power source
13	19	ACM	P	P	Internal analog circuit command ground pin
14	21	AI0	A	A	Analog channel pin
15	22	AI1	A	A	Analog channel pin
16	29	AI2	A	A	Analog channel pin
17	30	PT4.3/AI3 PT4.3 AI3	I A	S A	Digital input Analog channel pin
18	31	PT4.4/AI4			

		PT4.4 AI4	I A	S A	Digital input Analog channel pin
19	32	PT4.5/AI5 PT4.5 AI5	 I A	 S A	 Digital input Analog channel pin
20	33	PT4.6/AI6 PT4.6 AI6	 I A	 S A	 Digital input Analog channel pin
-	34	PT4.7/AI7 PT4.7 AI7	 I A	 S A	 Digital input Analog channel pin
-	35	PT5.0/AI8 PT5.0 AI8	 I A	 S A	 Digital input Analog channel pin
21	36	PT5.1/AI9 PT5.1 AI9	 I A	 S A	 Digital input Analog channel pin
-	37	PT5.2/AI10 PT5.2 AI10	 I A	 S A	 Digital input Analog channel pin
-	38	PT5.3/AI11 PT5.3 AI11	 I A	 S A	 Digital input Analog channel pin
22	39	VSS	P	P	Grounding pin for IC operation voltage
23	41	OPO2	A	A	OP output
24	42	RST/VPP RST VPP	I P	S P	Reset IC EPROM Programming voltage input
25	43	PT1.0/INT0/PSCK PT1.0 INT0 PSCK	 I I I	 C S S	 Digital input Interrupt input INT0 OTP programming interface SCK
26	44	PT1.1/INT1/PSDI PT1.1 INT1 PSDI	 I I I	 C S S	 Digital input Interrupt input INT1 OTP programming interface SDI
27	45	PT1.2/LVDIN	I	C	

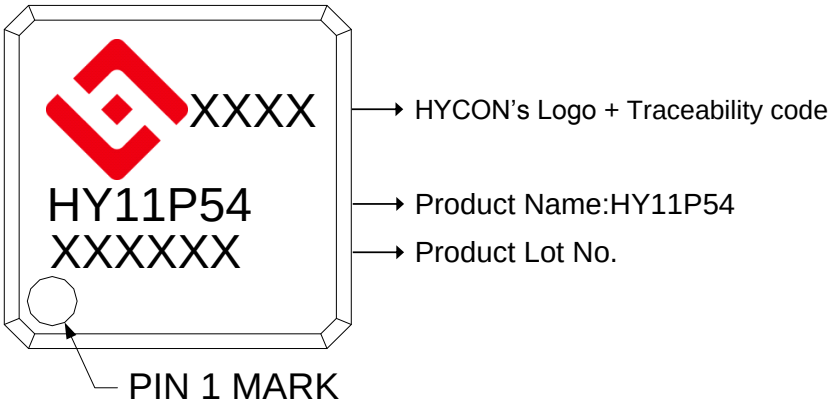
		PT1.2 LVDIN	A	A	Digital input LVD external signal input port
28	46	PT1.3/TST/RC PT1.3 TST RC	I I I	C S S	Digital input Test Mode input pin (invalid) EUART communication interface RC
29	47	PT1.4/TX PT1.4 TX	I/O I	C S	Digital I/O EUART communication interface TX
30	48	PT1.5/PSDO PT1.5 PSDO	I/O O	S C	Digital I/O OTP programming interface SDO
31	56	PT1.6 PT1.6	I/O	S	Digital I/O
32	57	PT1.7/BZ PT1.7 BZ	I/O O	S C	Digital I/O Buzzer output
33	58	SEG33	O	A	Segment output for LCD
34	59	SEG32	O	A	Segment output for LCD
35	60	SEG31	O	A	Segment output for LCD
36	61	SEG30	O	A	Segment output for LCD
37	62	SEG29	O	A	Segment output for LCD
38	63	SEG28	O	A	Segment output for LCD
39	64	SEG27	O	A	Segment output for LCD
40	65	SEG26	O	A	Segment output for LCD
41	66	SEG25	O	A	Segment output for LCD
42	67	SEG24	O	A	Segment output for LCD
43	68	SEG23	O	A	Segment output for LCD
44	69	SEG22	O	A	Segment output for LCD
45	70	SEG21	O	A	Segment output for LCD
46	71	SEG20	O	A	Segment output for LCD
47	77	SEG19	O	A	Segment output for LCD
48	78	SEG18	O	A	Segment output for LCD
49	79	SEG17	O	A	Segment output for LCD
50	80	SEG16	O	A	Segment output for LCD
51	81	SEG15	O	A	Segment output for LCD

52	82	SEG14	O	A	Segment output for LCD
53	83	SEG13	O	A	Segment output for LCD
54	84	SEG12	O	A	Segment output for LCD
55	85	SEG11	O	A	Segment output for LCD
56	86	SEG10	O	A	Segment output for LCD
57	87	SEG9	O	A	Segment output for LCD
58	88	SEG8	O	A	Segment output for LCD
59	89	SEG7	O	A	Segment output for LCD
60	90	SEG6	O	A	Segment output for LCD
61	91	SEG5	O	A	Segment output for LCD
62	92	SEG4	O	A	Segment output for LCD
63	93	SEG3	O	A	Segment output for LCD
64	94	SEG2	O	A	Segment output for LCD
1	95	COM3	O	A	Segment output for LCD
2	96	COM2	O	A	Segment output for LCD
3	97	COM1	O	A	Segment output for LCD
4	98	COM0	O	A	Segment output for LCD
-	Others	NC	-	-	Not connect

Table 2-1 Pin Definition and Function Description

2.4. Package marking information

2.4.1 Package marking information



3. Application Circuit

3.1. Bridge Sensor

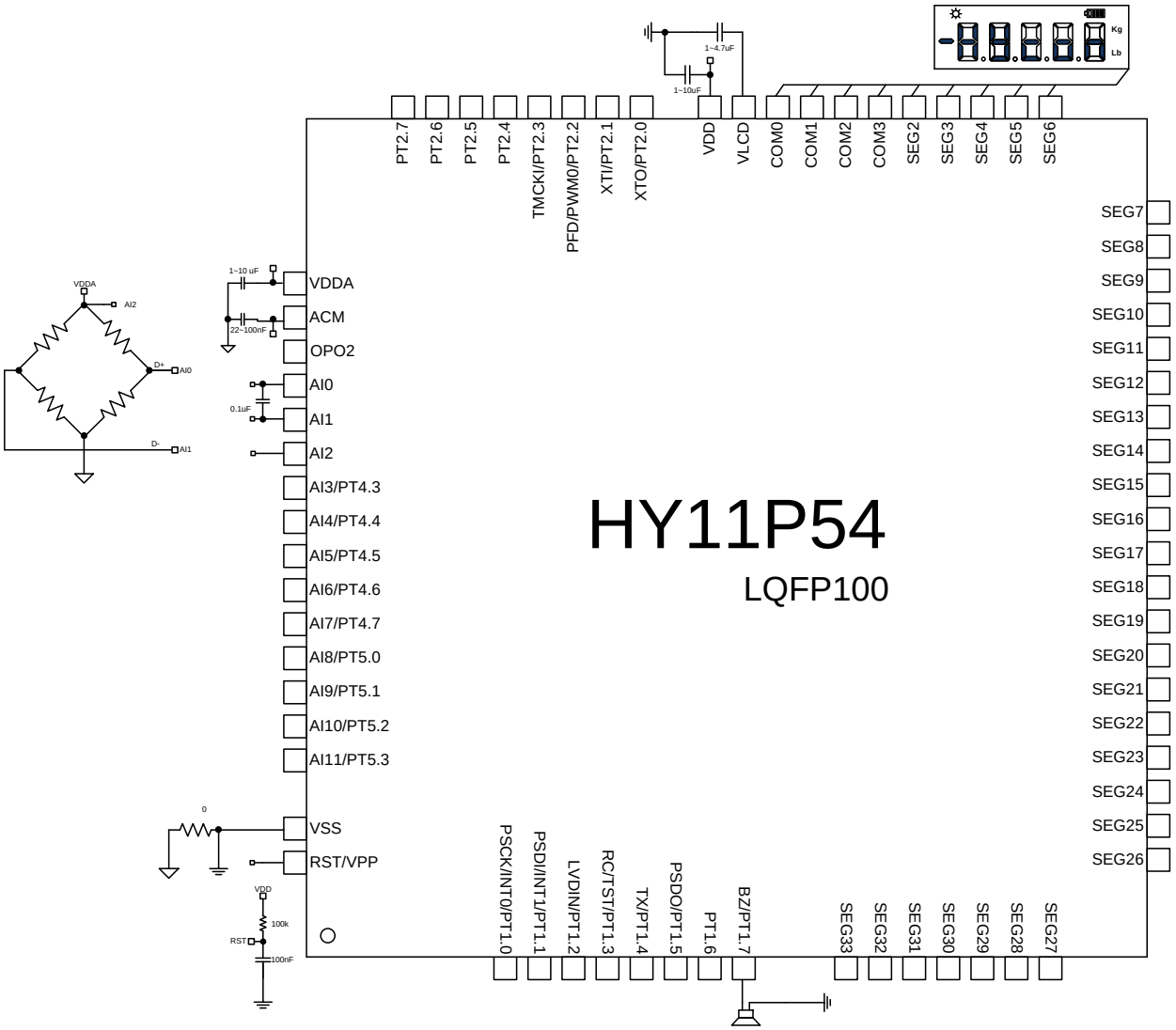


Figure 3-1 Application Circuit of Compensation Bridge Sensor

Note：DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address.

4. Function Outline

4.1. Internal Block Diagram

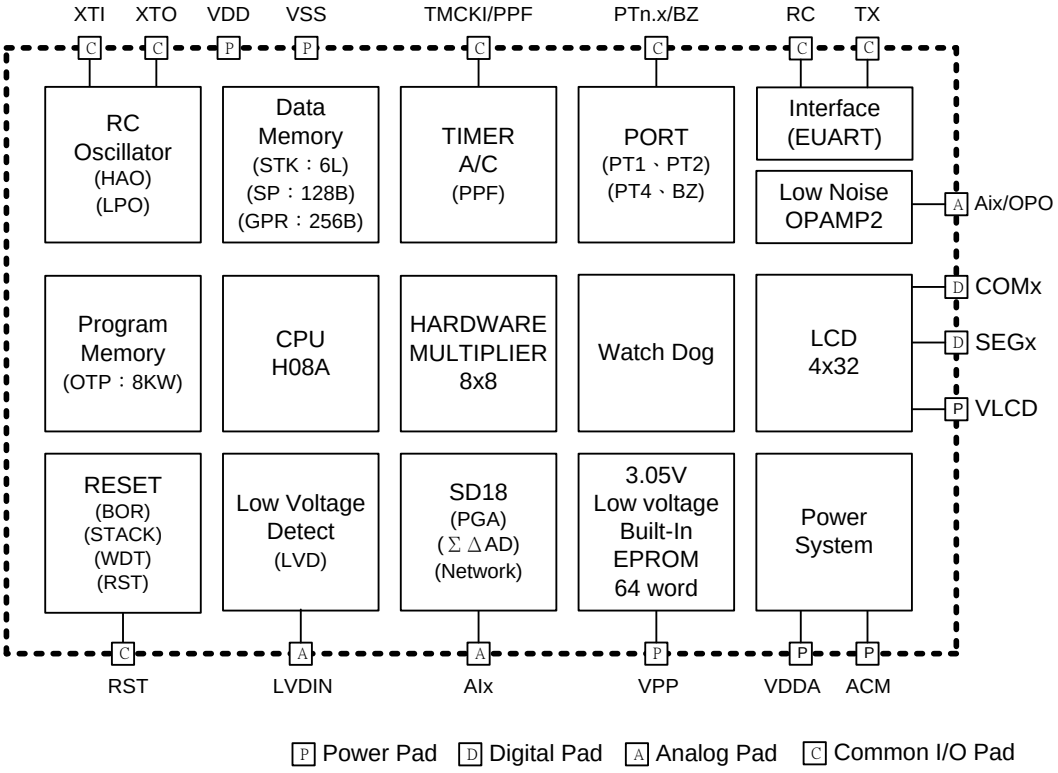


Figure 4-1 HY11P54 Internal Block Diagram

4.2. Related Description and Supporting Documents

IC Function Related Operating Instruction

DS-HY11P54-Vxx	HY11P54 Data Sheet
UG-HY11S14-Vxx	HY11Pxx Series Users' Manual
APD-CORE002-Vxx	H08A Instruction Description

Development Tool Related Operating Instruction

APD-HYIDE006-Vxx	HY11xxx Series Development Tool Software Instruction Manual
APD-HYIDE005-Vxx	HY11xxx Series Development Tool Hardware Instruction Manual
APD-OTP001-Vxx	OTP Products Programming Pin Manual

Product Production Related Operating Instruction

APD-HYIDE004-Vxx	HY1xxxx Series Production Line Specialized Programmer Manual
BDI-HY11P54-Vxx	HY11P54 Individual Product Die Bonding Information

4.3. SD18 Network

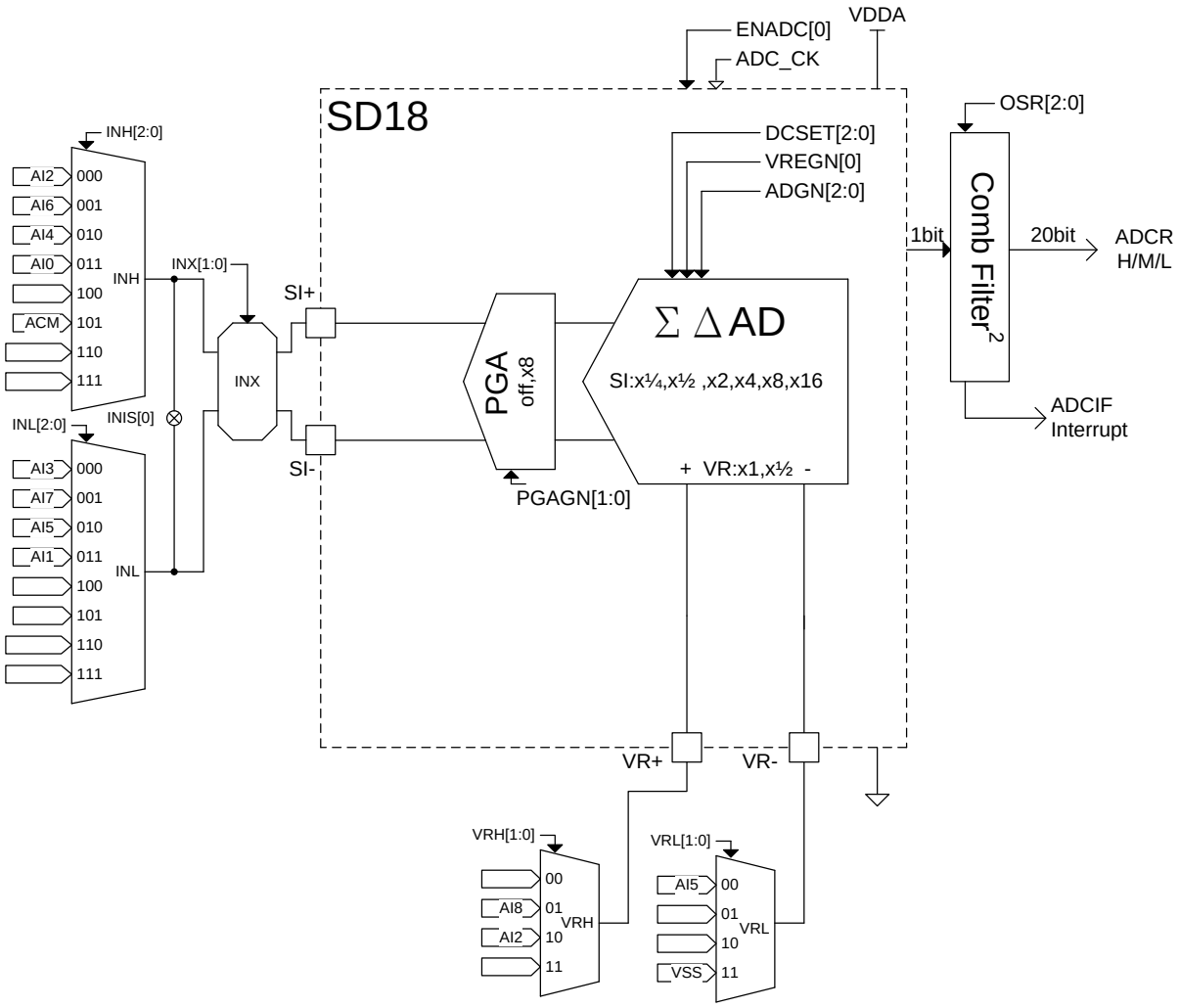


Figure 4-2 SD18 Network

4.4. LNOP2 Network

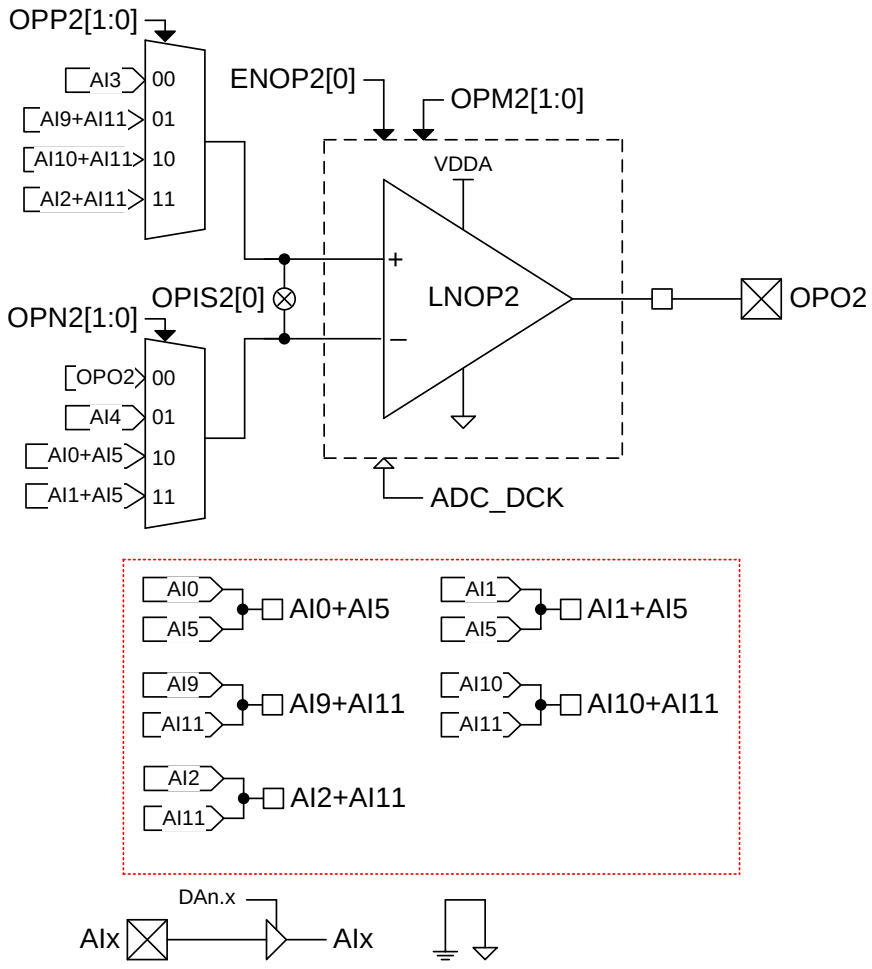


Figure 4-3 Low Noise OPAMP2 Network

5. Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W
00H	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
01H	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
02H	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
03H	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
04H	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
05H	INDF1	Contents of FSR1 to address data memoryvalue of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
06H	POINC1	Contents of FSR1 to address data memoryvalue of FSR0 post-incremented								N/A	N/A	*,*,*,*,*,*,*,*
07H	PODEC1	Contents of FSR1 to address data memoryvalue of FSR0 post-decremented								N/A	N/A	*,*,*,*,*,*,*,*
08H	PRINC1	Contents of FSR1 to address data memoryvalue of FSR0 pre-incremented								N/A	N/A	*,*,*,*,*,*,*,*
09H	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR0 offset by W								N/A	N/A	*,*,*,*,*,*,*,*
0FH	FSR0H								FSR0[8]	x	....u	-,-,-,-,-,-,-,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
11H	FSR1H								FSR1[8]	x	....u	-,-,-,-,-,-,-,*
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
16H	TOSH					TOS[11]	TOS[10]	TOS[9]	TOS[8]	 0000	 0000	-,-,-,-,*,*,*,*
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV			STKPRT[2:0]			000. .000	000. .000	r,rw 0,rw 0,- -,r,r,r
1AH	PCLATH					PC[11]	PC[10]	PC[9]	PC[8]	 0000	 0000	-,-,-,-,*,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1DH	TBLPTRH					TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	 0000	 0000	-,-,-,-,*,*,*,*
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1FH	TBLDH	Program Memory Table Latch High Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	0000 0000	*,*,*,*,*,*,*,*
21H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
22H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
23H	INTE1	GIE	ADCIE	TMCIE		TMAIE	WDTIE	E1IE	E0IE	000. 0000	000. 0000	*,*,*,*,*,*,*,*
24H	INTE2	TXIE	RCIE							00.. 0000	00.. 0000	*,*,-,-,*,*,*,*
26H	INTF1		ADCIF	TMCIF		TMAIF	WDTIF	E1IF	E0IF	.00. 0000	.00. 0000	-,*,*,-,*,*,*,*
27H	INTF2	TXIF	RCIF							00.. 0000	00.. 0000	*,*,-,-,*,*,*,*
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2AH	BSRCN								BSR[0]	0	0	-,-,-,-,-,-,-,*
2BH	STATUS				C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
2CH	PSTATUS	PD	TO	IDLEB	BOR		SKERR			000d .0..	uduu .d..	rw 0,rw 0,rw 0,rw 0 -,rw 0,-,-
2DH	LVDCN		LVDFG	LVD	LVDON	VLDX[3:0]				.000 0000	.000 uuuu	-,*,r,r *,*,*,*
30H	PWRCN	ENVDDA	**VDDAX[1:0]=11**		ENACM			**ENLEDP**		0xx0 ..0.	0xx0 ..0.	*-,-,-*-,-,-,-
31H	MCKCN1	ADCS[2:0]			ADCCK	XTHSP	XTSP	ENXT	ENHAO	0000 0001	0000 0001	*,*,*,*,*,*,*,*
32H	MCKCN2			LSCK	HSCK	HSS[1:0]		CPUCK[1:0]		..00 0000	..00 0000	-,-,*,*,*,*,*,*
33H	MCKCN3	LCDS[2:0]				PERCK	BZS[2:0]			000. 0000	000. 0000	*,*,*,-,*,*,*,*
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte				0	0	0	0	xxxx 0000	uuuu 0000	r,r,r,r r0,r0,r0,r0
3CH	ADCCN1	ENADC		ENCHP	PGAGN[1:0]		ADGN[2:0]			0.00 0000	0.00 0000	*,-,*,*,*,*,*,*
3DH	ADCCN2			**INBUF=0**	**VRBUF=0**	VREGN	DCSET[2:0]			...xx 0000	...xx 0000	-,-,-,*,*,*,*,*
3EH	ADCCN3	OSR[2:0]						**OSR[3]**		000. ..0.	000. ..0.	*,*,-,-,-,*,-,-
3FH	AINET1	INH[2:0]			INL[2:0]			INIS		0000 000x	0000 000x	-,-,-,*,*-,-,*,-
40H	AINET2		VRH[1:0]		INX[1:0]		VRL[1:0]			xx00 xx0x	xx00 xx0x	-,-,-,*,*,*-,-,-
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,*w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
46H	TMCCN	ENTMC	TMCCK[1:0]		TMCS1[2:0]			TMCS0[1:0]		0000 0000	0000 0000	*,*,*,*,*,*,*,*
47H	PRC	TimerC programmable register								1111 1111	1111 1111	*,*,*,*,*,*,*,*
48H	TMCR	TimerC register								0000 0000	0000 0000	r,r,r,r r,r,r,r
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]						0000	0000	*,*,*,*-,-,-,-,-
51H	PWMR	PWM MSB Byte register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	**LCDBI[1:0]=10**			0000 0xxx	0000 0xxx	*,*,*,*,-,-,-,-
53H	LCDCN2	LCDBL	**LCDMX[1:0]=11**							0xxx xxxx	0xxx xxxx	-,-,-,-,-,-,-,-
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5AH	LCD6	Segment SEG14@[3:0] and SEG15@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5BH	LCD7	Segment SEG16@[3:0] and SEG17@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5CH	LCD8	Segment SEG18@[3:0] and SEG19@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
5DH	LCD9	Segment SEG20@[3:0] and SEG21@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
63H	URCON	ENSP	ENTX	TX9	TX9D	PARITY			WUE	0000 0..0	0000 0..0	*,*,*,*-,-,-,*
64H	URSTA		RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0110	.000 0110	-,r,r,r r,r,r,rw 0
65H	BAUDCON					ENCR	RC9	ENADD	ENABD	 0000	 0000	-,-,-,-,*,*,*,*
66H	BRGRH	Baud Rate Generator Register High Byte								...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
67H	BRGRL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
68H	TXREG	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
69H	RCREG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
6AH	PT4	PT4.7	PT4.6	PT4.5	PT4.4	PT4.3				xxxx x...	uuuu u...	r,r,r,r r,r,r,r
6BH	PT4DA	DA4.7	DA4.6	DA4.5	DA4.4	DA4.3	DA4.2	DA4.1	DA4.0	1111 1111	1111 1111	*,*,*,*,*,*,*,*
6CH	PT4PU	PU4.7	PU4.6	PU4.5	PU4.4	PU4.3				0000 0...	0000 0...	*,*,*,*,*,*,*,*
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000	0000	*,*,*,*-,-,-,-
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*

Table 5-1a HY11P54 Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1												
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition												
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**i-RESET**	**R/W**
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		 0000	 0000	-,-,-,- *,*,*
72H	PT1M2		PM1.7[0]						PM1.4[0]	.0.. ...0	.0.. ...0	-,*,-,- -,-,-,-
74H	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	-,-,-,- *,*,*
75H	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	0000 0000	-,-,-,- *,*,*
77H	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	0000 0000	-,-,-,- *,*,*
78H	PT2M1			PM2.2[1]	PM2.2[0]					..00	..00	-,-,** -,-,-,-
80H ~ FFH	GPR0	General Purpose Register as 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
100H~17FH	GPR1	General Purpose Register as 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
180H	LCD10	Segment SEG22@[3:0] and SEG23@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
181H	LCD11	Segment SEG24@[3:0] and SEG25@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
182H	LCD12	Segment SEG26@[3:0] and SEG27@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
183H	LCD13	Segment SEG28@[3:0] and SEG29@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
184H	LCD14	Segment SEG30@[3:0] and SEG31@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
185H	LCD15	Segment SEG32@[3:0] and SEG33@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
192H	PT5					PT5.3	PT5.2	PT5.1	PT5.0	 xxxx	.... uuuu	r,r,r,r r,r,r,r
193H	PT5DA					DA5.3	DA5.2	DA5.1	DA5.0	 1111	 1111	*,*,*,*,*,*,*,*
194H	PT5PU					PU5.3	PU5.2	PU5.1	PU5.0	 0000	 0000	*,*,*,*,*,*,*,*
195H	BIECTRLA					VPP_HIGH		BIEWR	BIERD	1000 d000	1000 d000	-,-,-,- *,r0,*,*
196H	BIEPTRHA	SBMSEL					BIE_ADDR[10:8]			1000 0000	1000 0000	w0,w0,W0,W0 W0,W0,W0,W0
197H	BIEPTRLA	0	0	BIE_ADDR[5:0]						0000 0000	0000 0000	w 0,w 0,*,*,*,*,*,*
198H	BIEDHA	BIE_DATA[15:8]								xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
199H	BIEDLA	BIE_DATA[7:0]								xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
19BH	OPCN2	ENOP2	OPM2[1:0]		OPIS2[0]	OPP2[1:0]		OPN2[1:0]		0000 0000	0000 0000	*,*,*,*,*,*,*,*

Table 5-1b HY11P54 Register List

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS}. . . . . −0.2 V to 4.0 V

Voltage applied to any pin . . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.3 pin . . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal. . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT2 I/O pin. 25mA

6.1. Recommended Operating Conditions

T_A = -40℃ ~ 85℃, unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		All digital peripherals and CPU		2.2		3.6	V
			Analog peripherals		2.4		3.6	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.2V, ENXT[0]=1	XTSP[0]=0, XTHSP[0]=0	32.768K			Hz
		Ceramic resonator		XTSP[0]=1, XTHSP[0]=0	450K		8M	
		Crystal		XTSP[0]=1, XTHSP[0]=0	1M		8M	

6.2. Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.6	2.0	2.4	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

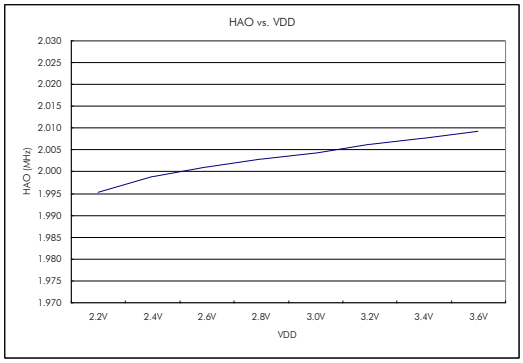


Figure 6.2-1 HAO vs. VDD

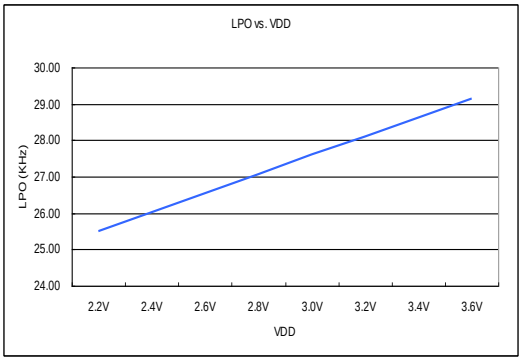


Figure 6.2-2 LPO vs. VDD

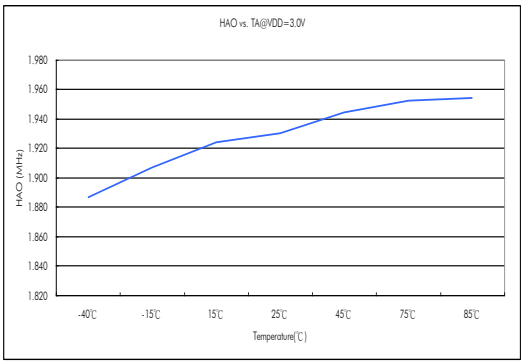


Figure 6.2-3 HAO vs. Temperature

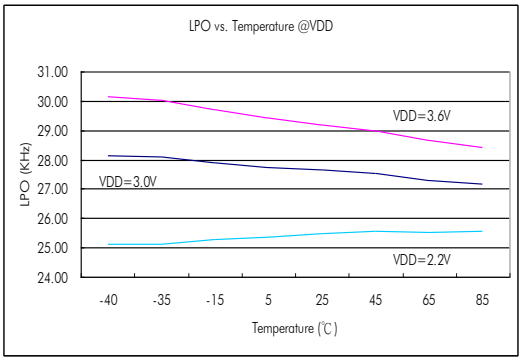


Figure 6.2-4 LPO vs. Temperature

6.3. Supply Current into VDD Excluding Peripherals Current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 28KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1.34	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.36	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.2	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

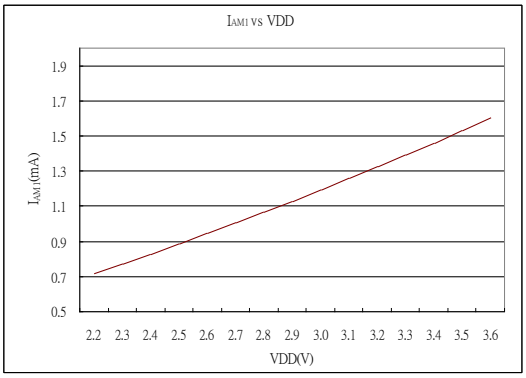


Figure 6.3-1 I_{AM1} vs. VDD

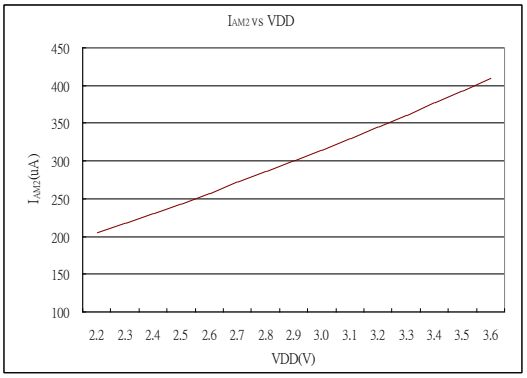


Figure 6.3-2 I_{AM2} vs. VDD

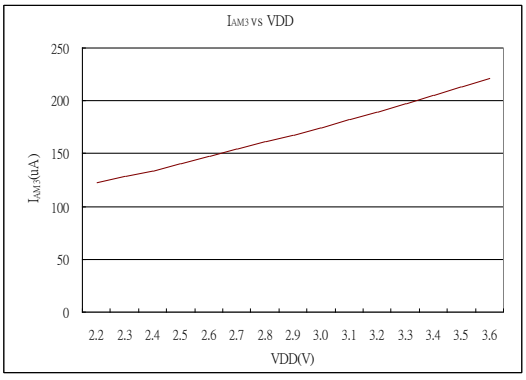


Figure 6.3-3 I_{AM3} vs. VDD

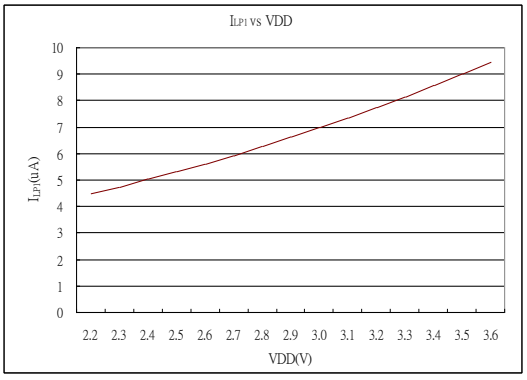


Figure 6.3-4 I_{LP1} vs. VDD

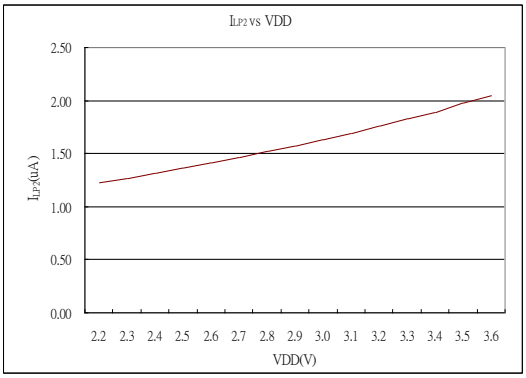


Figure 6.3-5 I_{LP2} vs. VDD

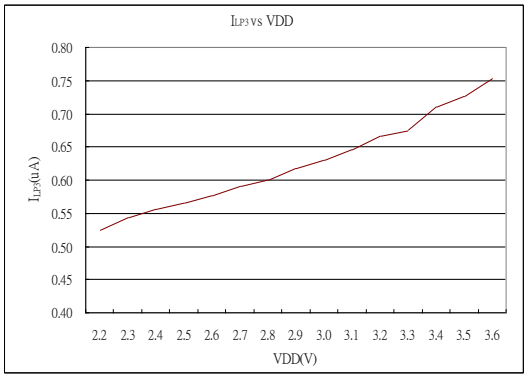


Figure 6.3-6 I_{LP3} vs. VDD

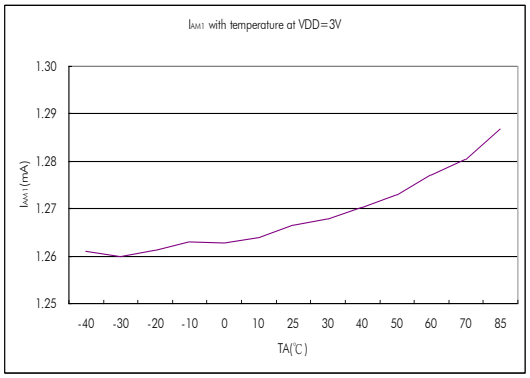


Figure 6.3-7 I_{AM1} vs. Temperature

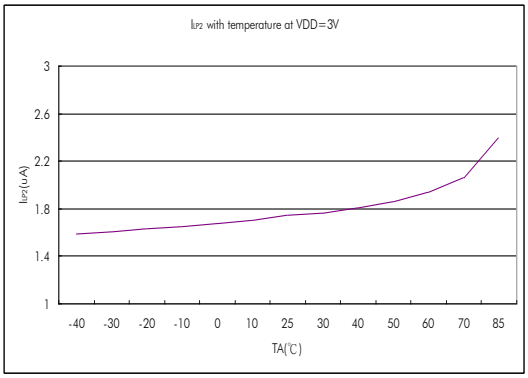


Figure 6.3-8 I_{LP2} vs. Temperature

.

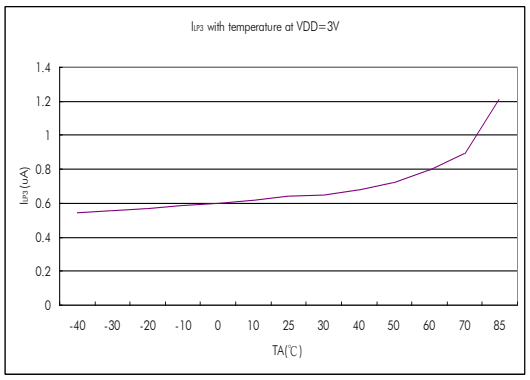


Figure 6.3-9 I_{LP3} vs. Temperature

6.4. Port1~2

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

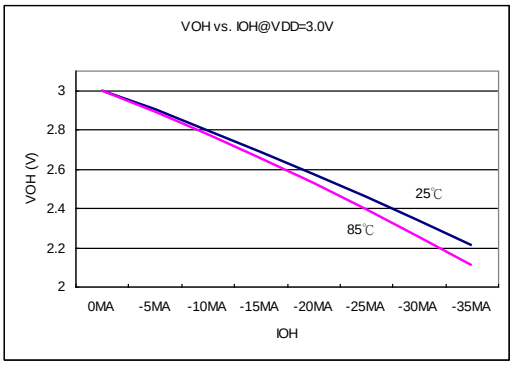


Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

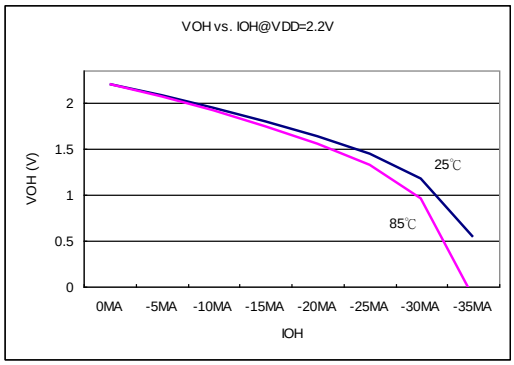


Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

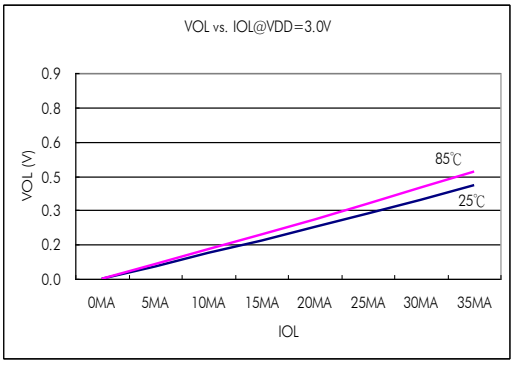


Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

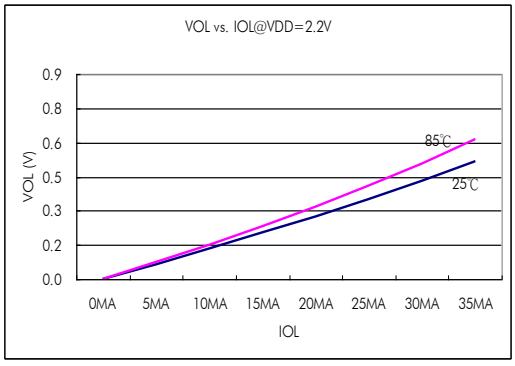


Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5. Reset (Brownout, External RST Pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		100		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

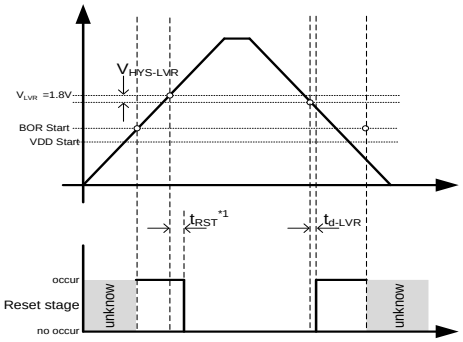


Figure 6.5-1 BOR reset diagram

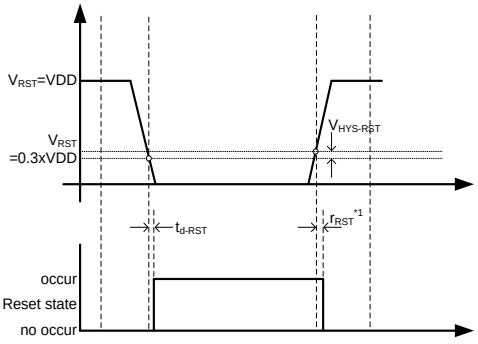


Figure 6.5-2 RST reset diagram

*1 r_{RST}：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

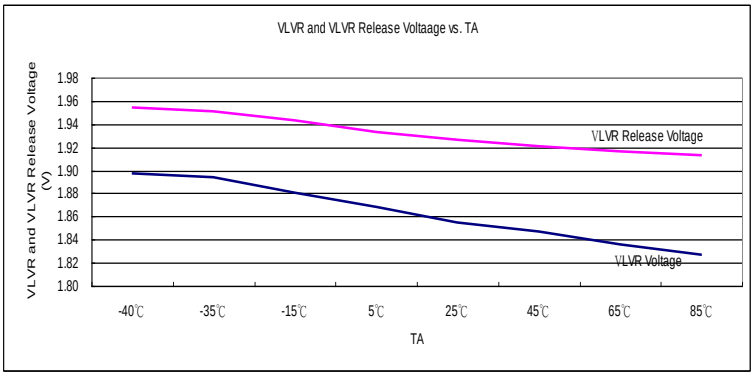


Figure 6.5-3 LVR vs. Temperature

6.6. Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.25V	VDDAX [1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX [1:0]=11b		250		mV
	Temperature drift	VDDAX [1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1, I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift				100		uV/V
VDDA：Adjust Voltage Regulator ACM：Analog Common Mode Voltage							

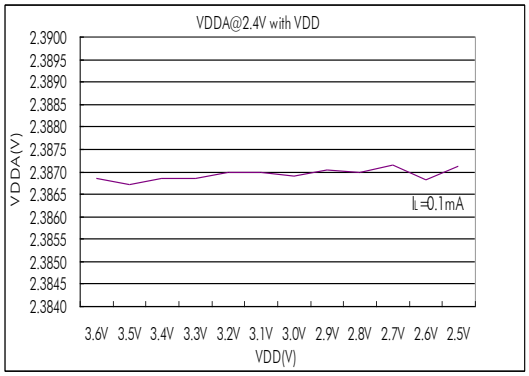


Figure6.6-1 VDDA I_L=0.1mA vs. VDD

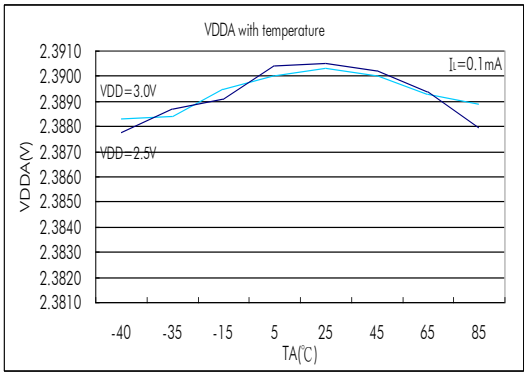


Figure6.6-2 VDDA I_L=0.1mA vs. Temperature

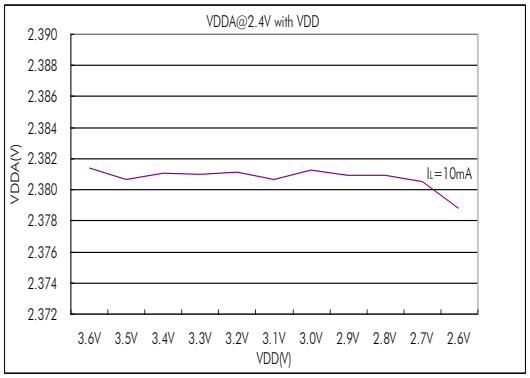


Figure6.6-3 VDDA I_L=10mA vs. VDD

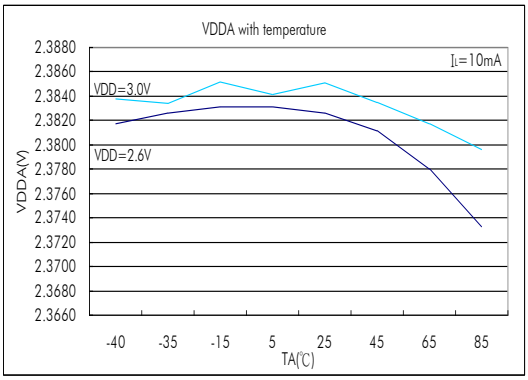


Figure6.6-4 VDDA I_L=10mA vs. Temperature

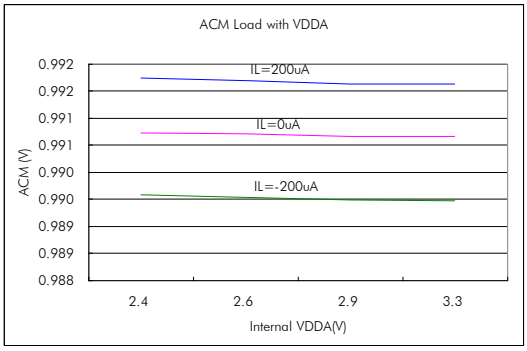


Figure6.6-5 ACM Load vs. VDDA

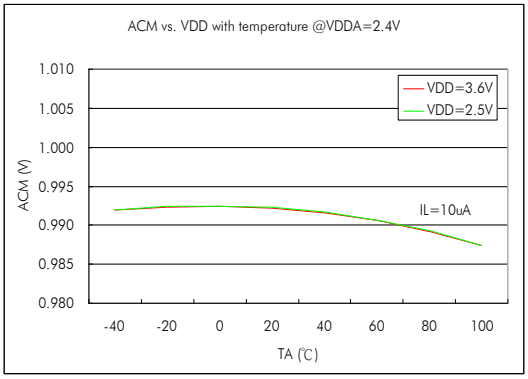


Figure6.6-6 ACM vs. Temperature

6.7. LCD

T_A = 25℃,V_{DD} = 3.0V, C_{VLCD} =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	V_{DD} = 2.2V		10		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =4.7uF	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
			VLCDX[1:0]=00b	2.97	3.3	3.63	
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

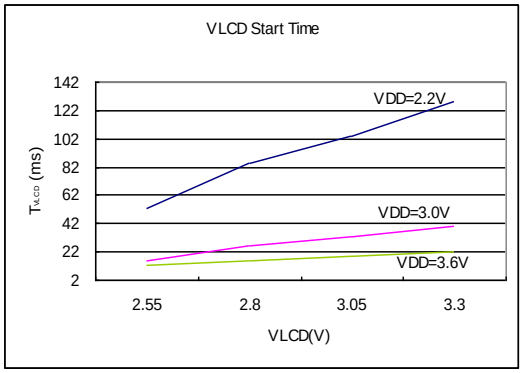


Figure 6.7-1 LCD start time

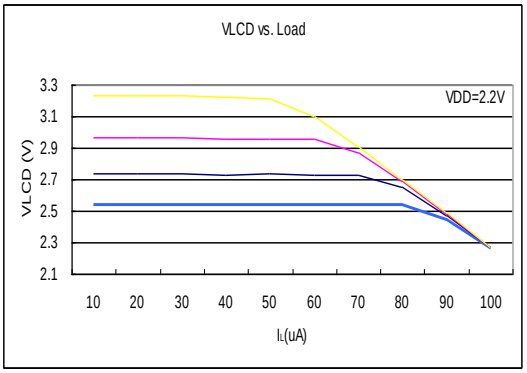


Figure6.7-2 VLCD vs. IL @VDD=2.2V

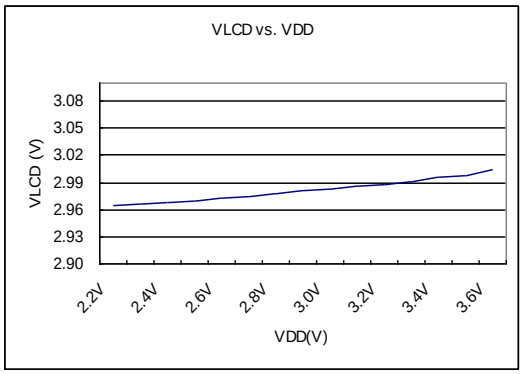


Figure6.7-3 VLCD vs. VDD

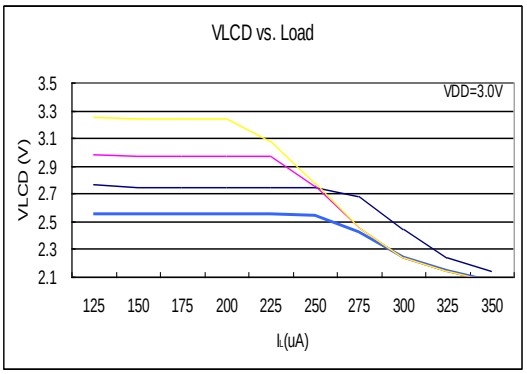


Figure 6.7-4 VLCD vs. IL @VDD=3.0V

6.8. Low Noise OPAMP 2

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{LNOP}	Supply voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{LNOP}	Operation supply current		OPM[1:0]=xxb		200		uA
V_{OS-OP}	Input offset voltage without chopper.		OPM[1:0]=1xb	-2		2	mV
	Input offset voltage with chopper		OPM[1:0]=0xb		20		uV
	Input offset voltage temperature drift.	OPM[1:0]=00b	T_A=-40℃~85℃		0.1		uV
		OPM[1:0]=10			2		℃
V_{OLR}	Unit gain load regulation	V_O=1.2V, VDDA=2.4V	I_L=+1mA		0.1		%V_O
			I_L=-1mA				
CMVR	Common-mode voltage input range		OPM[1:0]=xxb	0.1		VDDA-1.1	V
CMRR	Common-mode rejection ratio		OPM[1:0]=xxb		90		dB

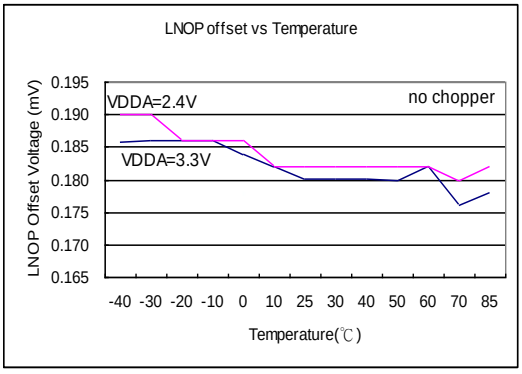


Figure 6.8-1 LNOP2 Offset Temperature

6.9. SD18, Power Supply and Recommended Operating Conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			128 *1		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz		120		uA

*1, OSR=128, setting by ADCCN3[OSR3] bit.
OSR[3:0]=1010b, OSR=128; OSR[3:0]=0xxx, OSR=256 ~ 32768
OSR[3:0]=1xxxb can't set by user

2.4.2 PGA, Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<01>or<1x>			320		Ua
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		5		ppm/℃

2.4.3 SD18, performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions			Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV				±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV						
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b			19			Bits
G_{SD18}	Temperature drift **Gain 1~x16 (INBUF[0]=0b,)**	INBUF[0]=0b,VRBUF[0]=0b		T_A = -40℃~ 85℃		10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short		Gain=2			1	%FSR
	Offset error temperature drift with chopper without PGA			GAIN=1		2		uV/℃
				GAIN=2		1		
				GAIN=4		0.5		
				GAIN=16		0.15		

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16		75		
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off		75		dB
			GAIN=16 PGA=8				

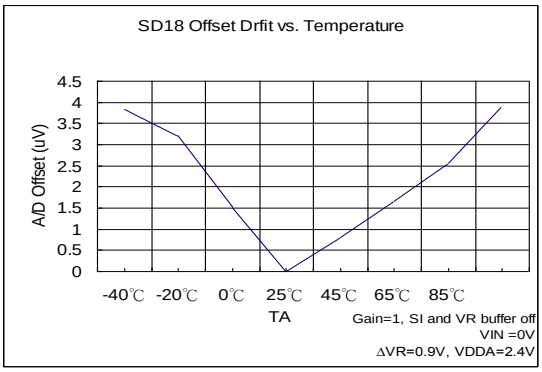


Figure 6.9-1(a) SD18 Offset Temperature drift

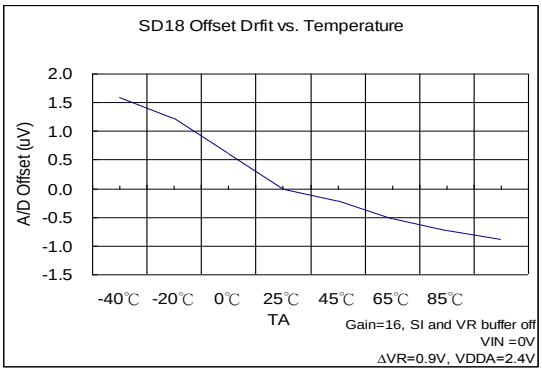


Figure 6.9-1(b) SD18 Offset Temperature drift

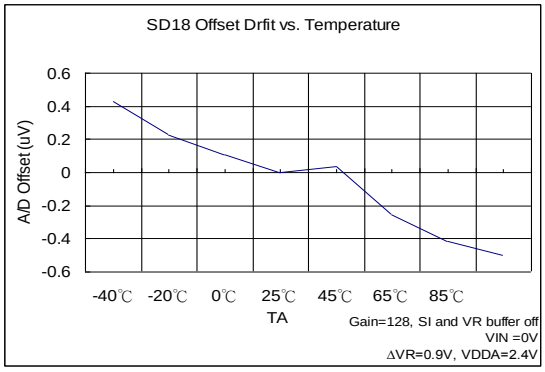


Figure 6.9-1(c) SD18 Offset Temperature drift

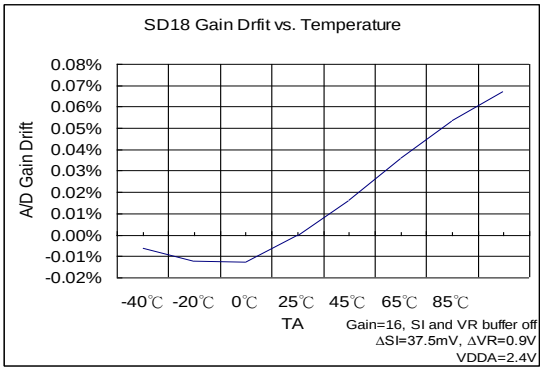


Figure 6.9-2(b) SD18 Gain drift with Temperature

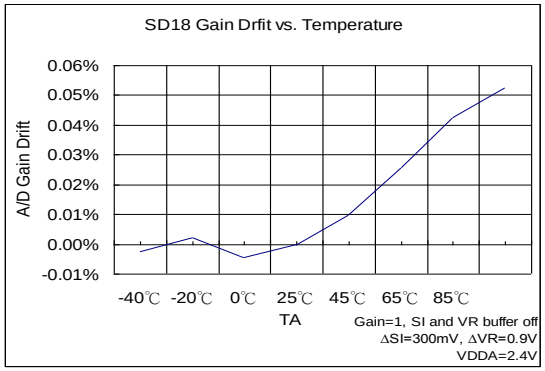


Figure 6.9-2(a) SD18 Gain drift with Temperature

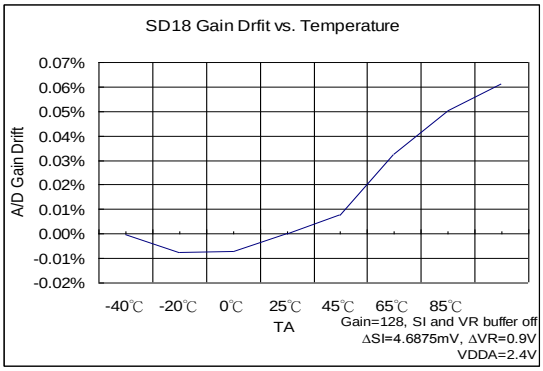


Figure 6.9-2(c) SD18 Gain drift with Temperature

2.4.4 SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P54 provides important input noise specification that aims at SD18. Table 6.9-4(a) and Table 6.9-4(b) lists out the relations of typical noise specification, gain, output rate and maximum input voltage of single end. Test conditions are external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF (1)	**OSR**					**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**									
±2400	**0.25**	**=**	**1**	**×**	**0.25**	14.43	16.07	17.20	17.86	18.29	18.66	18.98	19.13	19.30
±2160	**0.5**	**=**	**1**	**×**	**0.5**	14.34	16.05	17.13	17.84	18.26	18.62	18.90	19.13	19.27
±1080	**1**	**=**	**1**	**×**	**1**	14.38	16.06	17.11	17.72	18.13	18.53	18.88	19.05	19.22
±540	**2**	**=**	**1**	**×**	**2**	14.40	15.98	16.96	17.59	18.01	18.45	18.79	19.01	19.17
±270	**4**	**=**	**1**	**×**	**4**	14.39	15.88	16.82	17.39	17.85	18.28	18.65	18.95	19.13
±135	**8**	**=**	**1**	**×**	**8**	14.27	15.75	16.58	17.15	17.60	18.04	18.45	18.78	19.02
±68	**16**	**=**	**1**	**×**	**16**	14.14	15.51	16.18	16.73	17.21	17.70	18.15	18.52	18.83
±8	**128**	**=**	**8**	**×**	**16**	13.04	13.83	14.32	14.87	15.38	15.86	16.36	16.84	17.28

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.9-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF	**OSR**					**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**1953**	**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**									
±2400	**0.25**	**=**	**1**	**×**	**0.25**	362.92	139.77	64.33	40.65	30.04	23.35	18.70	16.75	14.92
±2160	**0.5**	**=**	**1**	**×**	**0.5**	193.22	70.82	33.83	20.60	15.37	12.00	9.86	8.38	7.61
±1080	**1**	**=**	**1**	**×**	**1**	94.14	35.38	17.16	11.17	8.40	6.34	5.01	4.44	3.92
±540	**2**	**=**	**1**	**×**	**2**	46.23	18.59	9.48	6.13	4.57	3.35	2.66	2.28	2.05
±270	**4**	**=**	**1**	**×**	**4**	23.37	9.98	5.20	3.51	2.54	1.89	1.46	1.18	1.05
±135	**8**	**=**	**1**	**×**	**8**	12.66	5.47	3.06	2.06	1.51	1.11	0.84	0.67	0.56
±68	**16**	**=**	**1**	**×**	**16**	6.93	3.23	2.02	1.38	0.99	0.70	0.51	0.40	0.32
±8	**128**	**=**	**8**	**×**	**16**	1.86	1.29	0.91	0.63	0.44	0.32	0.22	0.16	0.12

Table 6.9-4(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}(\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

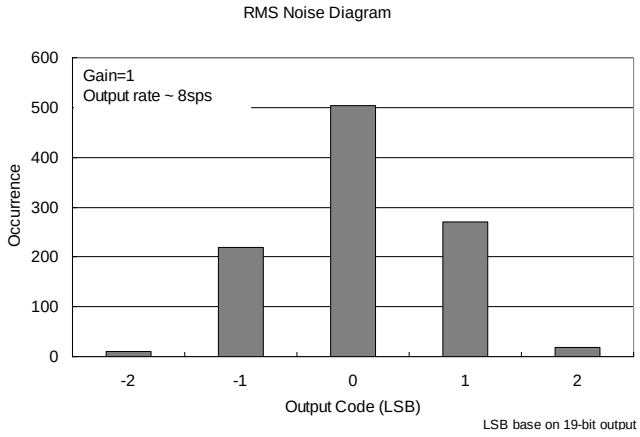


Figure 6.9-4(a) RMS Noise Diagram

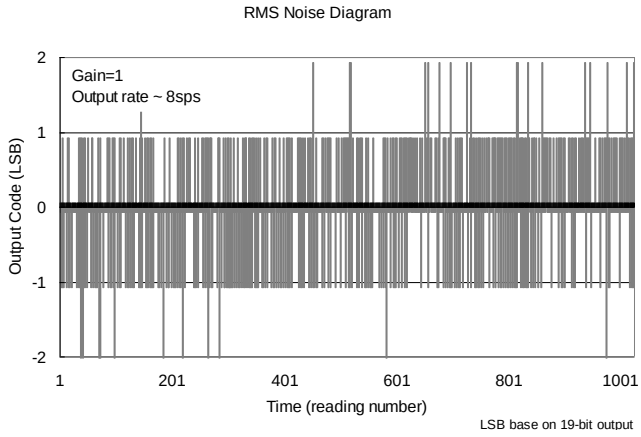


Figure 6.9-4(b) Output Code Diagram

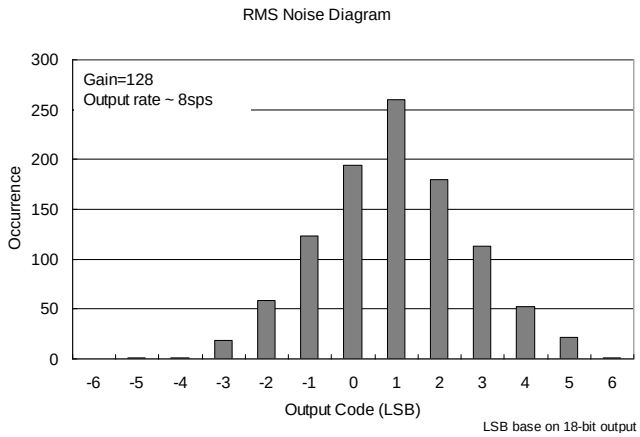


Figure 6.9-4(c) RMS Noise Diagram

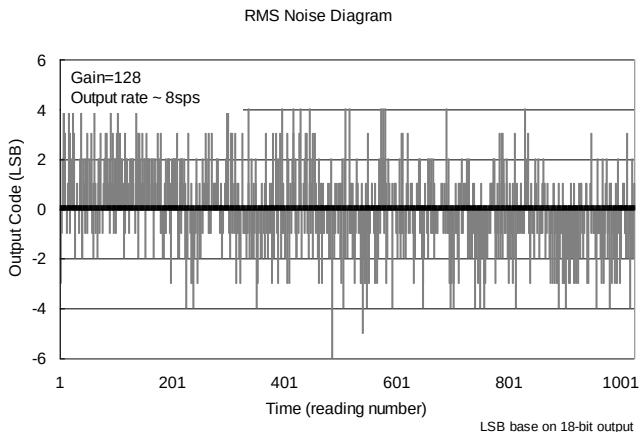


Figure 6.9-4(d) Output Code Diagram

6.10. Build-In EPROM(BIE)

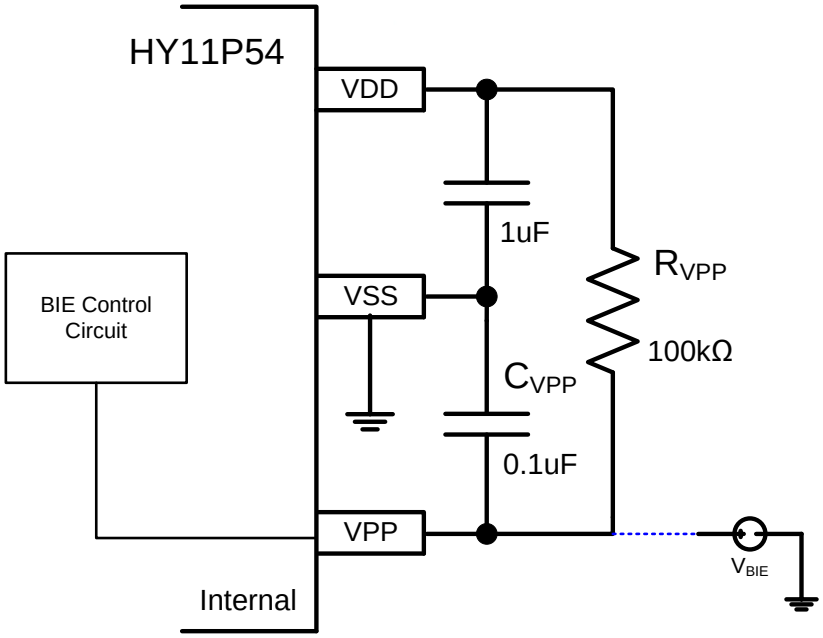
T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage			6.0	6.5	V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V
When using external VBIE power to write BIE zone, one word can be written in a time via instruction in BIE zone.						

6.11. Build-In EPROM(BIE) Low voltage control circuit

T_A=25℃, V_{DD} = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		3.05		3.4	V
V_{SS}	Supply Voltage			0		V
Starts 3.05V low programming voltage control circuit, it is not necessary to connect V_{BIE} power to program BIE zone.						



BIE typical application

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2] Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY11P54-D000	Die	-	D	000	000	-	100	Green[4]	-
HY11P54-L064	LQFP	64	L	064	000	Tray	250	Green[4]	MSL-3
HY11P54-L100	LQFP	100	L	100	000	Tray	90	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code** (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 008 and you require die shipment.
The device No. will be HY11P54-D000-008

Ex: You request blank code in die package.
The device No. will be HY11P54-D000.

Ex: You request blank code in LQFP 100 package.
The device No. will be HY11P54-L100.
And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in LQFP 100 package.The device No. will be HY11P54-L100-009.And please clearly indicate the shipment packing type when placing orders.

[2] **Code:**

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

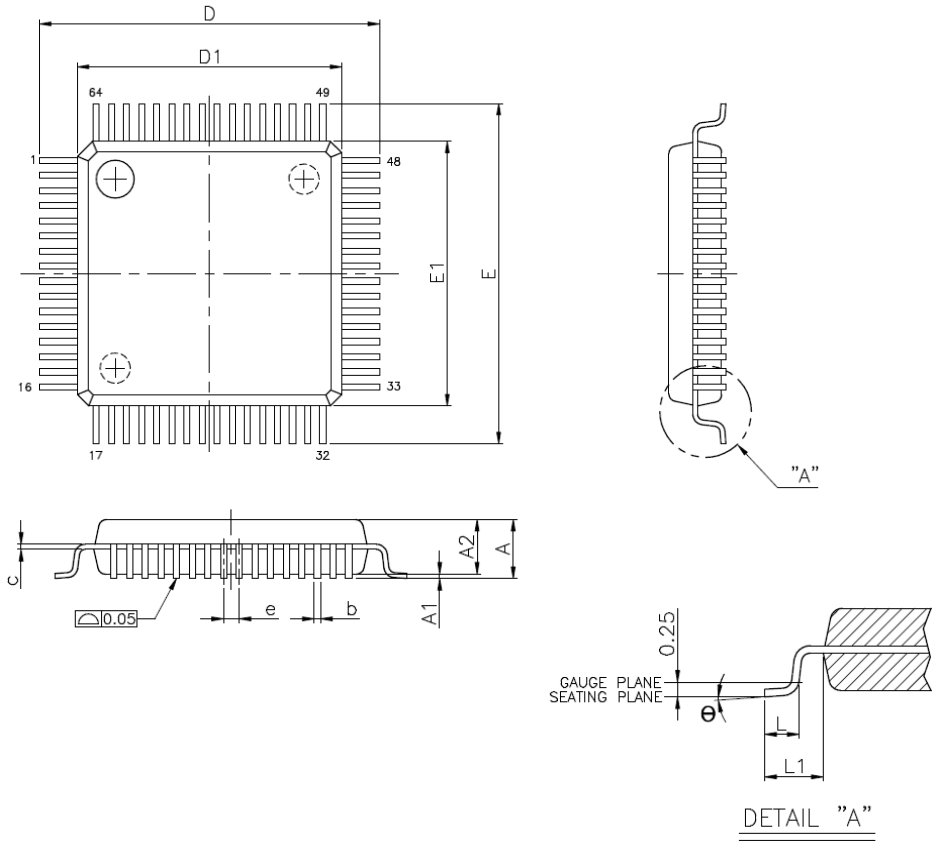
[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm).

8. Package Information

8.1. LQFP64(L064)

8.1.1. Package Dimensions LQFP64 (7x7)



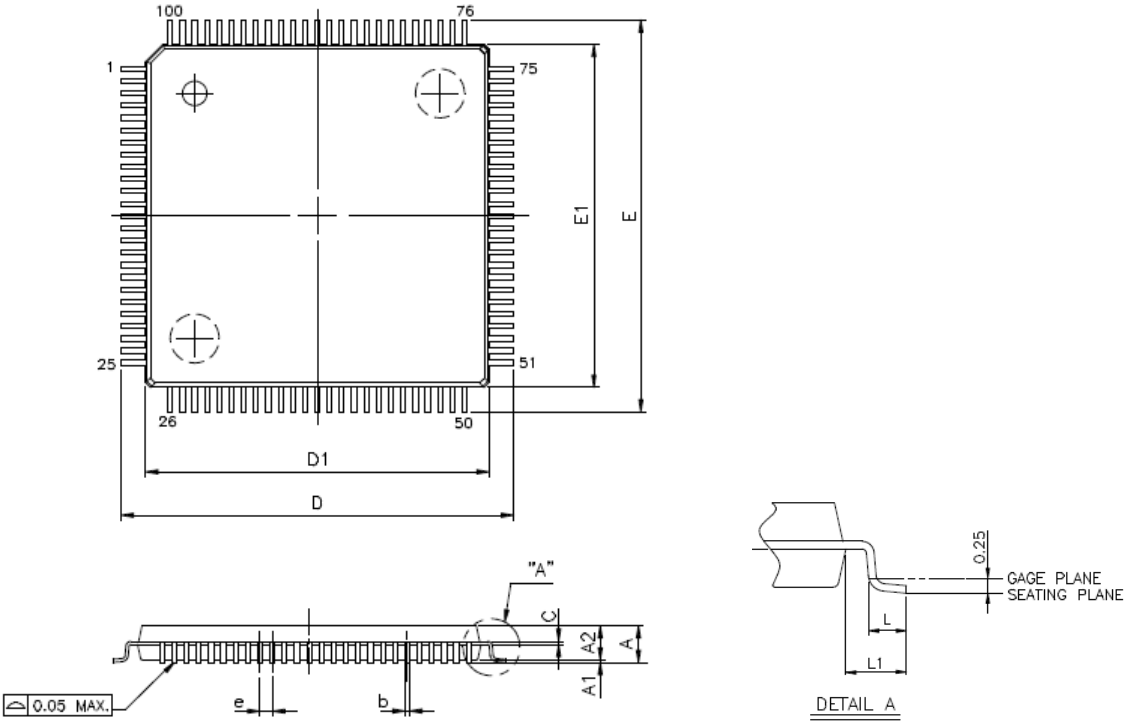
SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.

8.2. LQFP100(L100)

8.2.1. Package Dimensions LQFP100 (14x14)



SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.

9. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V06	All	First edition.
V07	3,5,35,38	QFN Series Pin Code Name Change.
V08	12	Delete HY11P54-NS48, add Package marking information.
	35	Update "MSL" and "Green" Description.
V09	8,9	Modified the function description of PT4.x and PT5.x as digital input.
	16	Modified the Figure 4-3.