HY14E10M

Datasheet

Digital Pressure Sensor Platform

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1. Features

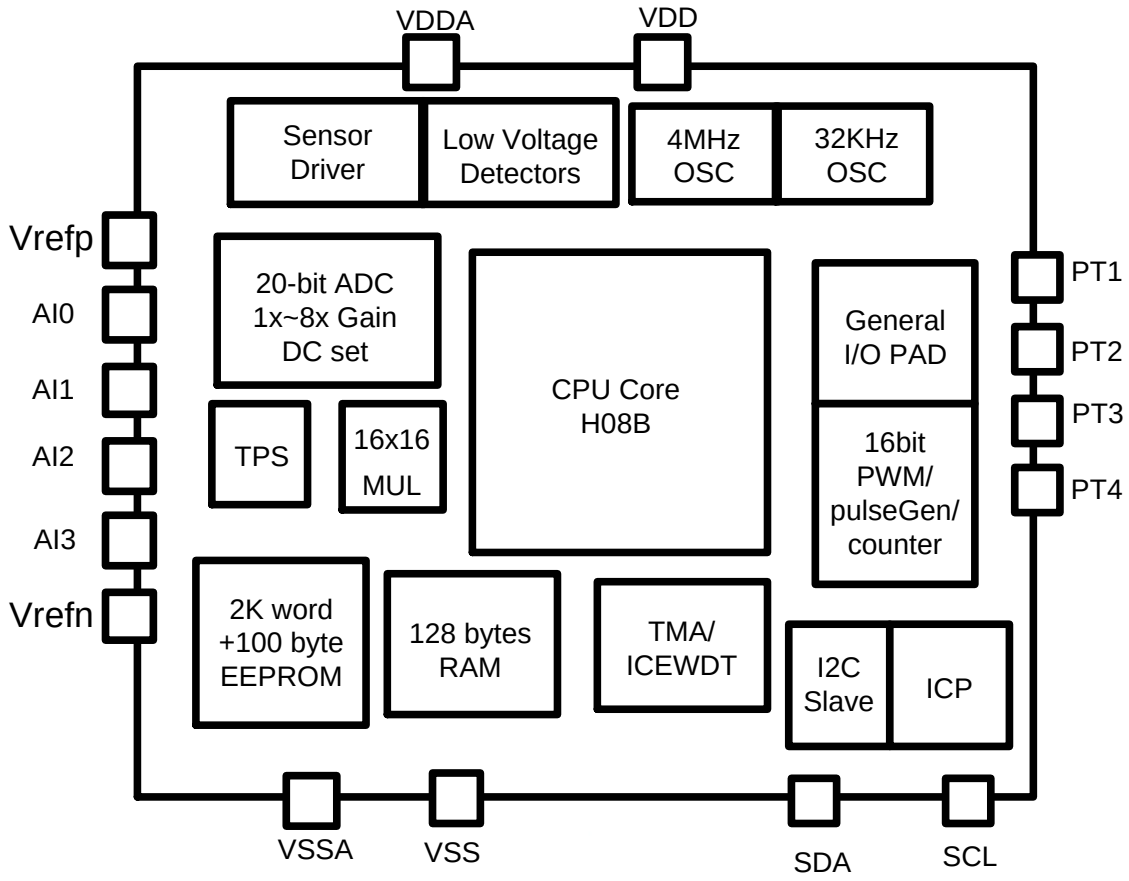
- Used as Integrated Piezo-resistive Pressure Sensors
  - Integrate a 20–Bit ADC for Voltage, and Temperature Measurements
  - Integrate a PGA for input signal amplification
- Wide operation range: 2.0 ~ 5.5V
- Integrate a 2K words EEPROM
  - In system program circuit is embedded
  - 100,000 program time
- 128 bytes SRAM
- 16x16b hardware multiplier
- Slave I2C communication port
- 4 general I/O ports (PT0/PT1 with input interrupt function)
- 16-bit PWM
- 2 wires JTAG (share with I2C) for program development
- Programmable sensor drive voltage
- Only VDD external capacitor is required
- Build-in VDDA LDO (Option)
- Two aux analog inputs
- **Wide Operating Temperature Range: -40℃~125℃**

Function List

Model No.	VDD	System Clock	Program Memory (word)	SRAM (byte)	ADC ENOB (bit x ch)	Sample Rate (sps)	TPS	I/O	Timer (bit x ch)	PWM (bit x ch)	Serial I/F	Package
HY14E10M	2.0V~ 5.5V	32KHz~ 4MHz	2K	128	19bit x 4	60~7.8K	yes	4	8-bit x 1 16-bit x 1	8-bit x 1 16-bit x 1	I^2C Slave	QFN16 SSOP16

2. Function Outline

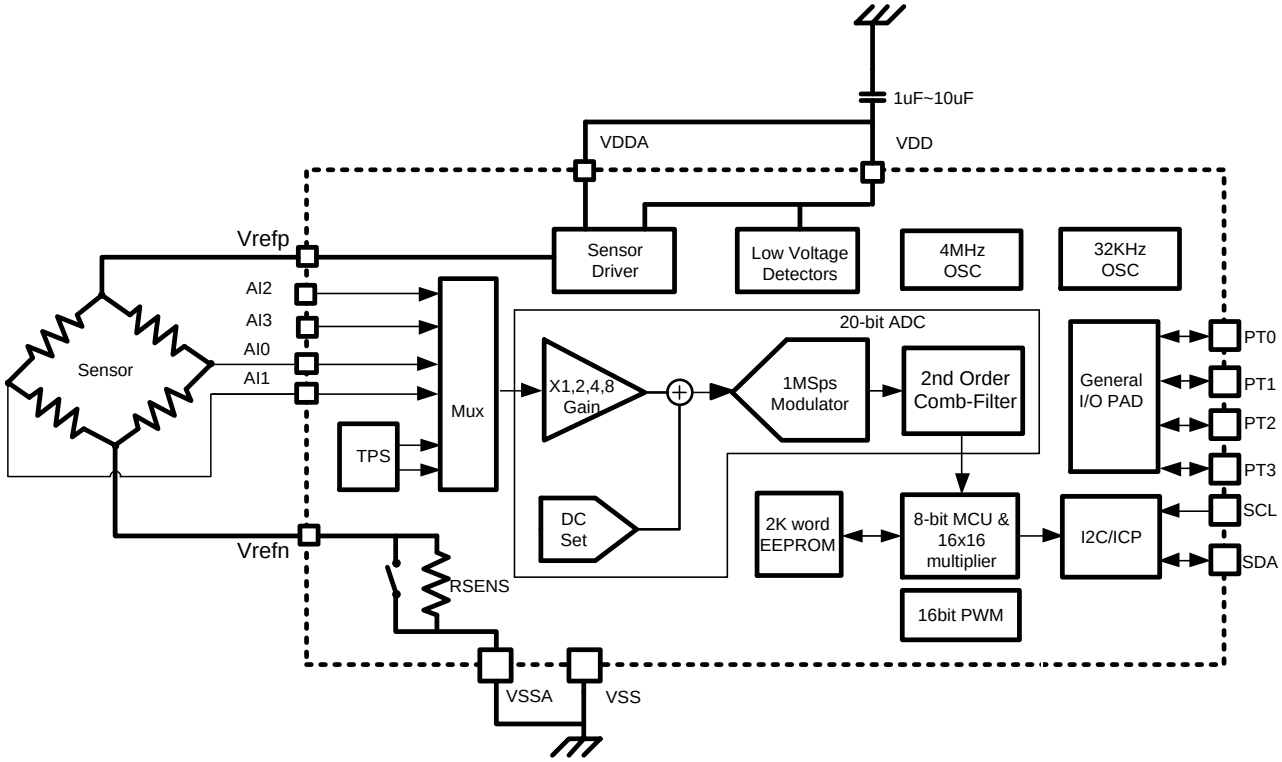
2.1. Block Diagram



Note :

Voltage amplifier ratio x1 / x2 / x4 as reservations and recommend the use of amplifiers ratio x8.

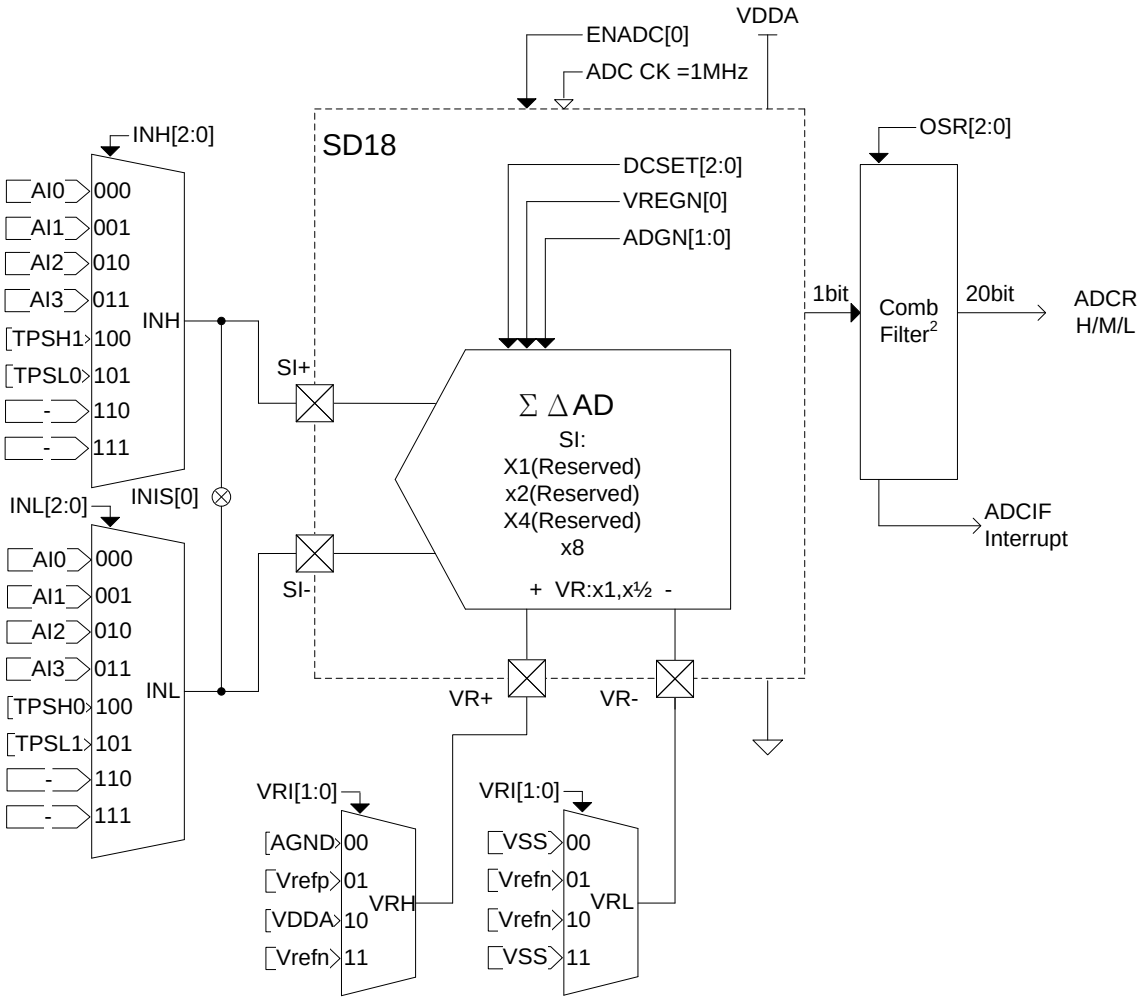
2.2. Application Circuit



Note :

Voltage amplifier ratio x1 / x2 / x4 as reservations and recommend the use of amplifiers ratio x8.

2.3. SD18 Network

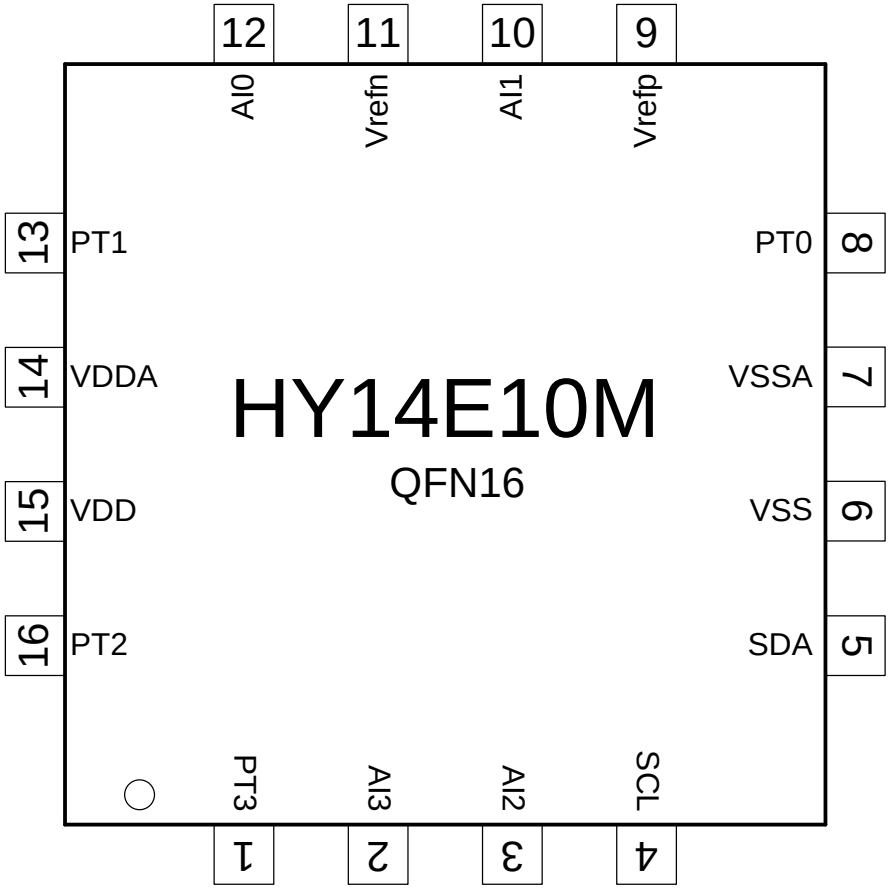


Note :

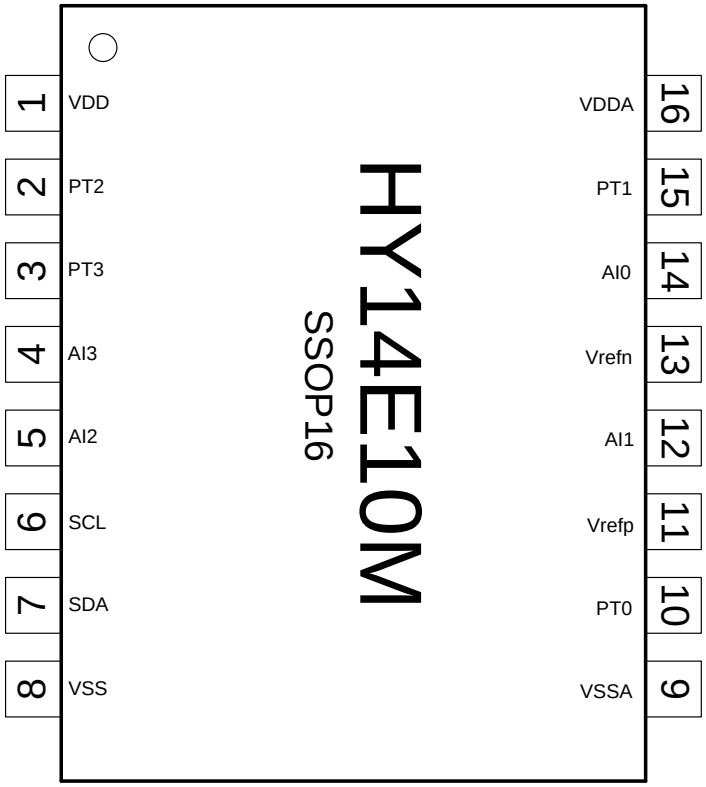
Voltage amplifier ratio x1 / x2 / x4 as reservations and recommend the use of amplifiers ratio x8.

3. Pin Definition

3.1. QFN16(N016) Diagram



3.2. SSOP16(E016) Diagram



3.3. Pinout I/O Description

N016	E016	Pin	Characteristic		Description
		Name	I/O	Type	
11	13	Vrefn	O	A	**Sense Ground.** Used to ground resistive bridge sensor.
12	14	AI0	I	A	**Sensing Input 0.** Used for analog input to ADC multiplexer
13	15	PT1	I/O	S	**Digital Input/Output Port 1** Used as general digital input or output pad. It has level change interrupt
14	16	VDDA	I	P	**Analog Power Supply.** A 2.0V ~ 5.5V voltage input. (Short with VDD by wire bonding or LDO output option)
15	1	VDD	I	P	**Power Supply.** A 2.0V ~ 5.5V voltage input. Connect a 1uF capacitor to VSS.
16	2	PT2	I/O	S	**Digital Input/Output Port 2** Used as general digital input or output pad. It has level change interrupt
1	3	PT3	I/O	S	**Digital Input/Output Port 3** Used as general digital input or output pad
2	4	AI3	I	A	**Sensing Input 3.** Used for analog input to ADC multiplexer
3	5	AI2	I	A	**Sensing Input 2.** Used for analog input to ADC multiplexer
4	6	SCL	I	C	**I2C Serial Clock Input.** Slave I2C communication clock line
5	7	SDA	I/O	D	**I2C Serial Data Input/Output** Slave I2C communication data line. Open-drain output. Use with an external pull-up resistor
6	8	VSS	I	P	**Device Ground.**
7	9	VSSA	I	P	**Device Analog Ground.**
8	10	PT0	I/O	S	**Digital Input/Output Port 0** Used as general digital input or output pad
9	11	Vrefp	O	A	**Power Supply.** Used to power resistive bridge sensor.
10	12	AI1	I	A	**Sensing Input 1.** Used for analog input to ADC multiplexer

"I/O" Input/Output, "I" Input, "O" Output, "D" Digital Open-Drain, "S" Schmitt Trigger, "C" CMOS, "P" Power, "A" Analog

4. REGISTER LIST

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
00H	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								N/A	*,*,*,*,*,*,*,*
0FH	FSR0H									x	-,-,-,- -,-,-,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV	-	-	STKPRT[2:0]			000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH	-	-	-	-	-	PC[10]	PC[9]	PC[8]	 0000	-,-,-,- *,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	*,*,*,*,*,*,*,*
1DH	TBLPTRH	TBLW+	TBLW	TBLR+	TBLR	TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	 0000	-,-,-,- *,*,*,*
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	*,*,*,*,*,*,*,*
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	*,*,*,*,*,*,*,*
23H	INTE0	GIE	ADCIE	TMBIE	TMAIE	LVD_BE	LVDE	E1IE	E0IE	000. 0000	*,*,*,*,*,*,*,*
24H	INTE1	I2CW7IE	I2CW6IE	I2CW5IE	I2CW4IE	I2CW3IE	I2CW2IE	I2CW1IE	I2CW0IE	000. 0000	*,*,*,*,*,*,*,*
25H	INTE2	-	-	-	-	-	I2CW10IE	I2CW9IE	I2CW8IE	000. 0000	*,*,*,*,*,*,*,*
26H	INTF0	-	ADCIF	TMBIF	TMAIF	LVD_BF	LVDF	E1IF	E0IF	000. 0000	w0
27H	INTF1	I2CW7IF	I2CW6IF	I2CW5IF	I2CW4IF	I2CW3IF	I2CW2IF	I2CW1IF	I2CW0IF	000. 0000	w0
28H	INTF2	-	-	-	-	-	I2CW10IF	I2CW9IF	I2CW8IF	000. 0000	w0
29H	WREG	Working Register								xxxx xxxx	*,*,*,*,*,*,*,*
2BH	STATUS	-	-	-	C	-	-	-	Z	...x xxxx	-,-,-,*,*,*,*,*
2CH	PSTATUS	BOR	PD	-	IDLE	ICP_Crst	STK_ERR	I2C_RST	I2C_GC_RST	000d .0..	rw0,rw0,rw0,rw0 -,rw0,-,-
2DH	ADCR0H	ADC[19:12]								xxxx xxxx	*,*,*,*,*,*,*,*
2EH	ADCR0M	ADC[11:4]								xxxx xxxx	*,*,*,*,*,*,*,*
2FH	ADCR0L	ADC[3:0]				0	0	0	0	xxxx xxxx	*,*,*,*,*,*,*,*
30H	ADCR1H	ADC[19]	ADC[19]	ADC[19]	ADC[19]	ADC[19]	ADC[18]	ADC[17]	ADC[16]	xxxx xxxx	*,*,*,*,*,*,*,*
31H	ADCR1M	ADC[15:8]								xxxx xxxx	*,*,*,*,*,*,*,*
32H	ADCR1L	ADC[7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
33H	PWRCN0	ENBGR	ENTPS	ENSDR	INIS	TPSLCN	ENLDO	ENLVD	ENADC	000. 0000	*,*,*,*,*,*,*,*
34H	PWRCN1	ADHV	SDRV[1:0]		LVDV[1:0]		LDOV[1:0]		LVDO	000. 0000	*,*,*,*,*,*,*,*
35H	ADCCN0	OSR[2:0]			VREGN	ADG[1:0]		SACM[1:0]		000. 0000	*,*,*,*,*,*,*,*
36H	ADCCN1	INL[2:0]			INH[2:0]			VRI[1:0]		000. 0000	*,*,*,*,*,*,*,*
37H	ADCCN2	DCSET[2:0]			TCR[1:0]		-	-	ADRST	000. 0000	*,*,*,*,*,*,*,*
38H	CLKCN	-	-	-	HAOM[1:0]		CPUCKS	ENHAO	ENLPO	000. 0011	*,*,*,*,*,*,*,*
39H	AL_MO0	LSB for multiplexer input A / LSB for multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3AH	AH_MO1	MSB for multiplexer input A / 15-8 bit multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3BH	BL_MO2	LSB for multiplexer input B / 23-16 bit multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3CH	BH_MO3	MSB for multiplexer input B / MSB for multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3DH	PT0	-	-	PT0EG[1:0]		ENPWM1O	PU0	TC0	PT0IO	000. 0000	*,*,*,*,*,*,*,*
3EH	PT1	-	-	PT1EG[1:0]		ENPWM0O	PU1	TC1	PT1IO	000. 0000	*,*,*,*,*,*,*,*
3FH	PT2	-	-	-	-	ENPWM1O	PU2	TC2	PT2IO	000. 0000	*,*,*,*,*,*,*,*
40H	PT3	-	-	-	-	ENPWM0O	PU3	TC3	PT3IO	000. 0000	*,*,*,*,*,*,*,*

Figure 4-1 HY14E10M Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
41H	LSB_SEL	SEL_FLAG[7:0]								0000 0000	********
42H	I2C_CMD	TIP	scu_L3	SP	0	0	0	0	EN_SCLO	0000 0000	RRRRRRRW
43H	I2C_O0	I2C Data Output Buffer 0								xxxx xxxx	w
44H	I2C_O1	I2C Data Output Buffer 1								xxxx xxxx	w
45H	I2C_O2	I2C Data Output Buffer 2								xxxx xxxx	w
46H	I2C_O3	I2C Data Output Buffer 3								xxxx xxxx	w
47H	I2C_O4	I2C Data Output Buffer 4								xxxx xxxx	w
48H	I2C_O5	I2C Data Output Buffer 5								xxxx xxxx	w
49H	I2C_O6	I2C Data Output Buffer 6								xxxx xxxx	w
4AH	I2C_O7	I2C Data Output Buffer 7								xxxx xxxx	w
4BH	I2C_I0	I2C Data Intput Buffer 0								xxxx xxxx	r
4CH	I2C_I1	I2C Data Intput Buffer 1								xxxx xxxx	r
4DH	I2C_I2	I2C Data Intput Buffer 2								xxxx xxxx	r
4EH	I2C_I3	I2C Data Intput Buffer 3								xxxx xxxx	r
4FH	I2C_I4	I2C Data Intput Buffer 4								xxxx xxxx	r
50H	I2C_I5	I2C Data Intput Buffer 5								xxxx xxxx	r
51H	I2C_I6	I2C Data Intput Buffer 6								xxxx xxxx	r
52H	I2C_I7	I2C Data Intput Buffer 7								xxxx xxxx	r
53H	I2C_I8	I2C Data Intput Buffer 8								xxxx xxxx	r
54H	I2C_I9	I2C Data Intput Buffer 9								xxxx xxxx	r
55H	I2C_I10	I2C Data Intput Buffer 10								xxxx xxxx	r
56H	TMACN	ENTMA	TMACL	TMAS	DTMA[2:0]			-	-	0000 $000	*,*,*,* rw1,*,*,*
57H	TMAR	TMAR[7:0]								0000 0000	r,r,r,r r,r,r,r
58H	TB1CN0	ENTMB	TB1M[1:0]		DTMB[1:0]		-	-	TMBCL	0000 0000	*,*,*,*,*,*,*,*
59H	TB1C0L	TimerB1 counter Condition Register0 [7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
5AH	TB1C0H	TimerB1 counter Condition Register0 [15:8]								xxxx xxxx	*,*,*,*,*,*,*,*
5BH	TB1C1L	TimerB1 counter Condition Register1 [7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
5CH	TB1C1H	TimerB1 counter Condition Register1 [15:8]								xxxx xxxx	*,*,*,*,*,*,*,*
5EH	EE_CTRL	EN_TBL	PGM	0	0	0	0	0	0		0,1,1,1,1,1,0,0
80H ~ FFH	GPR0	General Purpose Register as 128Byte								xxxx xxxx	

Figure 4-2 HY14E10M Register List (continued)

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD to VSS(VSSA) ..... −0.3 V to 6.5 V

Voltage applied at VDDA to VSS(VSSA) ..... −0.3 V to V_{DD} + 0.3 V

Voltage applied to any pin ..... −0.3 V to V_{DD} + 0.3 V

Storage temperature range, Tstg: (unprogrammed device) ..... −55℃ to 150℃

(programmed device)..... −40℃ to 85℃

Operating temperature range ..... −40℃ to 125℃

5.2. Power System

Typical values are at TA = 25℃ and VDD = 3.0V.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		2.0		5.5	V
SDR	Temperature drift	VDD=VDDA=3.6V, TA=-−40℃~125℃		100		ppm/C
	Driving Current	VDD – Vs > 0.15			1000	uA
	Sensor Drive Voltage	SDRV[1:0]=00	1.50	1.65	1.80	V
		SDRV[1:0]=01	2.05	2.20	2.35	
		SDRV[1:0]=10	2.65	2.80	2.95	
		SDRV[1:0]=11	3.65	3.80	3.95	
RSENS	Internal Resistance for sensor	RSENS=00b, 0.0 Kohm		0		Kohm
		RSENS =01b, 2.5 Kohm	2.25	2.5	2.75	
		RSENS =01b, 5.0 Kohm	4.5	5	5.5	
		RSENS =01b, 7.5 Kohm	6.75	7.5	8.25	
	Temperature drift	RSENS =01b, 2.5 Kohm			400	ppm/C
VDDA LDO	Current	VDDA = 1.65		12		uA
	Temperature drift	VDD=3.6V, TA=-−40℃~125℃		100		ppm/C
	C load		100		10,000	nF
	R load			10K		KOhm
	VDDA LDO Voltage	LDOV[1:0]=01	2.15	2.30	2.45	V
		LDOV[1:0]=10	2.75	2.90	3.05	
		LDOV[1:0]=11	3.65	3.80	3.95	

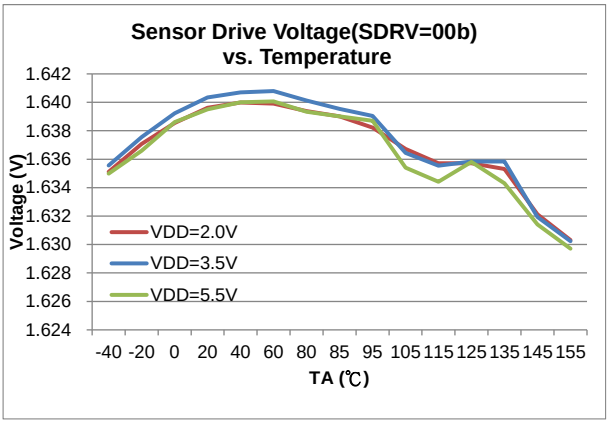


Figure 5.2-1(a) SDR vs. Temperature

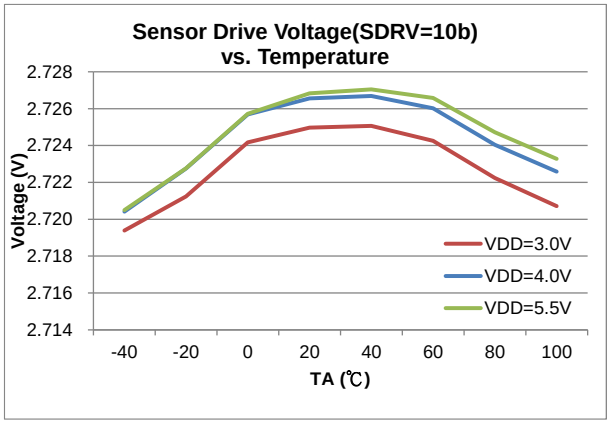


Figure 5.2-1(c) SDR vs. Temperature

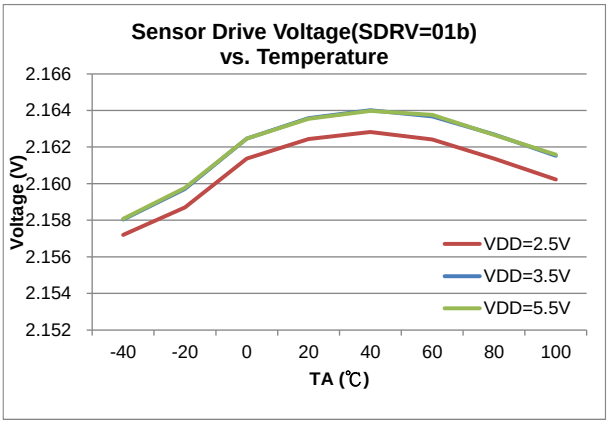


Figure 5.2-1(b) SDR vs. Temperature

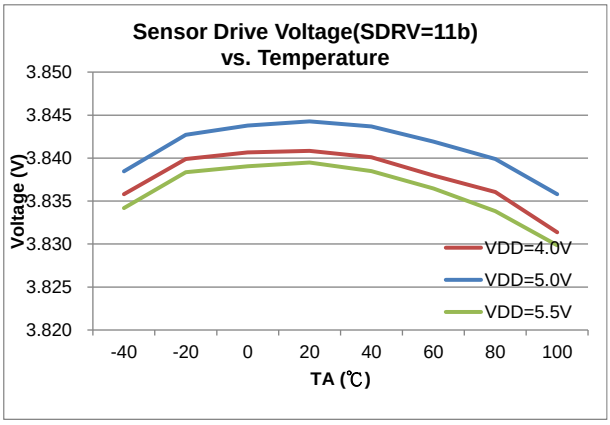


Figure 5.2-1(d) SDR vs. Temperature

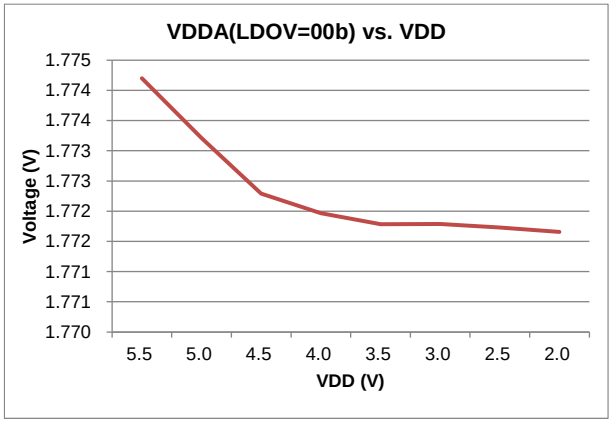


Figure 5.2-2(a) VDDA vs. VDD

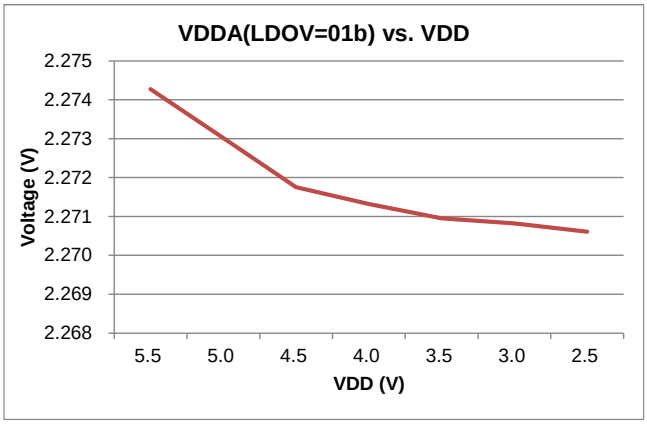


Figure 5.2-2(b) VDDA vs. VDD

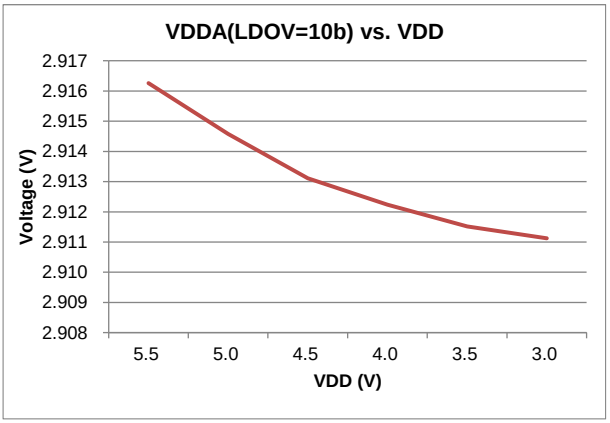


Figure 5.2-2(c) VDDA vs. VDD

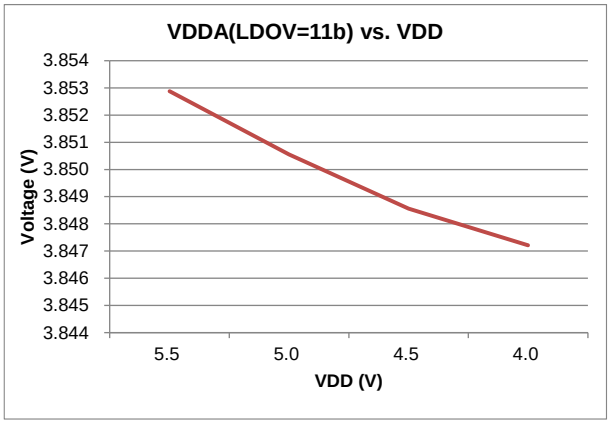


Figure 5.2-2(d) VDDA vs. VDD

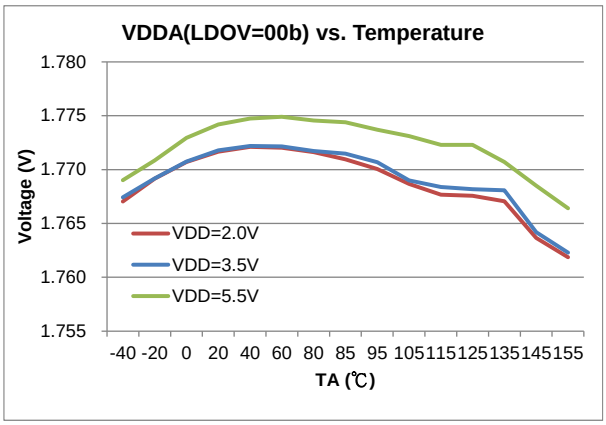


Figure 5.2-3(a) VDDA vs. Temperature

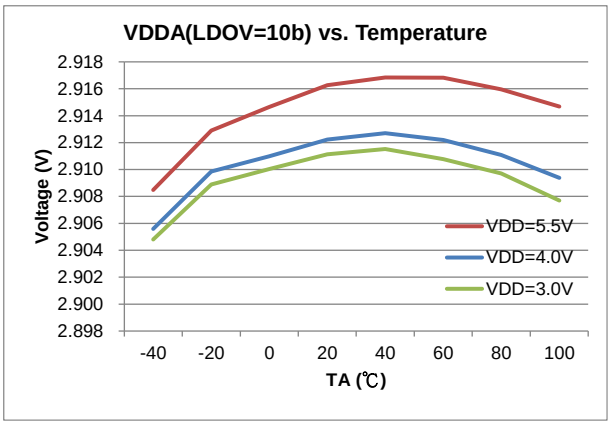


Figure 5.2-3(c) VDDA vs. Temperature

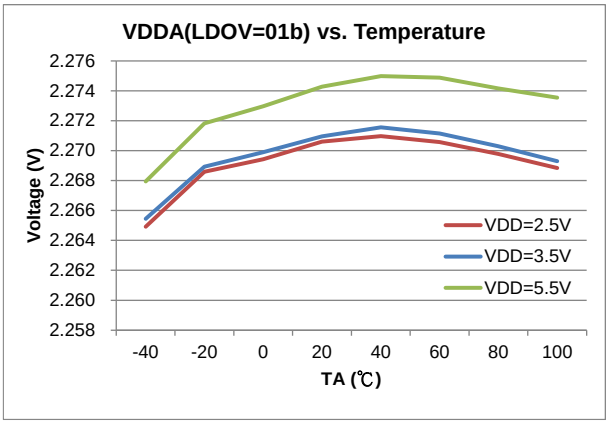


Figure 5.2-3(b) VDDA vs. Temperature

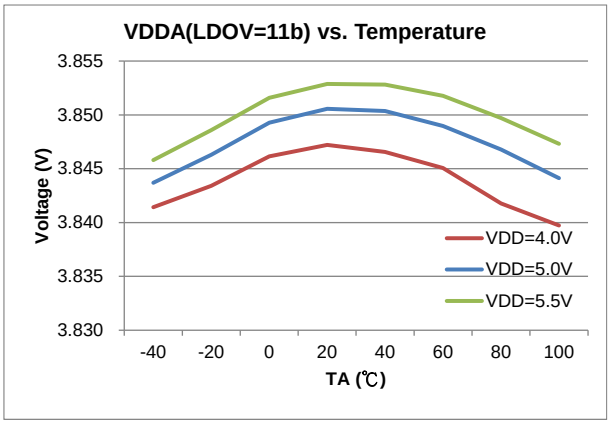


Figure 5.2-3(d) VDDA vs. Temperature

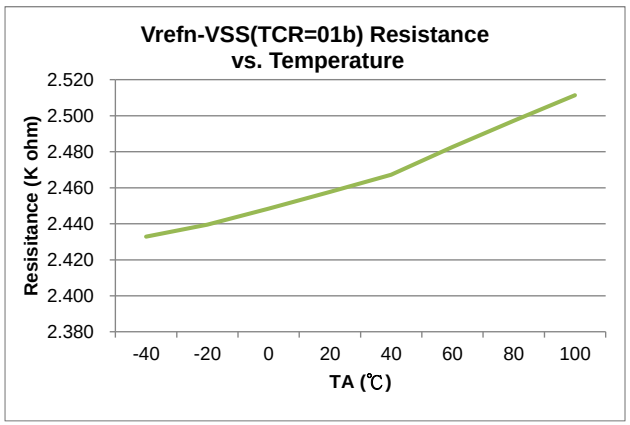


Figure 5.2-4(a) Vrefn resistance vs. Temperature

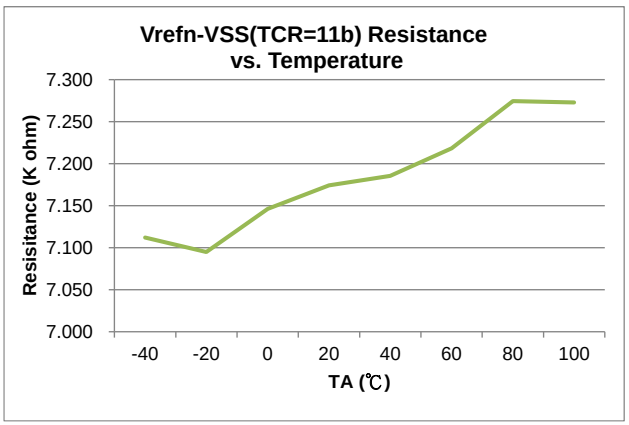


Figure 5.2-4(c) Vrefn resistance vs. Temperature

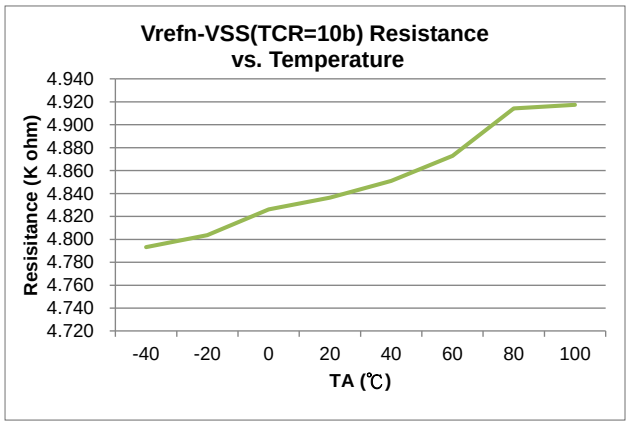


Figure 5.2-4(b) Vrefn resistance vs. Temperature

5.3. ΣΔADC, Power Supply and recommended operating conditions

Typical values are at TA = 25℃ and VDD = 3.0V

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
	Input Range	Vr = Vrefp –Vrefn Gain = AD Gain x Ref Gain	- 0.8Vr/Gain		+ 0.8Vr/Gain	V
	Resolution	Total gain = 8		20		bit
	INL	OSR = 16384		±0.003	±0.01	%FSR
	Gain drift	VDD=VDDA=3.6V, OSR = 16384, Gain=8, ADC VR=external 2.048V/2. TA=-−40℃~125℃		30		ppm/C
		VDD=VDDA=3.6V, OSR = 16384, Gain=8, ADC VR=internal AGND/1. TA=-−40℃~125℃		50		ppm/C
	Offset drift	VDD=VDDA=3.6V, OSR = 16384, Gain=8			1	%FSR
	Noise	Gain= 8 @ 8192 Gain=8 @ 128		1 15		uV
	Current		-		350	uA
	Offset		-	0.2	1	mV
	Sampling Rate		0.9	1	1.1	MS/s
	Input Gain		-	-	8	V/V
	ADC DC input shift	Vref = Vrefp – Vrefn		Vref/(4*gain)		V

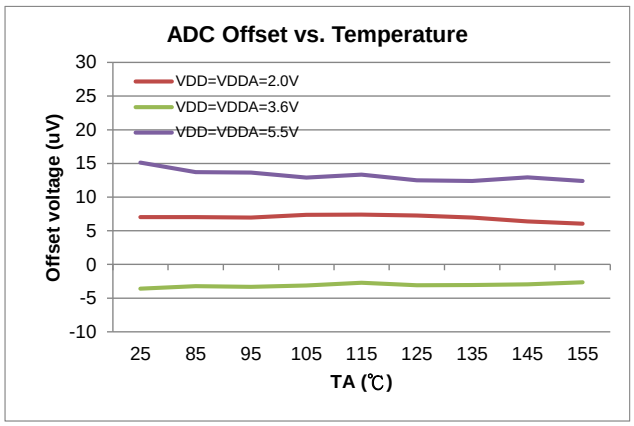


Figure 5.3-1 ADC Offset vs. Temperature

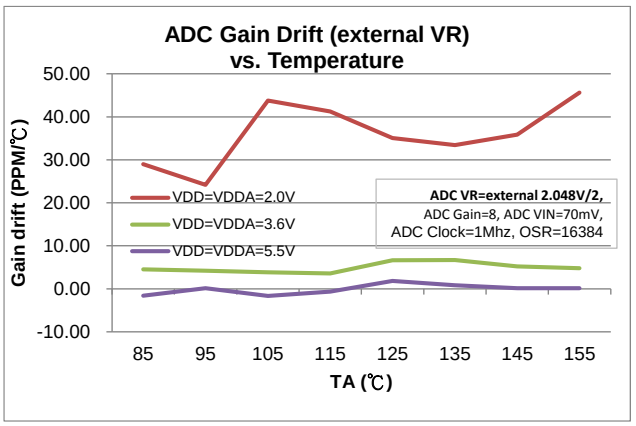


Figure 5.3-2 ADC Gain drift vs. Temperature

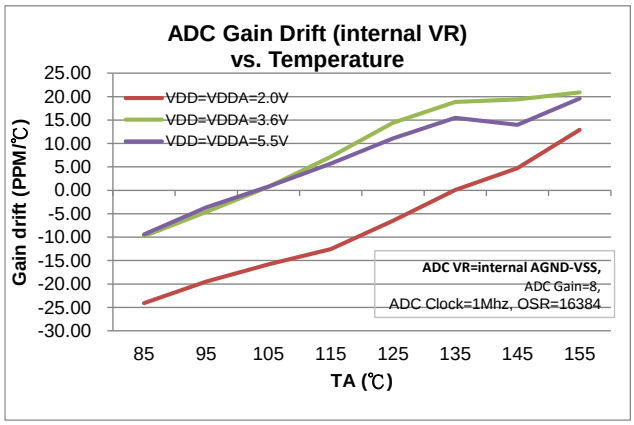


Figure 5.3-3 ADC Gain drift vs. Temperature

5.4. Temperature sensor

Typical values are at TA = 25℃ and VDD = 3.0V.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
	Resolution	After 2 points calculation; Monotonic	-	0.01	-	°C
	Temperature Sensor Slope		-	121	-	uV/℃
	Relative accuracy		+1	-	-1	uV/℃
KT	Absolute Temperature Scale 0°K					°C

5.5. Reset(Brownout, Low Voltage Detect)

Typical values are at TA = 25℃ and VDD = 3.0V.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
LVD	Current	Including R		7.5		uA
	Temperature drift	TA=-−40℃~85℃		100		ppm/C
	Low Voltage Detection	LVDV[1:0]=01	2.15	2.30	2.45	V
		LVDV[1:0]=10	2.75	2.90	3.05	
		LVDV[1:0]=11	3.65	3.80	3.95	
BOR	Detect Voltage		1.4	1.6	1.8	V
	Current			1	3	uA

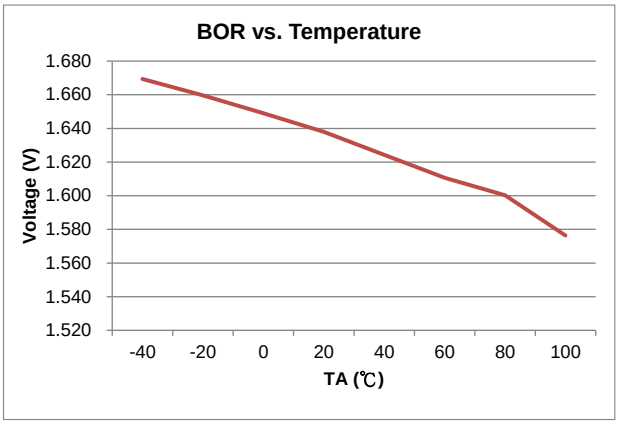


Figure 5.5-1 BOR vs. Temperature

5.6. Internal RC Oscillator

Typical values are at TA = 25℃ and VDD = 3.0V.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
LPO	Low Power Oscillator frequency	VDD=2.0~5.5V, TA=−40℃~125℃	27.2	32	40.0	KHz
	Temperature drift	VDD=3.6V, TA=−40℃~125℃		200		ppm/C
	Current			1.5		uA
HAO	High Speed Oscillator frequency	VDD=2.0~5.5V, TA=−40℃~85℃	3.92	4	4.08	MHz
		VDD=2.0~5.5V, TA=−40℃~125℃	3.60	4	4.40	
	Current			25		uA
	Temperature drift	VDD=3.6V, TA=−40℃~125℃		300		ppm/C

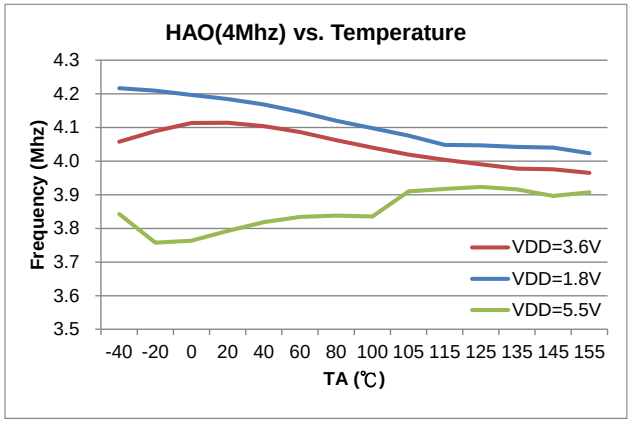


Figure 5.6-1 4Mhz HAO Frequency vs. Temperature

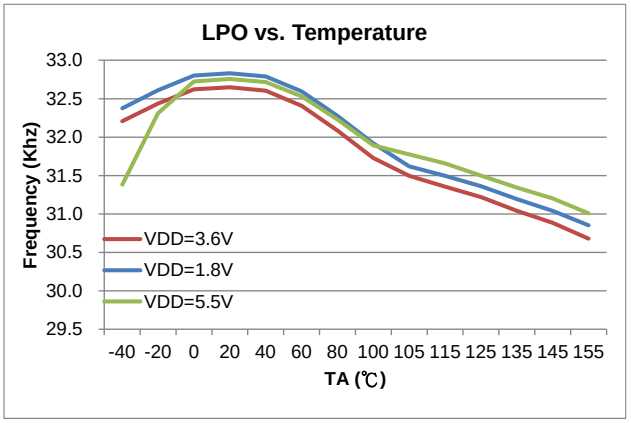


Figure 5.6-2 LPO Frequency vs. Temperature

5.7. Supply Current

TA = 25℃,VDD = 3.6V,OSC_LPO = 32KHz,unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
IAM	Active mode	OSC_HAO = 4MHz, CPU_CK = 4MHz		800		uA
ILP1	Low power mode 1	OSC_HAO = off, CPU_CK = LPO		6.5		uA
ILP2	Low power mode 2	OSC_HAO = off, CPU_CK = LPO, idle mode		1.65		uA
ILP3	Low power mode 3	OSC_HAO = off, CPU_CK = off, sleep mode		0.7		uA

TA = 25℃,VDD = 5.5V,OSC_LPO = 32KHz,unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
IAM	Active mode	OSC_HAO = 4MHz, CPU_CK = 4MHz		1100	2000	uA
ILP1	Low power mode 1	OSC_HAO = off, CPU_CK = LPO		11	25	uA
ILP2	Low power mode 2	OSC_HAO = off, CPU_CK = LPO, idle mode		2.5	6	uA
ILP3	Low power mode 3	OSC_HAO = off, CPU_CK = off, sleep mode		1	3	uA

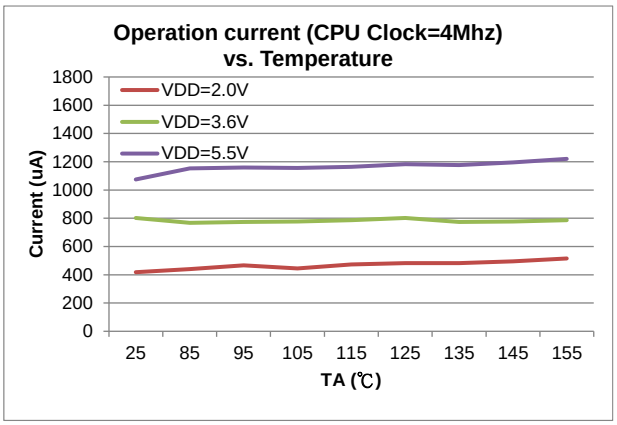


Figure 5.7-1 IAM vs. Temperature

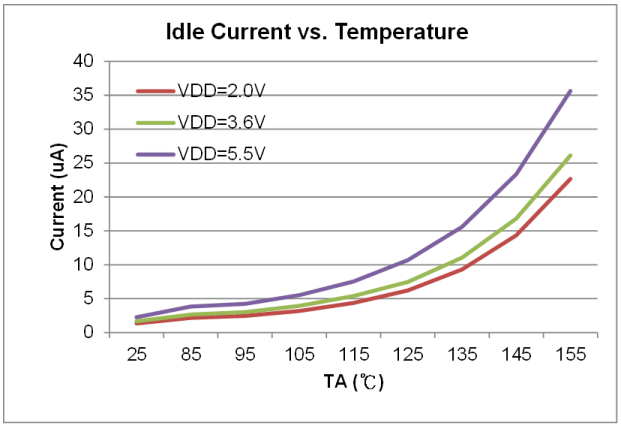


Figure 5.7-3 LP2 vs. Temperature

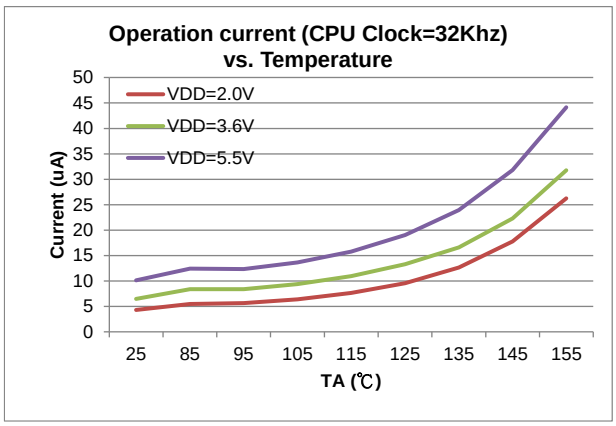


Figure 5.7-2 LP1 vs. Temperature

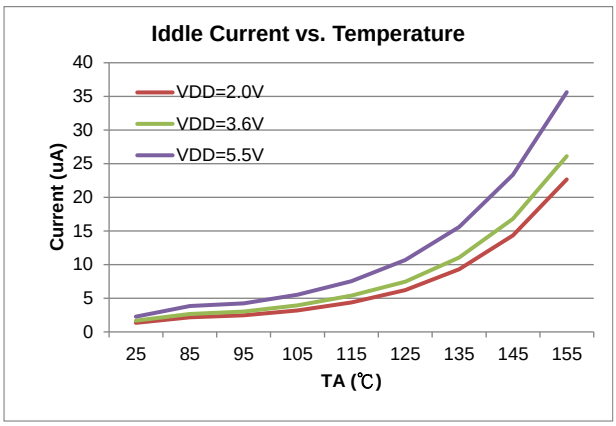


Figure 5.7-5 LPO IP current vs. Temperature

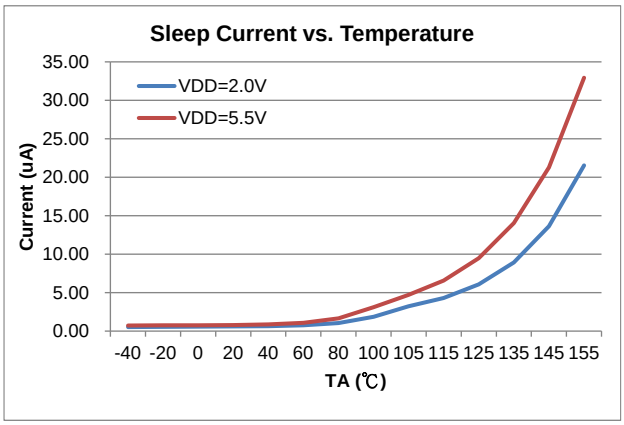


Figure 5.7-4 ILP3 vs. Temperature

5.8. Port

Typical values are at TA = 25℃ and VDD = 3.0V.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I²C	I²C interface speed				1	MHz
	SDA Output logic low (Open-drain)	IOL = 3mA	-	-	VDD X 0.2	V
	SDA, Output logic high	IOH = -50μA	VDD X 0.9	-	-	V
	SDA, SCL Input logic low		-	-	VDD X 0.2	V
	SDA, SCL Input logic high		VDD X 0.8	-	-	V
	SDA, SCL Digital input hysteresis		-	0.4	-	V
I/O	Sink	VDD = 3V, I/O= 0.3V	5			mA
	Source	VDD = 3V, I/O= 2.7V	5			mA
	Input H	VDD = 3V	1.6			V
	Input L	VDD = 3V			1.3	V

5.9. ΣΔADC Performance

HY14E10M for SD18 provide important input noise specifications. Table5.9-1 lists typical noise specification sheet and Gain, Output rate, and the largest single-ended input voltage relationship. Test conditions were set at the external input signal is a short circuit, a reference voltage (Vrefp-Vrefn) / 2, and 1024 records were sampled.

HY14E10M ENOB(RMS) with OSR/GAIN at A/D Clock=1Mhz, VR=(Vrefp-Vrefn)/2										
Max. Vin(mV) =0.9*VREF (1)	**OSR**			**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**
	Output rate(HZ)			**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**
	VDD	**GAIN**	**SDR**								
±157	**3.3**	**8**	**2.8**	14.3	15.9	16.3	16.4	16.4	17.1	17.3	18.7
HY14E10M RMS Noise(uV) with OSR/GAIN at A/D Clock=1Mhz, VR=(Vrefp-Vrefn)/2										
Max. Vin(mV) =0.9*VREF (1)	**OSR**			**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**
	Output rate(HZ)			**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**
	VDD	**GAIN**	**SDR**								
±157	**3.3**	**8**	**2.8**	16.8	5.7	4.2	4.1	4.1	2.4	2.1	0.8

Table5.9-1 SD18 ENOB and RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

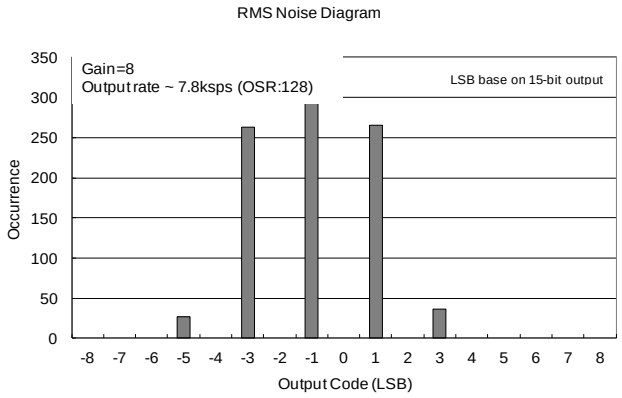


Figure5.9-1(a) RMS Noise Diagram

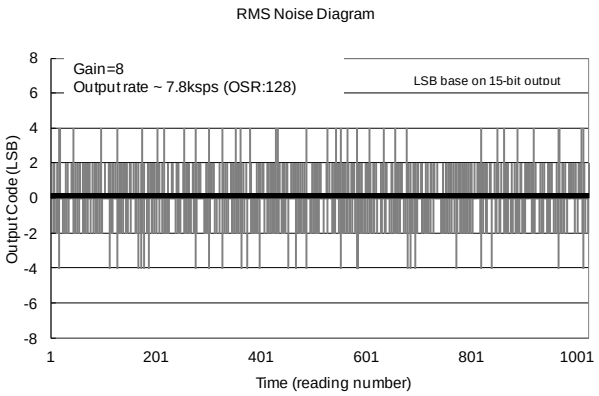


Figure5.9-1(b) Output Code Diagram

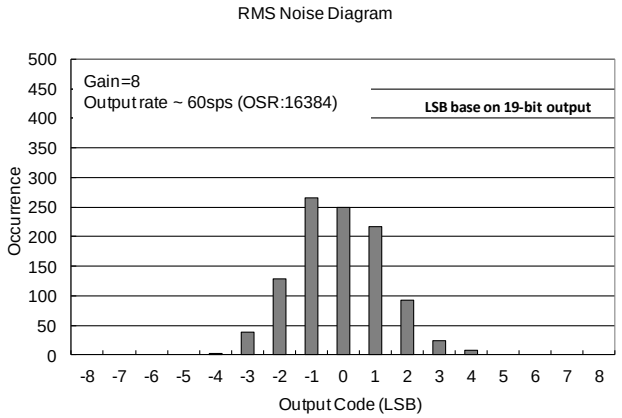


Figure5.9-2(a) RMS Noise Diagram

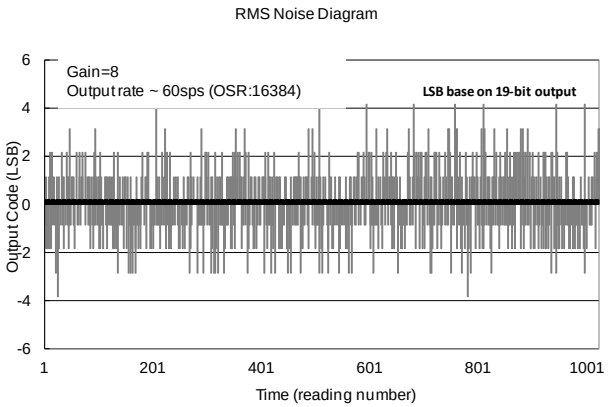


Figure5.9-2(b) Output Code Diagram

6. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY14E10M-D000	Die	-	D	000	000	-	250	Green4	-
HY14E10M-E016	SSOP	16	E	016	000	Tube	100	Green4	MSL-3
HY14E10M-E016	SSOP	16	E	016	000	Tape & Reel	2500	Green4	MSL-3
HY14E10M-N016	QFN	16	N	016	000	Tape & Reel	3000	Green4	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code (Blank Code/ Standard/Customized Programming Code)**

Ex: Your customized programming code is 007 and you require die shipment. The device No. will be HY14E10M-D000-007

Ex: You request blank code in die package. The device No. will be HY14E10M-D000

Ex: You request blank code in SSOP16 package. The device No. will be HY14E10M-E016 And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in QFN16 package. The device No. will be HY14E10M-N016-009.And please clearly indicate the shipment packing type when placing orders.

[2] **Code:**

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

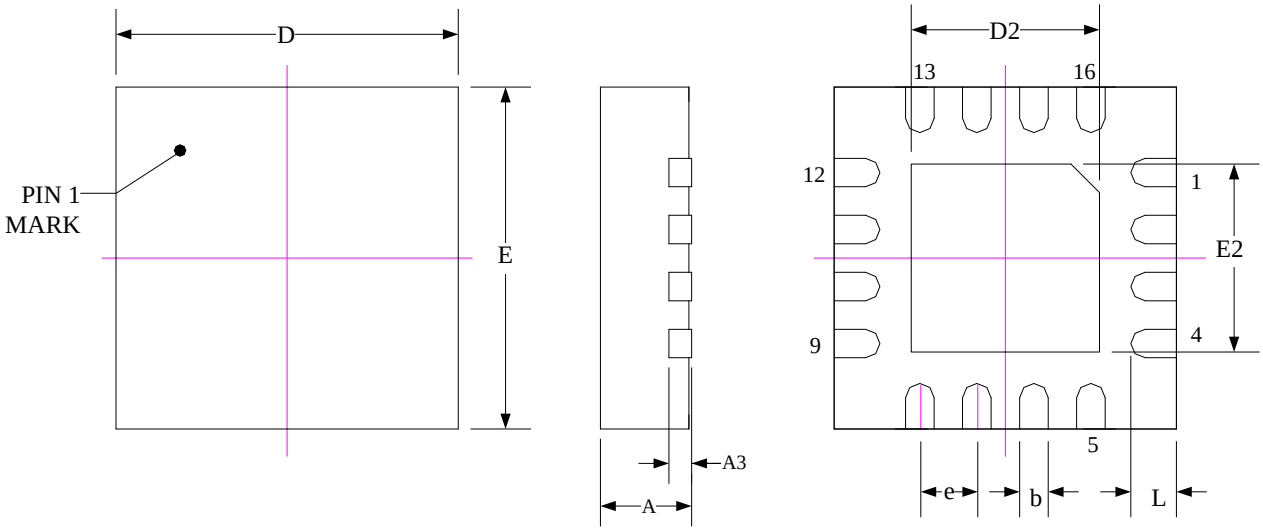
[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that are compliant with RoHS directive, SVHC under REACH and Halogen free.

7. Packaging Information

7.1. QFN16(N016)

7.1.1. Package Outline Drawing QFN16(3x3x0.75)

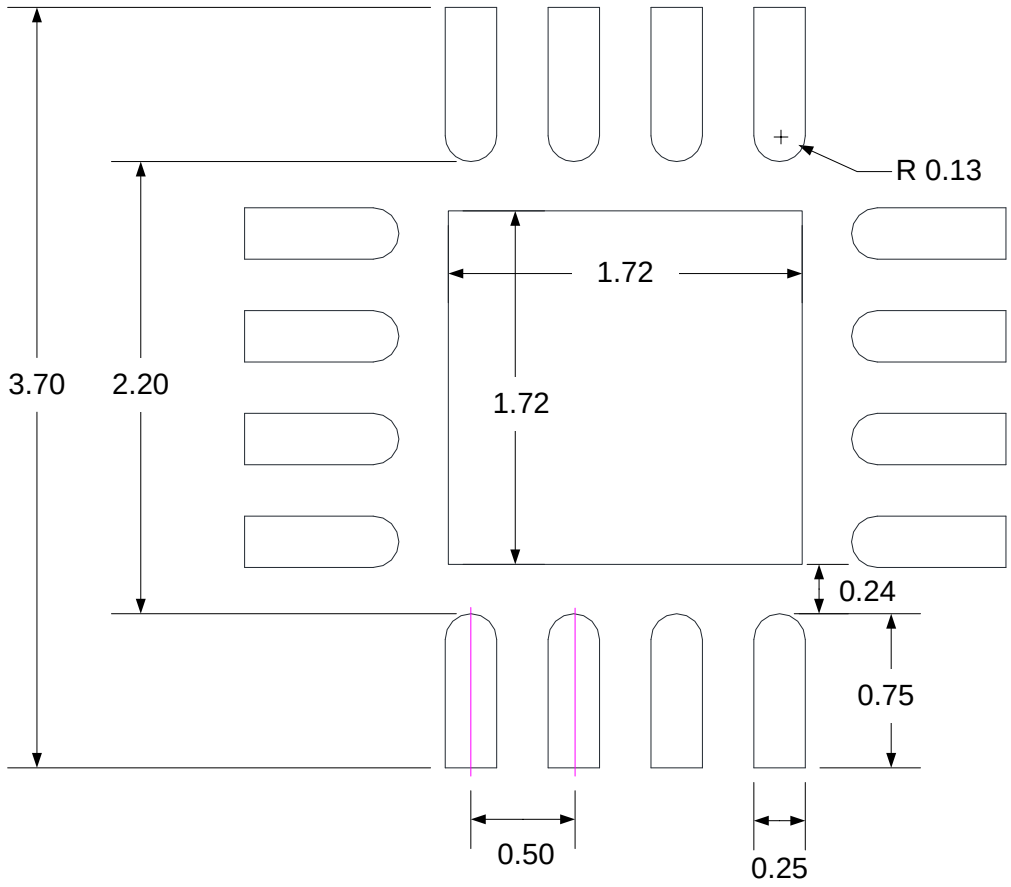


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.925	3.000	3.075
E	2.925	3.000	3.075
D2	1.625	1.725	1.825
E2	1.625	1.725	1.825
L	0.30	0.35	0.40
e	0.50 BASIC		

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Unit : mm
3. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB_EN.pdf

7.1.2. Land Pattern Design Recommendations QFN16(3x3x0.75)

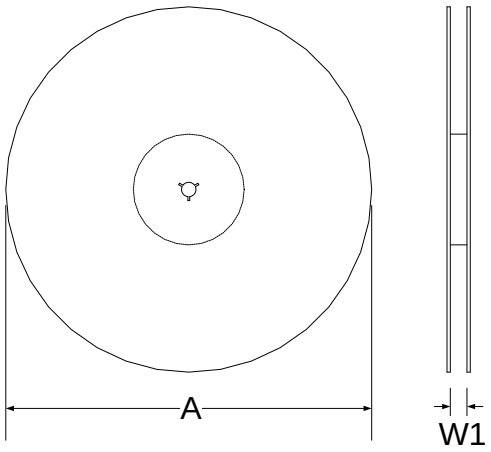


Note:

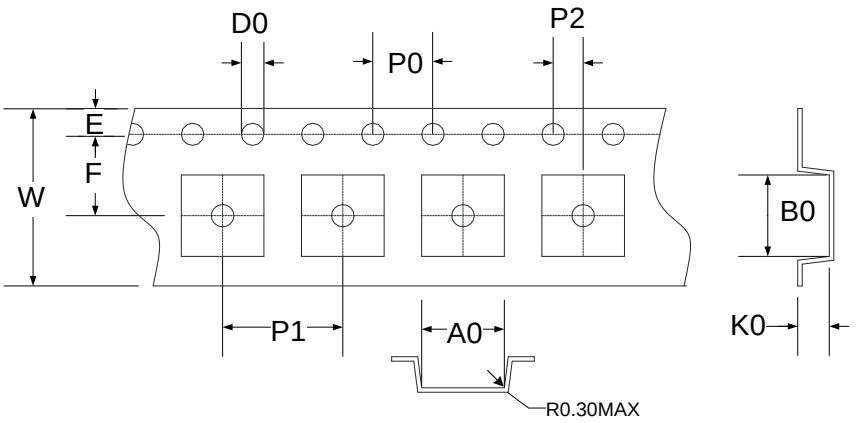
1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm
3. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB_EN.pdf

7.1.3. Tape & Reel Information QFN16(3x3x0.75)

1. Reel Dimensions



2. Carrier Tape Dimensions

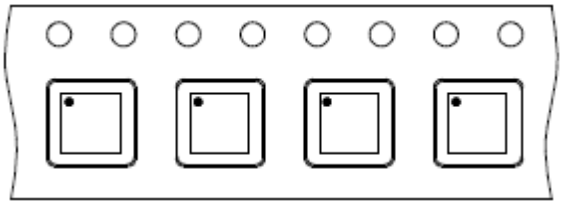


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	3.30	3.30	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

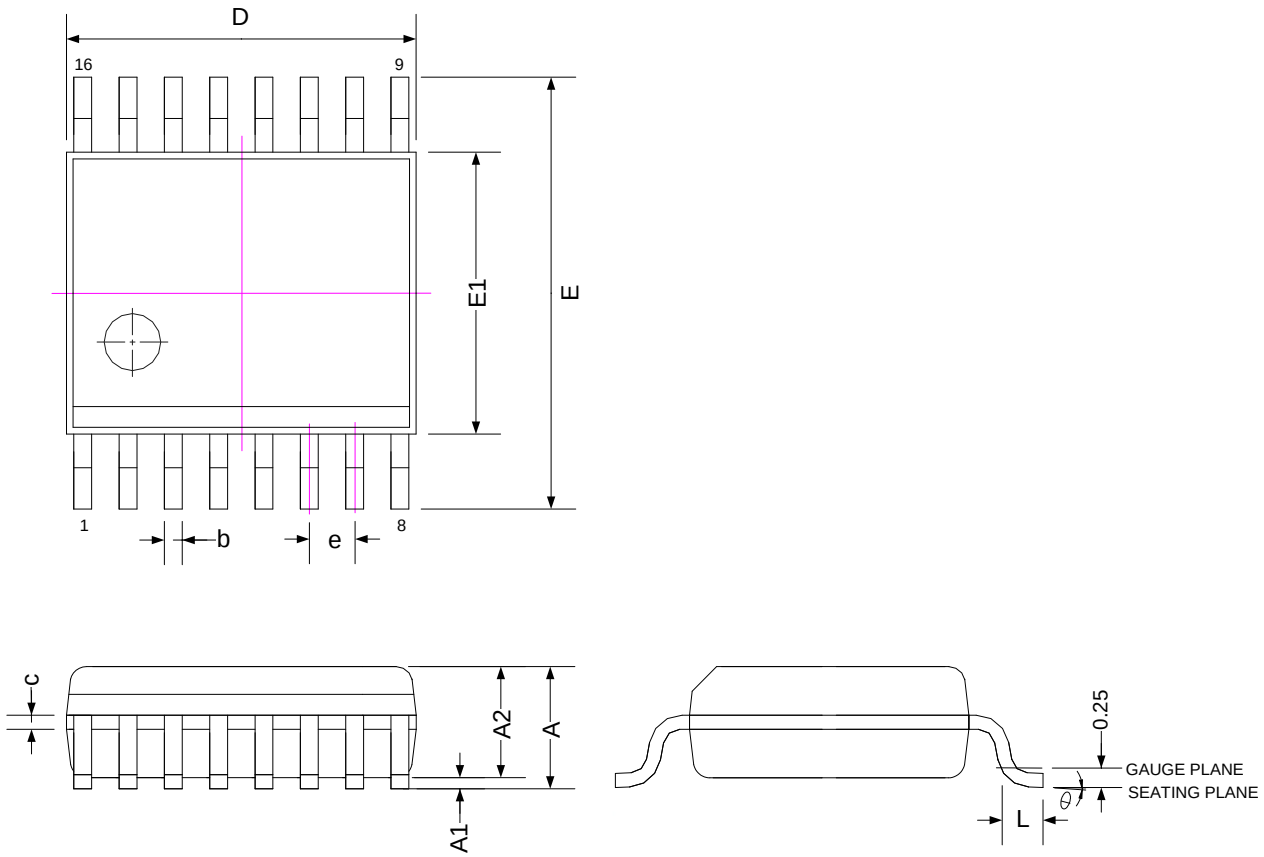
Unit: mm

3. Pin1 direction



7.2. SSOP16(E016)

7.2.1. Package Outline Drawing SSOP16(150mil)

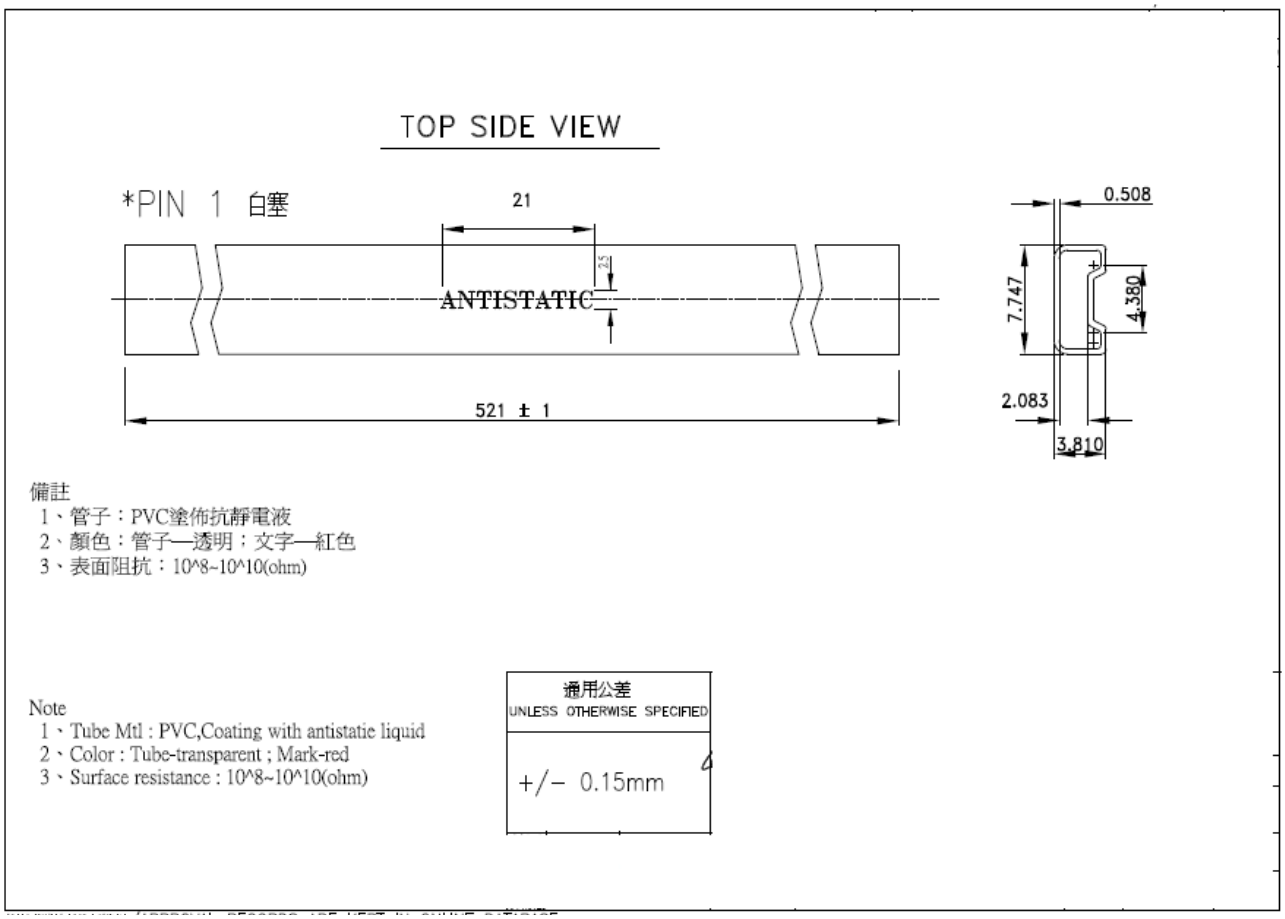


SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	4.80	4.90	5.00
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	-	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm

7.2.2. Tube Dimensions SSOP16(150mil)



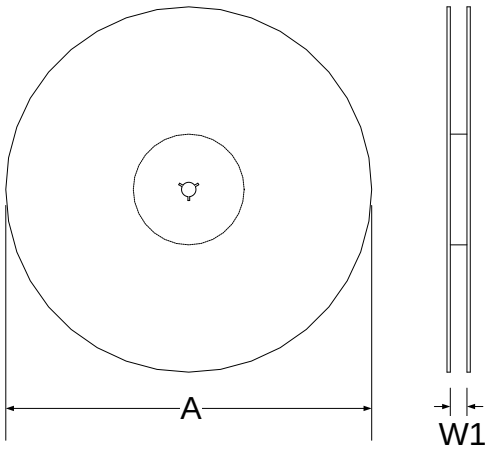
備註
1、管子：PVC塗佈抗靜電液
2、顏色：管子—透明；文字—紅色
3、表面阻抗：10^8~10^10(ohm)

Note
1、Tube Mtl : PVC,Coating with antistatic liquid
2、Color : Tube-transparent ; Mark-red
3、Surface resistance : 10^8~10^10(ohm)

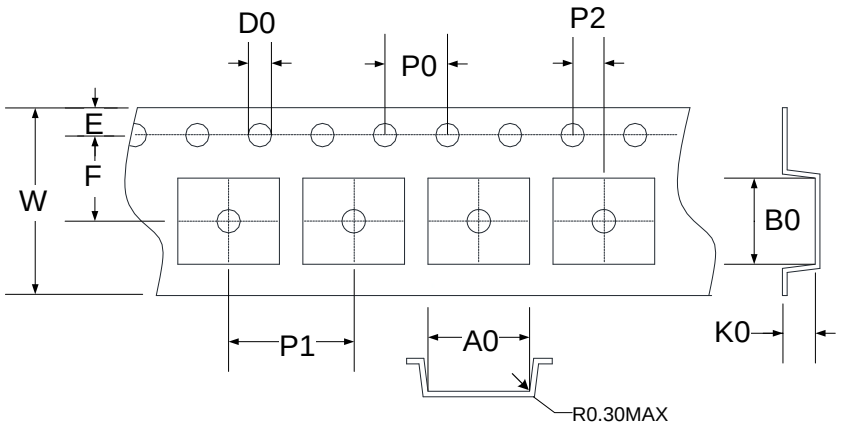
通用公差 UNLESS OTHERWISE SPECIFIED
+/− 0.15mm

7.2.3. Tape & Reel Information SSOP16(150mil)-Type 1

1. Reel Dimensions



2. Carrier Tape Dimensions

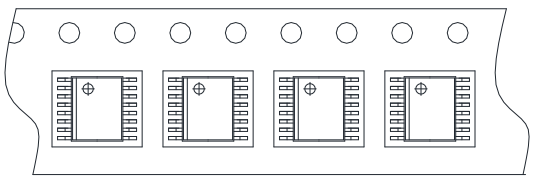


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

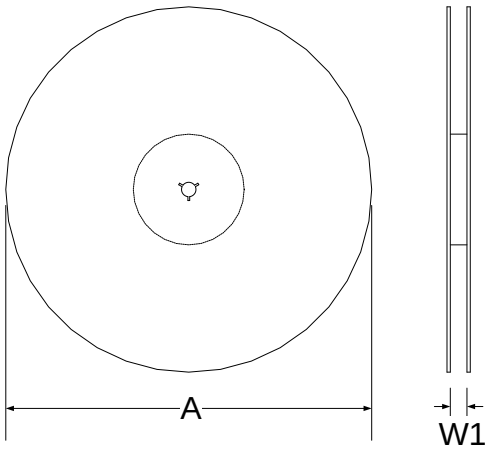
Unit: mm

3. Pin1 direction

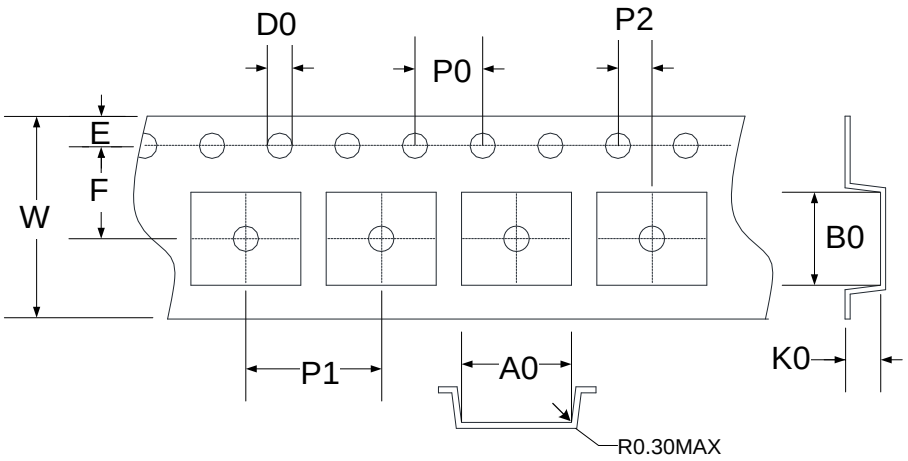


7.2.4. Tape & Reel Information SSOP16(150mil) -Type 2

1. Reel Dimensions



2. Carrier Tape Dimensions

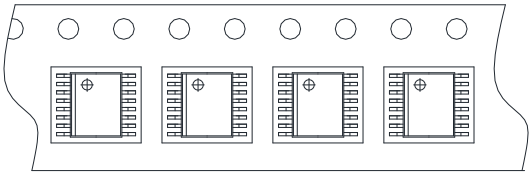


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.50	5.20	2.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

Unit: mm

3. Pin1 direction



8. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V01	All	First edition
V02	All	Remove the 2MHz and 8MHz HAO specifications
	5	Add in Function List
	14	Revised the SDR and VDDA LDO specifications in section 5.2
	20	Revised the LVD specifications in section 5.5
	21	Revised the LPO and 4MHz HAO specifications in section 5.6
V03	7	Add VDD Cap Size
	15	Add RSENS specifications
	23	Add VDD=5V Supply current specifications
	23	Add VDD=3.6V MAX Supply current specifications
V04	26	Update the unit quantity of tape packing type for QFN16 package