HY16F3910

Datasheet

High Precision Mixed-Signal Controller
4X44 ~ 8X40 LCD Driver
32-Bit Low Power MCU
21-bit ENOB ΣΔADC
128KB Flash ROM

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1. Features

Digital Circuit

- 32-bit MCU 1T Andes Core E801
- Andes Sight C IDE Complier & User Friendly Development Tools
- 2.0V to 5.5V wide operational voltage
- -40 to 85℃ operational environment
- Low power operation:
  - Normal Mode：
    0.8mA@HSRC=4.147MHz
  - Idle Mode：5uA@LSRC=32KHz
  - Sleep mode：Typ.2.5uA
- 128KB Flash ROM
  - Write/Erase cycle times：100,000 cycles
  - Write/Read/Erase operating voltage ≧ 2.0V
  - Support hardware In System Programming(ISP) function.
- 8KB SRAM
- 16-bit Timer A, Timer B(X2), Timer C, WDT
- 16-bit PWM controller and capture function
- I²C/32-bit SPI/UART(X2) communication interface
- RTC Hardware IP
- 72 programmable digital I/O ports
  - 24 general propose digital I/O ports
  - 48 programmable digital I/O ports multiplexed with LCD Segment
- 4x44 ~ 8x40 LCD Driver
  - 1/3、1/4、1/5、1/6、1/8 Duty
  - 1/3 及 1/4 Bias mode

- R-type External VLCD Application
- Internal Charge Pump VLCD, support 6-stage VLCD voltage, 2.8V, 3.0V, 3.3V, 3.9V, 4.5V and 5.0V

Analog Circuit
- 2.4V to 3.6V analog operational voltage
- 24-bit Σ ADC
  - ADC support x1~x4 signal amplification
  - built-in PGA support x8,x16,x32 signal amplification
  - The input reference signal can be resolved to 65nVrms (Gain=128)
  - Highest conversion rate of up to 15Ksps
  - Built-in absolute temperature sensor
- External High Speed Oscillator Max 16MHz
- External Low Speed Oscillator Mode 32768Hz
- Internal High Speed Oscillator HAO 4.147MHz and 31.795MHz (CPU max speed is 16MHz)
- Internal Low Speed Oscillator LPO 32KHz
- Power management
  - Build-in selectable voltage (VDDA)
  - 1.2V Band gap reference output (REFO)
- Multi-function Comparator
  - Support external voltage input comparison
  - Support 15-stage Low voltage detection (LVD)

Part No.	24-b ΣΔADC	Flash (byte)	SRAM (byte)	Temp. Sensor	RTC	I/O	PWM	Serial Interface	LCD	ISP Mode	Package
HY16F3910-N088	9-CH	128K	8K	Y	1	24+48	4-CH	2*UART 32bits SPI I²C	4x44 6x42 8x40	Y	QFN88
HY16F3910-L080	9-CH	128K	8K	Y	1	24+44	4-CH	2*UART 32bits SPI I²C	4x40 6x38 8x36	Y	LQFP80
HY16F3910-L064	9-CH	128K	8K	Y	1	24+30	4-CH	2*UART 32bits SPI I²C	4x26 6x24 8x22	Y	LQFP64

2. Pin Definition

2.1. HY16F3910 series pin diagram
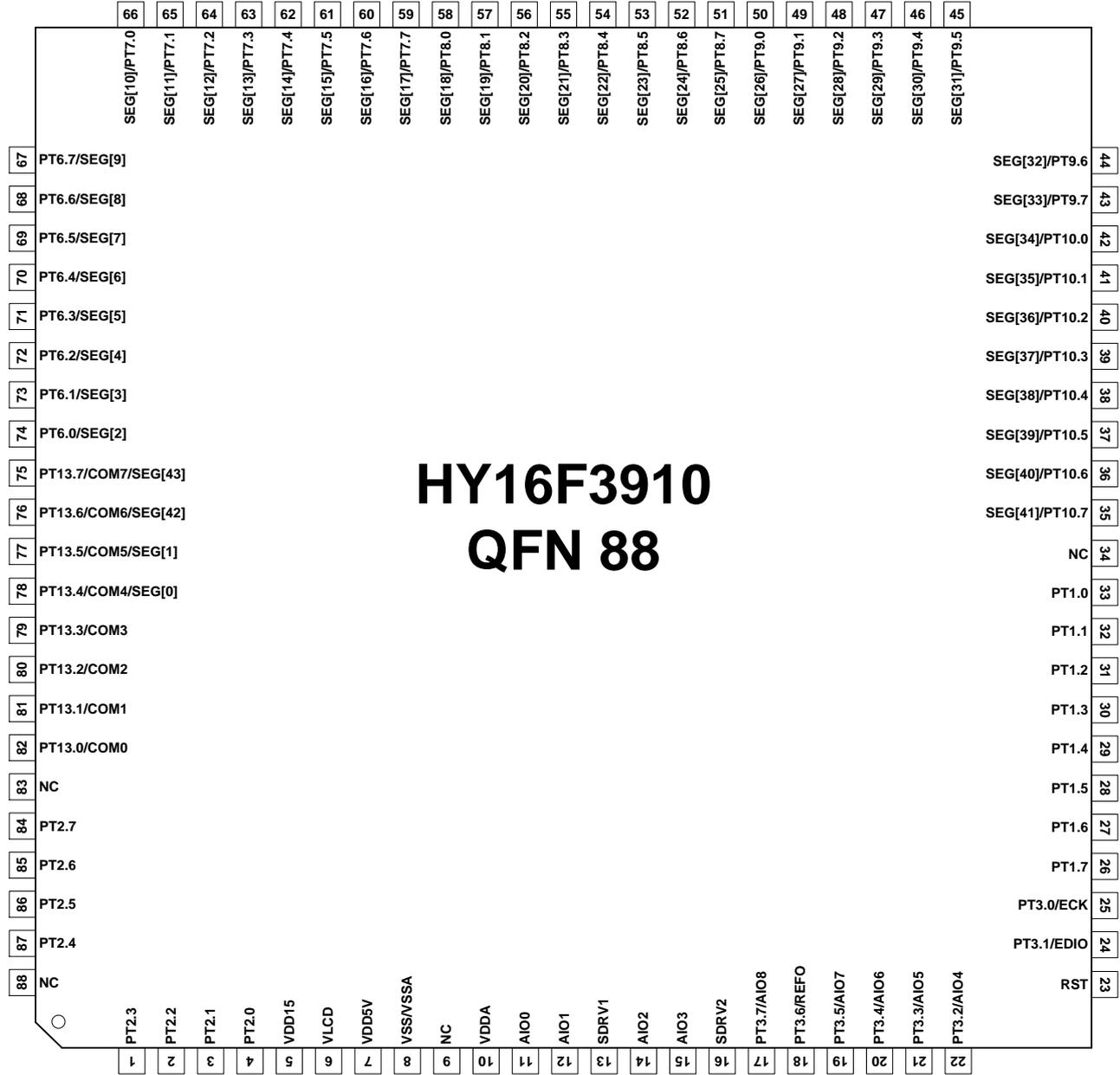
Figure 2-1-1 QFN 88 Pin Diagram

Pin	Left Signal		Right Signal	Pin
61	PT6.6/SEG[8]		SEG[31]/PT9.5	40
62	PT6.5/SEG[7]		SEG[34]/PT10.0	39
63	PT6.4/SEG[6]		SEG[35]/PT10.1	38
64	PT6.3/SEG[5]		SEG[36]/PT10.2	37
65	PT6.2/SEG[4]		SEG[37]/PT10.3	36
66	PT6.1/SEG[3]		SEG[38]/PT10.4	35
67	PT6.0/SEG[2]		SEG[39]/PT10.5	34
68	PT13.7/COM7/SEG[43]		SEG[40]/PT10.6	33
69	PT13.6/COM6/SEG[42]		SEG[41]/PT10.7	32
70	PT13.5/COM5/SEG[1]		PT1.0	31
71	PT13.4/COM4/SEG[0]		PT1.1	30
72	PT13.3/COM3		PT1.2	29
73	PT13.2/COM2		PT1.3	28
74	PT13.1/COM1		PT1.4	27
75	PT13.0/COM0		PT1.5	26
76	PT2.7		PT1.6	25
77	PT2.6		PT1.7	24
78	PT2.5		PT3.0/ECK	23
79	PT2.4		PT3.1/EDIO	22
80	PT2.3		RST	21

HY16F3910
LQFP 80

Top pins (60–41):
60	SEG[9]/PT6.7
59	SEG[12]/PT7.2
58	SEG[13]/PT7.3
57	SEG[14]/PT7.4
56	SEG[15]/PT7.5
55	SEG[16]/PT7.6
54	SEG[17]/PT7.7
53	SEG[18]/PT8.0
52	SEG[19]/PT8.1
51	SEG[20]/PT8.2
50	SEG[21]/PT8.3
49	SEG[22]/PT8.4
48	SEG[23]/PT8.5
47	SEG[24]/PT8.6
46	SEG[25]/PT8.7
45	SEG[26]/PT9.0
44	SEG[27]/PT9.1
43	SEG[28]/PT9.2
42	SEG[29]/PT9.3
41	SEG[30]/PT9.4

Bottom pins (1–20):
1	PT2.2
2	PT2.1
3	PT2.0
4	VDD15
5	VLCD
6	VDD5V
7	VSS/VSSA
8	VDDA
9	AIO0
10	AIO1
11	SDRV1
12	AIO2
13	AIO3
14	SDRV2
15	PT3.7/AIO8
16	PT3.6/REFO
17	PT3.5/AIO7
18	PT3.4/AIO6
19	PT3.3/AIO5
20	PT3.2/AIO4

Figure 2-1-2 LQFP 80 Pin Diagram
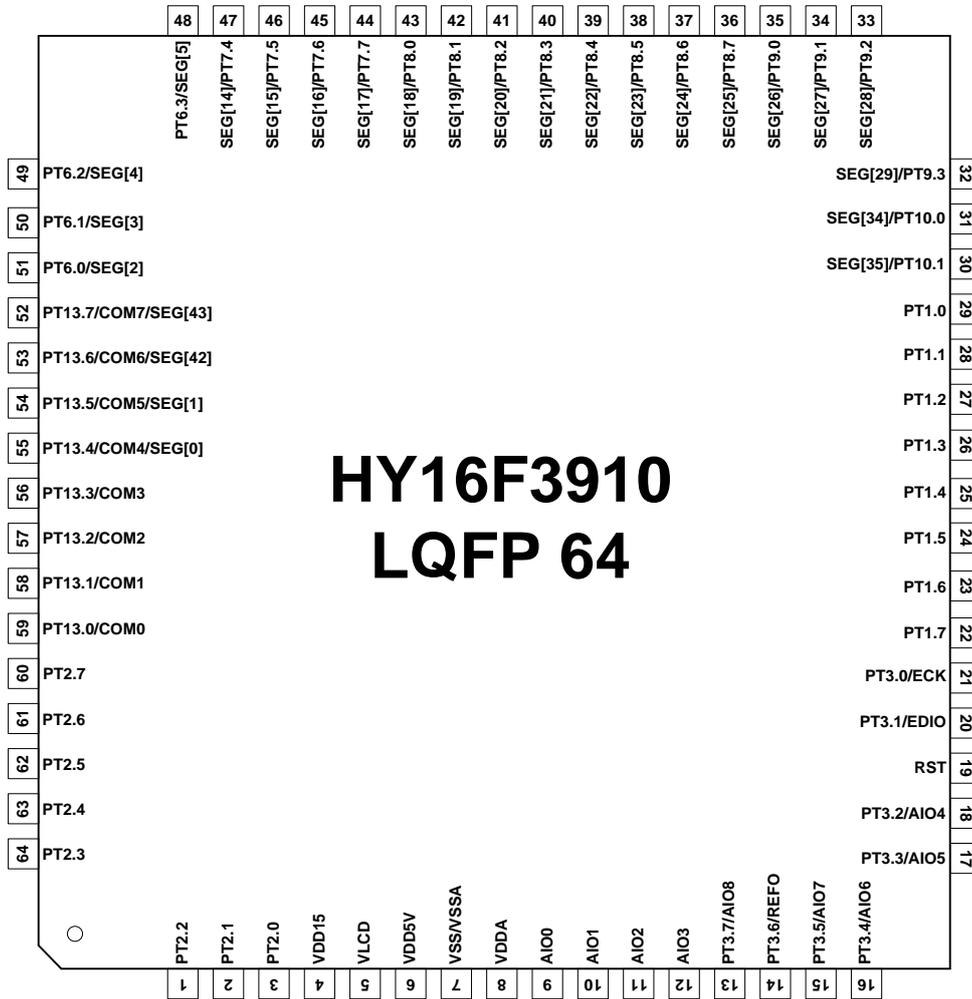
Figure 2-1-3 LQFP 64 Pin Diagram

2.2. Pin Description

2.2.1. HY6F3910 Pin Definition

"I" : Input ,"O" : Output, "A" : Analog, "S" : Smith triggers, "C" : CMOS I/O,"P" : Power Source,"/" : or ,"X" : Ignorable.

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
1	80	64	PT2.3	I/O	S/C	Digital Input/ Output Pin
			INT2.3	I	S	Interrupt Source INT 2.3
			LVDOO	O	C	Low voltage comparison (LVDO output pin)
			PWM3_3	O	C	TimerB2, PWM3_3 Output Pin
			MOSI_3	O	C	SPI Interface MOSI_3(Master output, Slave input)
			RX2_3	I	S	EUART2 Interface RX2_3
			TCI2_6	I	S	Capture Comparator Input Source Pin TCI2_6
			SDA_6	I/O	S/C	I²C Interface SDA_6
2	1	1	PT2.2	I/O	S/C	Digital Input/ Output Pin
			INT2.2	I	S	Interrupt Source INT 2.2
			PWM2_3	O	C	TimerB2, PWM2_3 Output Pin
			MISO_3	I	S	SPI Interface MISO_3(Master input, Slave output)
			TX2_3	O	C	EUART2 Interface TX2_3
			TCI1_6	I	S	Capture Comparator Input Source Pin TCI1_6
			SCL_6	I/O	S/C	I²C Interface SCL_6
3	2	2	PT2.1	I/O	S/C	Digital Input/ Output Pin
			INT2.1	I	S	Interrupt Source INT 2.1
			PWM1_3	O	C	TimerB, PWM1_3 Output Pin
			CK_3	O	C	SPI Interface CK_3
			RX_3	I	S	EUART Interface RX_3
			TCI2_5	I	S	Capture Comparator Input Source Pin TCI2_5
			SDA_5	I/O	S/C	I²C Interface SDA_5
4	3	3	PT2.0	I/O	S/C	Digital Input/ Output Pin
			INT2.0	I	S	Interrupt Source INT 2.0
			PWM0_3	O	C	TimerB, PWM0_3 Output Pin
			CS_3	I	S	SPI Interface CS_3
			TX_3	O	C	EUART Interface TX_3
			TCI1_5	I	S	Capture Comparator Input Source Pin TCI1_5
			SCL_5	I/O	S/C	I²C Interface SCL_5
5	4	4	VDD15	I	P	Digital Power Supply output, 1uF Cap to VSS
6	5	5	VLCD	I/O	P	LCD Power Supply Output, or Power Supply Input,

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
						10uF Cap to VSS.
7	6	6	VDD5V	I	P	Chip power supply voltage input pin, the external 0.1uF filtering capacitor and voltage stabilizing capacitor to VSS is required.
8	7	7	VSS	I	PP	Digital System Power Ground
			VSSA	I	P	Analog System Power Ground
10	8	8	VDDA	I/O	P	Analog Power Supply, LDO Output, or Analog Power Input , 1uF~10uF Cap to VSS.
11	9	9	AIO0	I	A	ADC Analog Input Signal Port AIO0
12	10	10	AIO1	I	A	ADC Analog Input Signal Port AIO1
13	11	-	SDRV1	O	P	Reserved, not connect.
14	12	11	AIO2	I	A	ADC Analog Input Signal Port AIO2
15	13	12	AIO3	I	A	ADC Analog Input Signal Port AIO3
16	14	-	SDRV2	O	P	Reserved, not connect.
17	15	13	PT3.7	I/O	S/C	Digital Input/ Output Pin
			INT3.7	I	S	Interrupt Source INT 3.7
			LVDIN	I	A	Low voltage comparison (LVD external signal input port)
			AIO8	I	A	ADC Analog Input Signal Port AIO8
18	16	14	PT3.6	I/O	S/C	Digital Input/ Output Pin
			INT3.6	I	S	Interrupt Source INT 3.6
			REFO	I/O	P	Reference Voltage output 1.2V, 0.1uF Cap to VSS.
19	17	15	PT3.5	I/O	S/C	Digital Input/ Output Pin
			INT3.5	I	S	Interrupt Source INT 3.5
			AIO7	I/O	A	ADC Analog Input Signal Port AIO7
20	18	16	PT3.4	I/O	S/C	Digital Input/ Output Pin
			INT3.4	I	S	Interrupt Source INT 3.4
			AIO6	I/O	A	ADC Analog Input Signal Port AIO6
21	19	17	PT3.3	I/O	S/C	Digital Input/ Output Pin
			INT3.3	I	S	Interrupt Source INT 3.3
			AIO5	I/O	A	ADC Analog Input Signal Port AIO5
22	20	18	PT3.2	I/O	S/C	Digital Input/ Output Pin
			INT3.2	I	S	Interrupt Source INT 3.2
			AIO4	I/O	A	ADC Analog Input Signal Port AIO4
23	21	19	RST	I	D	Reset pin (Active Low Reset) 10nF Cap to VSS

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
24	22	20	PT3.1	I/O	S/C	Digital Input/ Output Pin
			INT3.1	I	S	Interrupt Source INT 3.1
			EDIO	I/O	D	Embedded Debug Module (EDM) Data Input/ Output PIN,
25	23	21	PT3.0	I/O	S/C	Digital Input/ Output Pin
			INT3.0	I	S	Interrupt Source INT 3.0
			ECK	I/O	D	Embedded Debug Module (EDM) Clock Input PIN.
26	24	22	PT1.7	I/O	S/C	Digital Input/ Output Pin
			INT1.7	I	S	Interrupt Source INT 1.7
			PWM3_2	O	C	TimerB2, PWM3_2 Output Pin
			MOSI_2	O	C	SPI Interface MOSI_2(Master output, Slave input)
			RX2_2	I	S	EUART2 Interface RX2_2
			TCI2_4	I	S	Capture Comparator Input Source Pin TCI2_4
			SDA_4	I/O	S/C	I^{2}C Interface SDA_4
27	25	23	PT1.6	I/O	S/C	Digital Input/ Output Pin
			INT1.6	I	S	Interrupt Source INT 1.6
			PWM2_2	O	C	TimerB2, PWM2_2 Output Pin
			MISO_2	I	S	SPI Interface MISO_2(Master input, Slave output)
			TX2_2	O	C	EUART2 Interface TX2_2
			TCI1_4	I	S	Capture Comparator Input Source Pin TCI1_4
			SCL_4	I/O	S/C	I^{2}C Interface SCL_4
28	26	24	PT1.5	I/O	S/C	Digital Input/ Output Pin
			INT1.5	I	S	Interrupt Source INT 1.5
			PWM1_2	O	C	TimerB, PWM1_2 Output Pin
			CK_2	O	C	SPI Interface CK_2
			RX_2	I	S	EUART Interface RX_2
			TCI2_3	I	S	Capture Comparator Input Source Pin TCI2_3
			SDA_3	I/O	S/C	I^{2}C Interface SDA_3
29	27	25	PT1.4	I/O	S/C	Digital Input/ Output Pin
			INT1.4	I	S	Interrupt Source INT 1.4
			PWM0_2	O	C	TimerB, PWM0_2 Output Pin
			CS_2	I	S	SPI Interface CS_2
			TX_2	O	C	EUART Interface TX_2

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
			TCI1_3	I	S	Capture Comparator Input Source Pin TCI1_3
			SCL_3	I/O	S/C	I²C Interface SCL_3
30	28	26	PT1.3	I/O	S/C	Digital Input/ Output Pin
			INT1.3	I	S	Interrupt Source INT 1.3
			PWM3_1	O	C	TimerB2, PWM3_1 Output Pin
			MOSI_1	O	C	SPI Interface MOSI_1(Master output, Slave input)
			RX2_1	I	S	EUART2 Interface RX2_1
			TCI2_2	I	S	Capture Comparator Input Source Pin TCI2_2
			SDA_2	I/O	S/C	I²C Interface SDA_2
31	29	27	PT1.2	I/O	S/C	Digital Input/ Output Pin
			INT1.2	I	S	Interrupt Source INT 1.2
			PWM2_1	O	C	TimerB2, PWM2_1 Output Pin
			MISO_1	I	S	SPI Interface MISO_1(Master input, Slave output)
			TX2_1	O	C	EUART2 Interface TX2_1
			TCI1_2	I	S	Capture Comparator Input Source Pin TCI1_2
			SCL_2	I/O	S/C	I²C Interface SCL_2
32	30	28	PT1.1	I/O	S/C	Digital Input/ Output Pin
			INT1.1	I	S	Interrupt Source INT 1.1
			PWM1_1	O	C	TimerB, PWM1_1 Output Pin
			CK_1	O	C	SPI Interface CK_1
			RX_1	I	S	EUART Interface RX_1
			TCI2_1	I	S	Capture Comparator Input Source Pin TCI2_1
			SDA_1	I/O	S/C	I²C Interface SDA_1
33	31	29	PT1.0	I/O	S/C	Digital Input/ Output Pin
			INT1.0	I	S	Interrupt Source INT 1.0
			PWM0_1	O	C	TimerB, PWM0_1 Output Pin
			CS_1	I	S	SPI Interface CS_1
			TX_1	O	C	EUART Interface TX_1
			TCI1_1	I	S	Capture Comparator Input Source Pin TCI1_1
			SCL_1	I/O	S/C	I²C Interface SCL_1
34	-	-	NC	-	-	Not Connect
35	32	-	PT10.7	I/O	S/C	Digital Input/ Output Pin
			SEG41	O	A	LCD Segment 41 Output
36	33	-	PT10.6	I/O	S/C	Digital Input/ Output Pin

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
			SEG40	O	A	LCD Segment 40 Output
			TCI3_8	I	S	Capture Comparator Input Source Pin TCI3_8
37	34	-	PT10.5	I/O	S/C	Digital Input/ Output Pin
			SEG39	O	A	LCD Segment 39 Output
38	35	-	PT10.4	I/O	S/C	Digital Input/ Output Pin
			SEG38	O	A	LCD Segment 38 Output
			TCI3_7	I	S	Capture Comparator Input Source Pin TCI3_7
39	36	-	PT10.3	I/O	S/C	Digital Input/ Output Pin
			SEG37	O	A	LCD Segment 37 Output
40	37	-	PT10.2	I/O	S/C	Digital Input/ Output Pin
			SEG36	O	A	LCD Segment 36 Output
41	38	30	PT10.1	I/O	S/C	Digital Input/ Output Pin
			SEG35	O	A	LCD Segment 35 Output
42	39	31	PT10.0	I/O	S/C	Digital Input/ Output Pin
			SEG34	O	A	LCD Segment 34 Output
43	-	-	PT9.7	I/O	S/C	Digital Input/ Output Pin
			SEG33	O	A	LCD Segment 33 Output
44	-	-	PT9.6	I/O	S/C	Digital Input/ Output Pin
			SEG32	O	A	LCD Segment 32 Output
45	40	-	PT9.5	I/O	S/C	Digital Input/ Output Pin
			SEG31	O	A	LCD Segment 31 Output
46	41	-	PT9.4	I/O	S/C	Digital Input/ Output Pin
			SEG30	O	A	LCD Segment 30 Output
47	42	32	PT9.3	I/O	S/C	Digital Input/ Output Pin
			SEG29	O	A	LCD Segment 29 Output
			PWM3_7	O	C	TimerB2, PWM3_7 Output Pin
			MOSI_7	O	C	SPI Interface MOSI_7(Master output, Slave input)
			RX2_7	I	S	EUART2 Interface RX2_7
48	43	33	PT9.2	I/O	S/C	Digital Input/ Output Pin
			SEG28	I	S	LCD Segment 28 Output
			PWM2_7	O	C	TimerB2, PWM2_7 Output Pin
			MISO_7	I	S	SPI Interface MISO_7(Master input, Slave output)
			TX2_7	O	C	EUART2 Interface TX2_7
			TCI3_6	I	S	Capture Comparator Input Source Pin TCI3_6

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
49	44	34	PT9.1	I/O	S/C	Digital Input/ Output Pin
			SEG27	I	S	LCD Segment 27 Output
			PWM1_7	O	C	TimerB, PWM1_7 Output Pin
			CK_7	O	C	SPI Interface CK_7
			RX_7	I	S	EUART Interface RX_7
50	45	35	PT9.0	I/O	S/C	Digital Input/ Output Pin
			SEG26	I	S	LCD Segment 26 Output
			PWM0_7	O	C	TimerB, PWM0_1 Output Pin
			CS_7	I	S	SPI Interface CS_1
			TX_7	O	C	EUART Interface TX_1
			TCI3_5	I	S	Capture Comparator Input Source Pin TCI3_5
51	46	36	PT8.7	I/O	S/C	Digital Input/ Output Pin
			SEG25	O	A	LCD Segment 25 Output
52	47	37	PT8.6	I/O	S/C	Digital Input/ Output Pin
			SEG24	O	A	LCD Segment 24 Output
53	48	38	PT8.5	I/O	S/C	Digital Input/ Output Pin
			SEG23	O	A	LCD Segment 23 Output
54	49	39	PT8.4	I/O	S/C	Digital Input/ Output Pin
			SEG22	O	A	LCD Segment 22 Output
55	50	40	PT8.3	I/O	S/C	Digital Input/ Output Pin
			SEG21	O	A	LCD Segment 21 Output
			PWM3_8	O	C	TimerB2, PWM3_8 Output Pin
			MOSI_8	O	C	SPI Interface MOSI_8(Master output, Slave input)
			RX2_8	I	S	EUART2 Interface RX2_8
56	51	41	PT8.2	I/O	S/C	Digital Input/ Output Pin
			SEG20	I	S	LCD Segment 20 Output
			PWM2_8	O	C	TimerB2, PWM2_8 Output Pin
			MISO_8	I	S	SPI Interface MISO_8(Master input, Slave output)
			TX2_8	O	C	EUART2 Interface TX2_8
57	52	42	PT8.1	I/O	S/C	Digital Input/ Output Pin
			SEG19	I	S	LCD Segment 19 Output
			PWM1_8	O	C	TimerB, PWM1_8 Output Pin
			CK_8	O	C	SPI Interface CK_8
			RX_8	I	S	EUART Interface RX_8

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
58	53	43	PT8.0	I/O	S/C	Digital Input/ Output Pin
			SEG18	I	S	LCD Segment 18 Output
			PWM0_8	O	C	TimerB, PWM0_8 Output Pin
			CS_8	I	S	SPI Interface CS_8
			TX_8	O	C	EUART Interface TX_8
59	54	44	PT7.7	I/O	S/C	Digital Input/ Output Pin
			SEG17	O	A	LCD Segment 17 Output
			PWM3_6	O	C	TimerB2, PWM3_6 Output Pin
			MOSI_6	O	C	SPI Interface MOSI_6(Master output, Slave input)
			RX2_6	I	S	EUART2 Interface RX2_6
60	55	45	PT7.6	I/O	S/C	Digital Input/ Output Pin
			SEG16	I	S	LCD Segment 16 Output
			PWM2_6	O	C	TimerB2, PWM2_6 Output Pin
			MISO_6	I	S	SPI Interface MISO_6(Master input, Slave output)
			TX2_6	O	C	EUART2 Interface TX2_6
			TCI3_4	I	S	Capture Comparator Input Source Pin TCI3_4
61	56	46	PT7.5	I/O	S/C	Digital Input/ Output Pin
			SEG15	O	A	LCD Segment 15 Output
			PWM1_6	O	C	TimerB, PWM1_6 Output Pin
			CK_6	O	C	SPI Interface CK_6
			RC_6	I	S	EUART Interface RX_6
62	57	47	PT7.4	I/O	S/C	Digital Input/ Output Pin
			SEG14	O	A	LCD Segment 14 Output
			PWM0_6	O	C	TimerB, PWM0_6 Output Pin
			CS_6	O	C	SPI Interface CS_6
			TX_6	I	S	EUART Interface TX_6
			TCI3_3	I	S	Capture Comparator Input Source Pin TCI3_3
63	58	-	PT7.3	I/O	S/C	Digital Input/ Output Pin
			SEG13	O	A	LCD Segment 13 Output
64	59	-	PT7.2	I/O	S/C	Digital Input/ Output Pin
			SEG12	O	A	LCD Segment 12 Output
65	-	-	PT7.1	I/O	S/C	Digital Input/ Output Pin
			SEG11	O	A	LCD Segment 11 Output
66	-	-	PT7.0	I/O	S/C	Digital Input/ Output Pin

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
			SEG10	O	A	LCD Segment 10 Output
67	60	-	PT6.7	I/O	S/C	Digital Input/ Output Pin
			SEG9	O	A	LCD Segment 9 Output
68	61	-	PT6.6	I/O	S/C	Digital Input/ Output Pin
			SEG8	O	A	LCD Segment 8 Output
69	62	-	PT6.5	I/O	S/C	Digital Input/ Output Pin
			SEG7	O	A	LCD Segment 7 Output
70	63	-	PT6.4	I/O	S/C	Digital Input/ Output Pin
			SEG6	O	A	LCD Segment 6 Output
71	64	48	PT6.3	I/O	S/C	Digital Input/ Output Pin
			SEG5	O	A	LCD Segment 5 Output
			PWM3_5	O	C	TimerB2, PWM3_5 Output Pin
			MOSI_5	O	C	SPI Interface MOSI_5(Master output, Slave input)
			RX2_5	I	S	EUART2 Interface RX2_5
72	65	49	PT6.2	I/O	S/C	Digital Input/ Output Pin
			SEG4	O	A	LCD Segment 4 Output
			PWM2_5	O	C	TimerB2, PWM2_5 Output Pin
			MISO_5	I	S	SPI Interface MISO_5(Master input, Slave output)
			TX2_5	O	C	EUART2 Interface TX2_5
			TCI3_2	I	S	Capture Comparator Input Source Pin TCI3_2
73	66	50	PT6.1	I/O	S/C	Digital Input/ Output Pin
			SEG3	O	A	LCD Segment 3 Output
			PWM1_5	O	C	TimerB, PWM1_5 Output Pin
			CK_5	O	C	SPI Interface CK_5
			RX_5	I	S	EUART Interface RX_5
74	67	51	PT6.0	I/O	S/C	Digital Input/ Output Pin
			SEG2	O	A	LCD Segment 2 Output
			PWM0_5	O	C	TimerB, PWM0_5 Output Pin
			CS_5	I	S	SPI Interface CS_5
			TX_5	O	C	EUART Interface TX_5
			TCI3_1	I	S	Capture Comparator Input Source Pin TCI3_1
75	68	52	PT13.7	I/O	S/C	Digital Input/ Output Pin
			SEG43	O	A	LCD Segment 43 Output
			COM7	O	A	LCD Common 7 Output

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
76	69	53	PT13.6	I/O	S/C	Digital Input/ Output Pin
			SEG42	O	A	LCD Segment 42 Output
			COM6	O	A	LCD Common 6 Output
77	70	54	PT13.5	I/O	S/C	Digital Input/ Output Pin
			SEG1	O	A	LCD Segment 1 Output
			COM5	O	A	LCD Common 5 Output
78	71	55	PT13.4	I/O	S/C	Digital Input/ Output Pin
			SEG0	O	A	LCD Segment 0 Output
			COM4	O	A	LCD Common 4 Output
79	72	56	PT13.3	I/O	S/C	Digital Input/ Output Pin
			COM3	O	A	LCD Common 3 Output
80	73	57	PT13.2	I/O	S/C	Digital Input/ Output Pin
			COM2	O	A	LCD Common 2 Output
81	74	58	PT13.1	I/O	S/C	Digital Input/ Output Pin
			COM1	O	A	LCD Common 1 Output
82	75	59	PT13.0	I/O	S/C	Digital Input/ Output Pin
			COM0	O	A	LCD Common 0 Output
84	76	60	PT2.7	I/O	S/C	Digital Input/ Output Pin
			HS_XOUT	A	A	External High Speed oscillator XOUT 2~16MHz, output pin
			INT2.7	I	S	Interrupt Source INT 2.7
			PWM3_4	O	C	TimerB2, PWM3_4 Output Pin
			MOSI_4	O	C	SPI Interface MOSI_4(Master output, Slave input)
			RX2_4	I	S	EUART2 Interface RX2_4
			TCI2_8	I	S	Capture Comparator Input Source Pin TCI2_8
			SDA_8	I/O	S/C	I²C Interface SDA_8
85	77	61	PT2.6	I/O	S/C	Digital Input/ Output Pin
			HS_XIN	A	A	External High Speed oscillator XIN 2~16MHz, input pin
			INT2.6	I	S	Interrupt Source INT 2.6
			PWM2_4	O	C	TimerB2, PWM2_4 Output Pin
			MISO_4	I	S	SPI Interface MISO_4(Master input, Slave output)
			TX2_4	O	C	EUART2 Interface TX2_4
			TCI1_8	I	S	Capture Comparator Input Source Pin TCI1_8
			SCL_8	I/O	S/C	I²C Interface SCL_8
86	78	62	PT2.5	I/O	S/C	Digital Input/ Output Pin

Package / Pin number			Pin Name	Pin Characteristic		Description
QFN88	LQFP80	LQFP64		Pin Type	Butter Type	
			LS_XIN	A	A	External Low Speed oscillator XIN 32768Hz, input pin
			INT2.5	I	S	Interrupt Source INT 2.5
			PWM1_4	O	C	TimerB, PWM1_4 Output Pin
			CK_4	O	C	SPI Interface CK_4
			RX_4	I	S	EUART Interface RX_4
			TCI2_7	I	S	Capture Comparator Input Source Pin TCI2_7
			SDA_7	I/O	S/C	I²C Interface SDA_7
87	79	63	PT2.4	I/O	S/C	Digital Input/ Output Pin
			LS_XOUT	A	A	External Low Speed Crystal XOUT 32768Hz, output pin
			INT2.4	I	S	Interrupt Source INT 2.4
			PWM0_4	O	C	TimerB2, PWM0_4 Output Pin
			CS_4	O	C	SPI Interface CS_4
			TX_4	O	C	EUART Interface TX_4
			TCI1_8	I	S	Capture Comparator Input Source Pin TCI1_7
			SCL_7	I/O	S/C	I²C Interface SCL_7
9 34 83 88	-	-	NC	-	-	Not Connect

Table 2-1 Pin definition and description

2.3. GPIO Port Function Configuration

Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT1.0	INT1.0	DIO	TCI1_1		CS_1	SCL_1	Tx_1		PWM0_1
PT1.1	INT1.1	DIO	TCI2_1		CK_1	SDA_1	Rx_1		PWM1_1
PT1.2	INT1.2	DIO	TCI1_2		MISO_1	SCL_2	Tx2_1		PWM2_1
PT1.3	INT1.3	DIO	TCI2_2		MOSI_1	SDA_2	Rx2_1		PWM3_1
PT1.4	INT1.4	DIO	TCI1_3		CS_2	SCL_3	Tx_2		PWM0_2
PT1.5	INT1.5	DIO	TCI2_3		CK_2	SDA_3	Rx_2		PWM1_2
PT1.6	INT1.6	DIO	TCI1_4		MISO_2	SCL_4	Tx2_2		PWM2_2
PT1.7	INT1.7	DIO	TCI2_4		MOSI_2	SDA_4	Rx2_2		PWM3_2
PT2.0	INT2.0	DIO	TCI1_5		CS_3	SCL_5	Tx_3		PWM0_3
PT2.1	INT2.1	DIO	TCI2_5		CK_3	SDA_5	Rx_3		PWM1_3
PT2.2	INT2.2	DIO	TCI1_6		MISO_3	SCL_6	Tx2_3		PWM2_3
PT2.3	INT2.3	DIO	TCI2_6	LVDOO	MOSI_3	SDA_6	Rx2_3		PWM3_3
PT2.4	INT2.4	DIO	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4		PWM0_4
PT2.5	INT2.5	DIO	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4		PWM1_4
PT2.6	INT2.6	DIO	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4		PWM2_4
PT2.7	INT2.7	DIO	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4		PWM3_4
PT3.0	INT3.0	DIO		**ECK**					
PT3.1	INT3.1	DIO		**EDIO**					
PT3.2	INT3.2	DIOAI						AIO4	
PT3.3	INT3.3	DIOAI						AIO5	
PT3.4	INT3.4	DIOAI						AIO6	
PT3.5	INT3.5	DIOAI						AIO7	
PT3.6	INT3.6	DIOAIO						REFO	
PT3.7	INT3.7	DIOAI						AIO8/LVDIN	
AIO0		AI						AIO0	
AIO1		AI						AIO1	
AIO2		AI						AIO2	
AIO3		AI						AIO3	
PT13.0		DIOAO		COM 0					
PT13.1		DIOAO		COM 1					
PT13.2		DIOAO		COM 2					
PT13.3		DIOAO		COM 3					

Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT13.4		DIOAO		COM 4/SEG 0					
PT13.5		DIOAO		COM 5/SEG 1					
PT13.6		DIOAO		COM 6/SEG 42					
PT13.7		DIOAO		COM 7/SEG 43					
PT6.0		DIOAO	TCI3_1	SEG 2	CS_5		Tx_5		PWM0_5
PT6.1		DIOAO		SEG 3	CK_5		Rx_5		PWM1_5
PT6.2		DIOAO	TCI3_2	SEG 4	MISO_5		Tx2_5		PWM2_5
PT6.3		DIOAO		SEG 5	MOSI_5		Rx2_5		PWM3_5
PT6.4		DIOAO		SEG 6					
PT6.5		DIOAO		SEG 7					
PT6.6		DIOAO		SEG 8					
PT6.7		DIOAO		SEG 9					
PT7.0		DIOAO		SEG 10					
PT7.1		DIOAO		SEG 11					
PT7.2		DIOAO		SEG 12					
PT7.3		DIOAO		SEG 13					
PT7.4		DIOAO	TCI3_3	SEG 14	CS_6		Tx_6		PWM0_6
PT7.5		DIOAO		SEG 15	CK_6		Rx_6		PWM1_6
PT7.6		DIOAO	TCI3_4	SEG 16	MISO_6		Tx2_6		PWM2_6
PT7.7		DIOAO		SEG 17	MOSI_6		Rx2_6		PWM3_6
PT8.0		DIOAO		SEG 18	CS_8		Tx_8		PWM0_8
PT8.1		DIOAO		SEG 19	CK_8		Rx_8		PWM1_8
PT8.2		DIOAO		SEG 20	MISO_8		Tx2_8		PWM2_8
PT8.3		DIOAO		SEG 21	MOSI_8		Rx2_8		PWM3_8
PT8.4		DIOAO		SEG 22					
PT8.5		DIOAO		SEG 23					
PT8.6		DIOAO		SEG 24					
PT8.7		DIOAO		SEG 25					
PT9.0		DIOAO	TCI3_5	SEG 26	CS_7		Tx_7		PWM0_7
PT9.1		DIOAO		SEG 27	CK_7		Rx_7		PWM1_7
PT9.2		DIOAO	TCI3_6	SEG 28	MISO_7		Tx2_7		PWM2_7
PT9.3		DIOAO		SEG 29	MOSI_7		Rx2_7		PWM3_7
PT9.4		DIOAO		SEG 30					
PT9.5		DIOAO		SEG 31					

Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT9.6		DIOAO		SEG 32					
PT9.7		DIOAO		SEG 33					
PT10.0		DIOAO		SEG 34					
PT10.1		DIOAO		SEG 35					
PT10.2		DIOAO		SEG 36					
PT10.3		DIOAO		SEG 37					
PT10.4		DIOAO	TCI3_7	SEG 38					
PT10.5		DIOAO		SEG 39					
PT10.6		DIOAO	TCI3_8	SEG 40					
PT10.7		DIOAO		SEG 41					

2.4. Package marking information

2.4.1. QFN Package marking information

XXXX → HYCON's Logo + Traceability code

HY16F3910 → Product Name :HY16F3910

XXXXXX → Product Low No.

└ LASER MARK for PIN 1
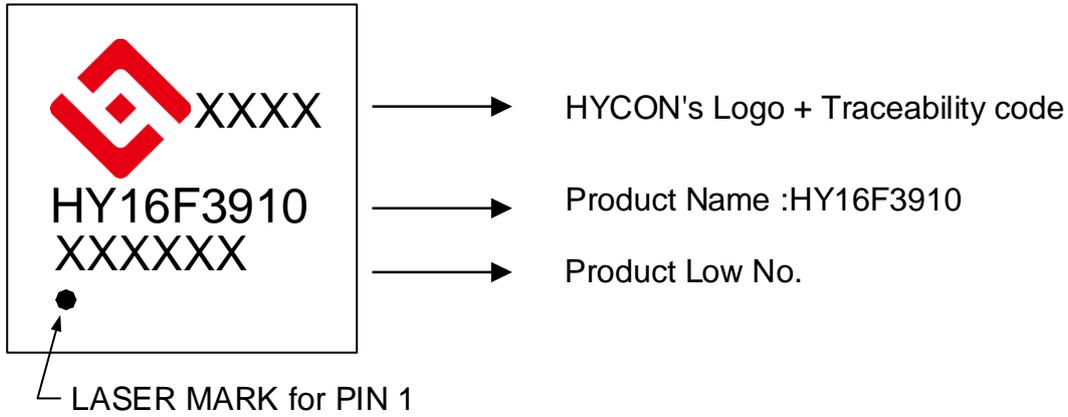
2.4.2. LQFP Package marking information

XXXX → HYCON's Logo + Traceability code

HY16F3910 → Product Name:HY16F3910

XXXXXX → Product Lot No.

└ PIN 1 MARK
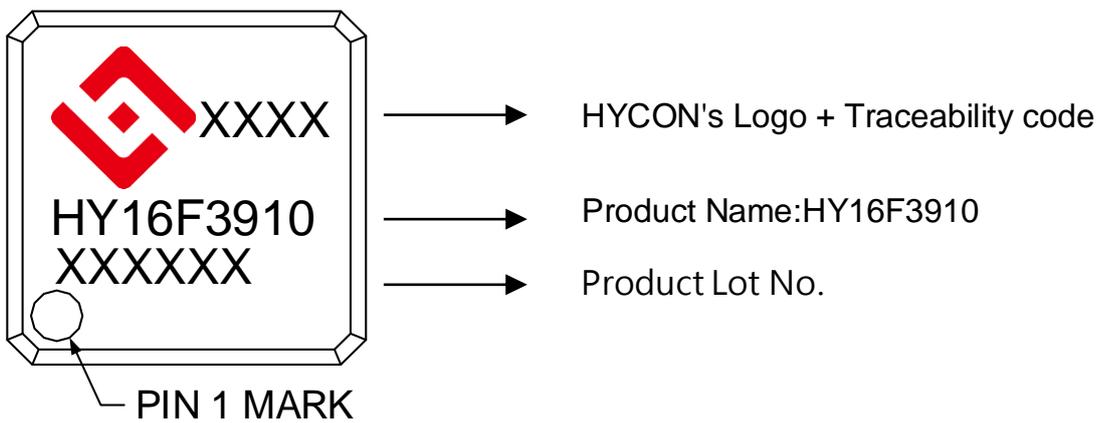
3. Application Circuit

3.1. Bridge Sensor Application Circuit
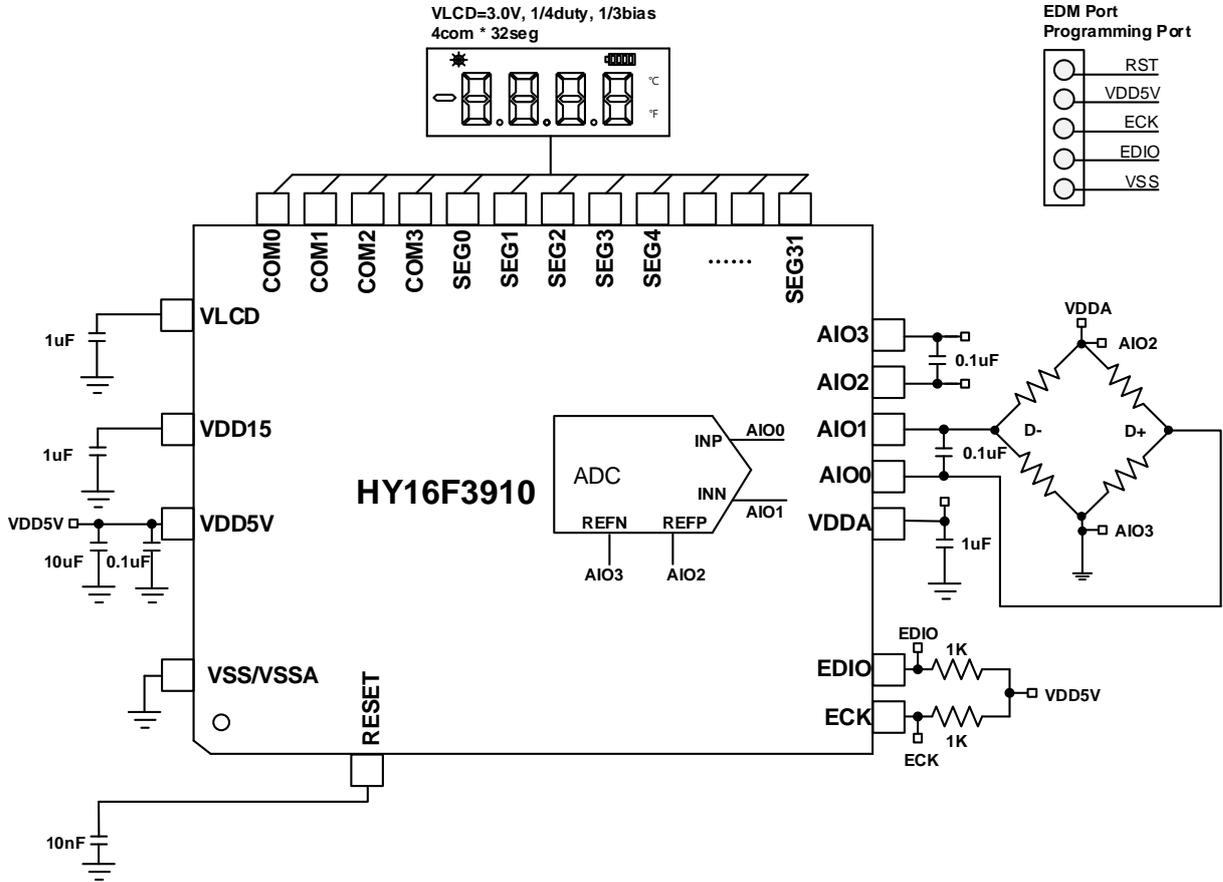
Figure 3-1 Bridge Sensor Application Circuit

3.2. Blood Pressure Application Circuit
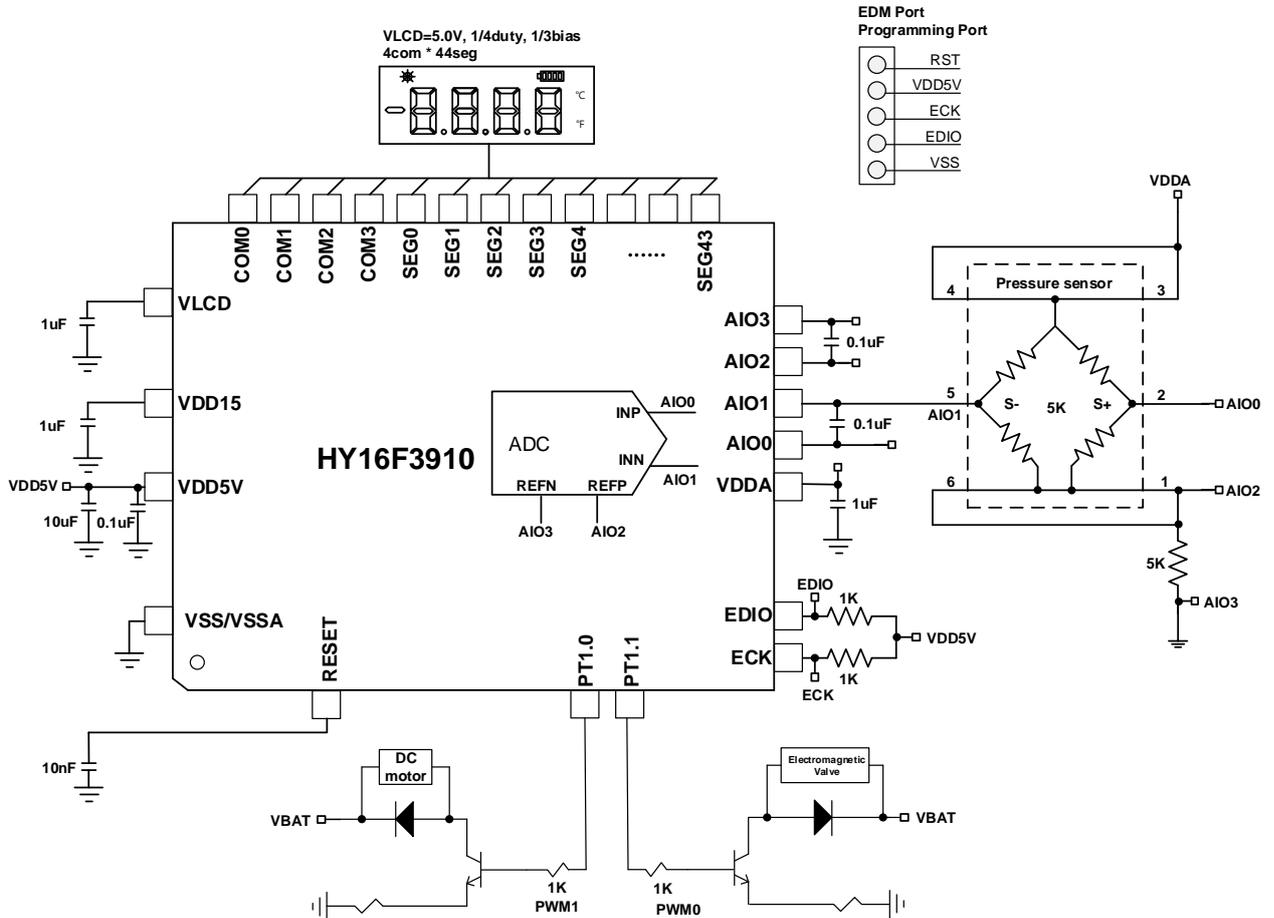
Figure 3-2 Blood Pressure Sensor Application Circuit

4. Function Outline

4.1. Internal Block Diagram
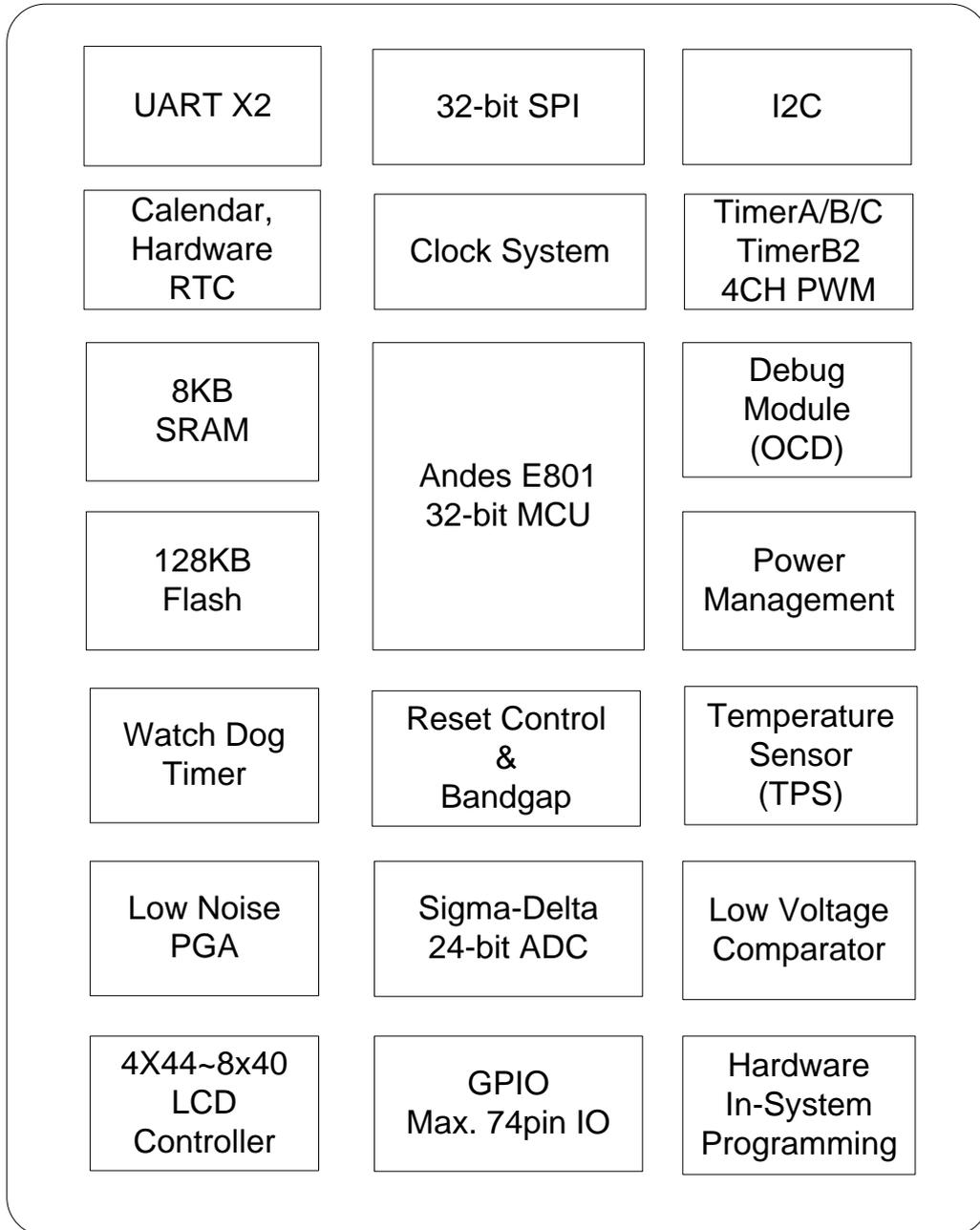
Figure 4-1 HY16F3910 Internal Block Diagram

4.2. Building Block Diagram
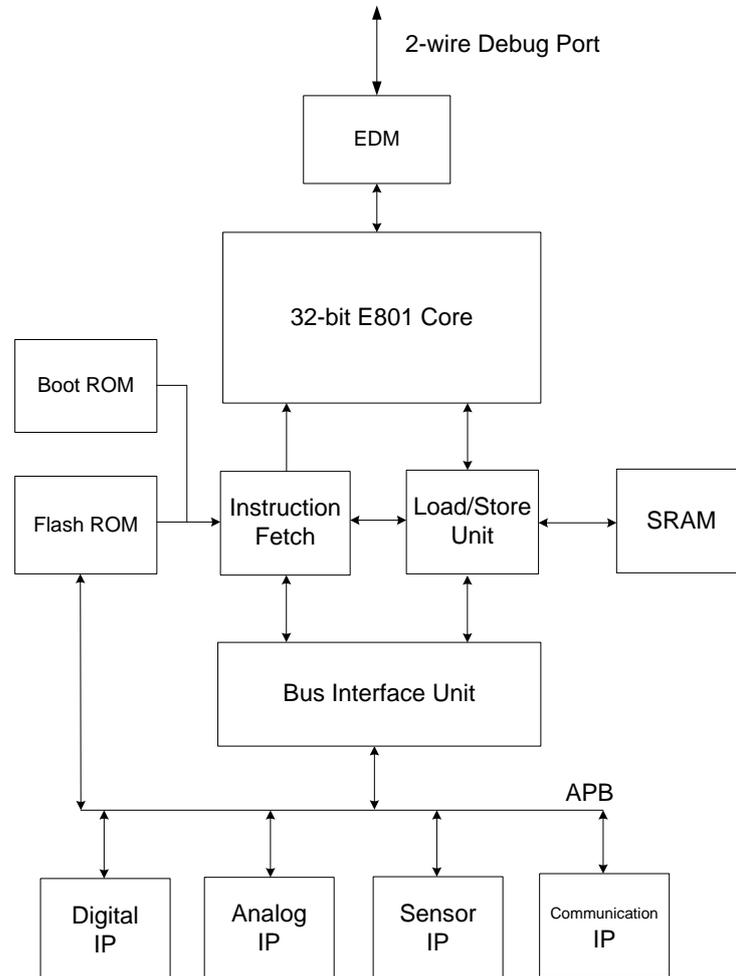
Figure 4-2 Building Block Diagram

4.3. Related Description and Supporting Document

File Name	Description
UG-HY16F3910	HY16F3910 User's Guide
APD-HY16F39IDE001	HY16F3910 C Library Manual
APD-HY16F39IDE002	HY16F3910 IP User's Manual
APD-HY16IDE030	HY16F Series IDE Software User's Manual(AndeSightV3.x Version) / HY16F Series Device Installer
APD-HY16F39IDE003	HY16F3910 IDE Hardware User's Manual
APD-HYIDE020	HY10000-WK09 Writer kit User's Manual

4.4. Clock System Network

NOTE :
Workable condition : CPU clock have to equal to UART clock
OK example1 : MCUCKS=HS_CK, CKHS=HSXT, TUCKS=HSXT
OK example2 : MCUCKS=HS_CK, CKHS=HSRC, TUCKS=HSRC
NG example1 : MCUCKS=HS_CK, CKHS=HSRC, TUCKS=HSXT
NG example2 : MCUCKS=HS_CK, CKHS=HSXT, TUCKS=HSRC

NOTE :
Workable condition : CPU clock have to equal to UART2 clock
OK example1 : MCUCKS=HS_CK, CKHS=HSXT, TU2CKS=HSXT
OK example2 : MCUCKS=HS_CK, CKHS=HSRC, TU2CKS=HSRC
NG example1 : MCUCKS=HS_CK, CKHS=HSRC, TU2CKS=HSXT
NG example2 : MCUCKS=HS_CK, CKHS=HSXT, TU2CKS=HSRC
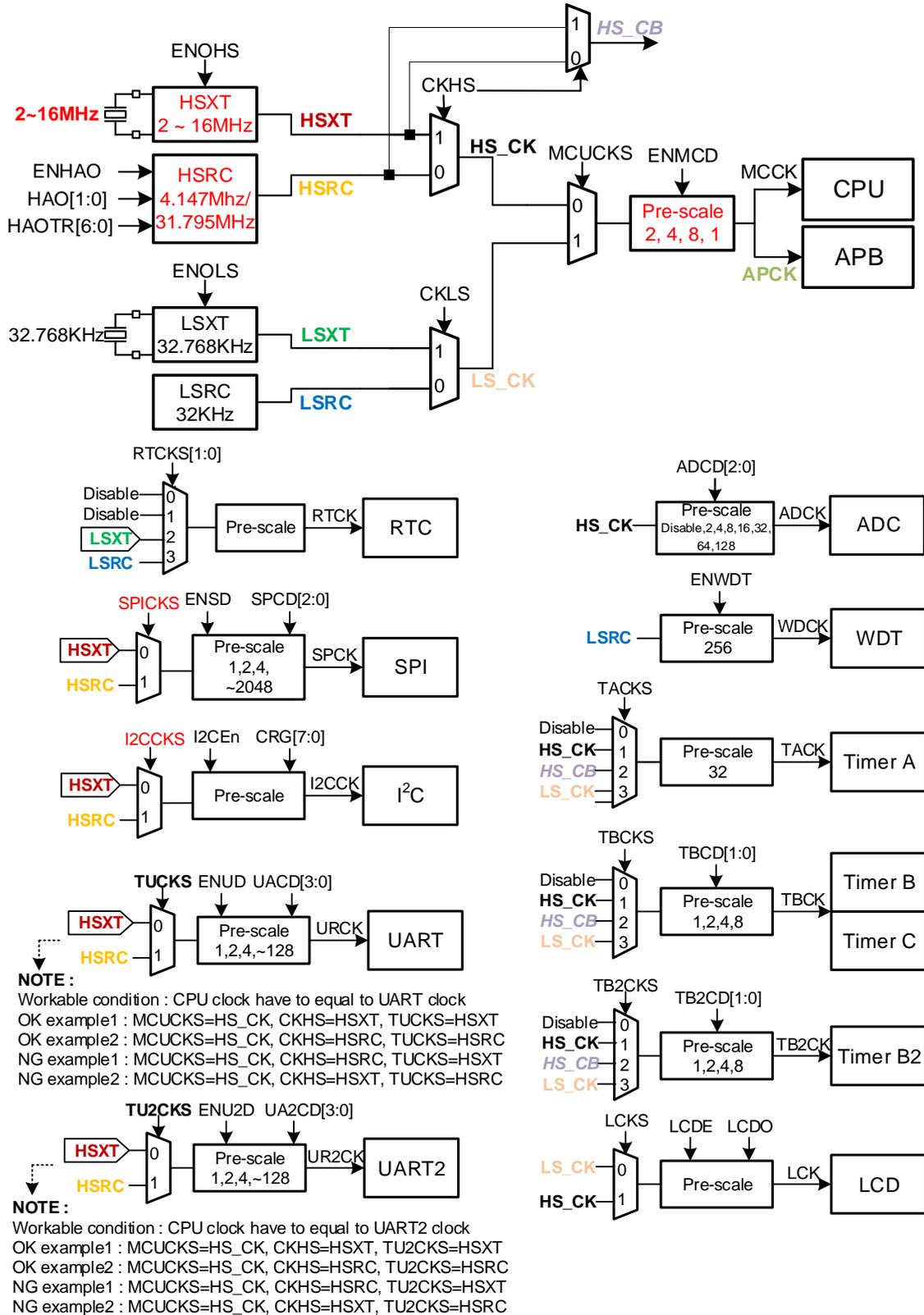
4.5. Power System Network
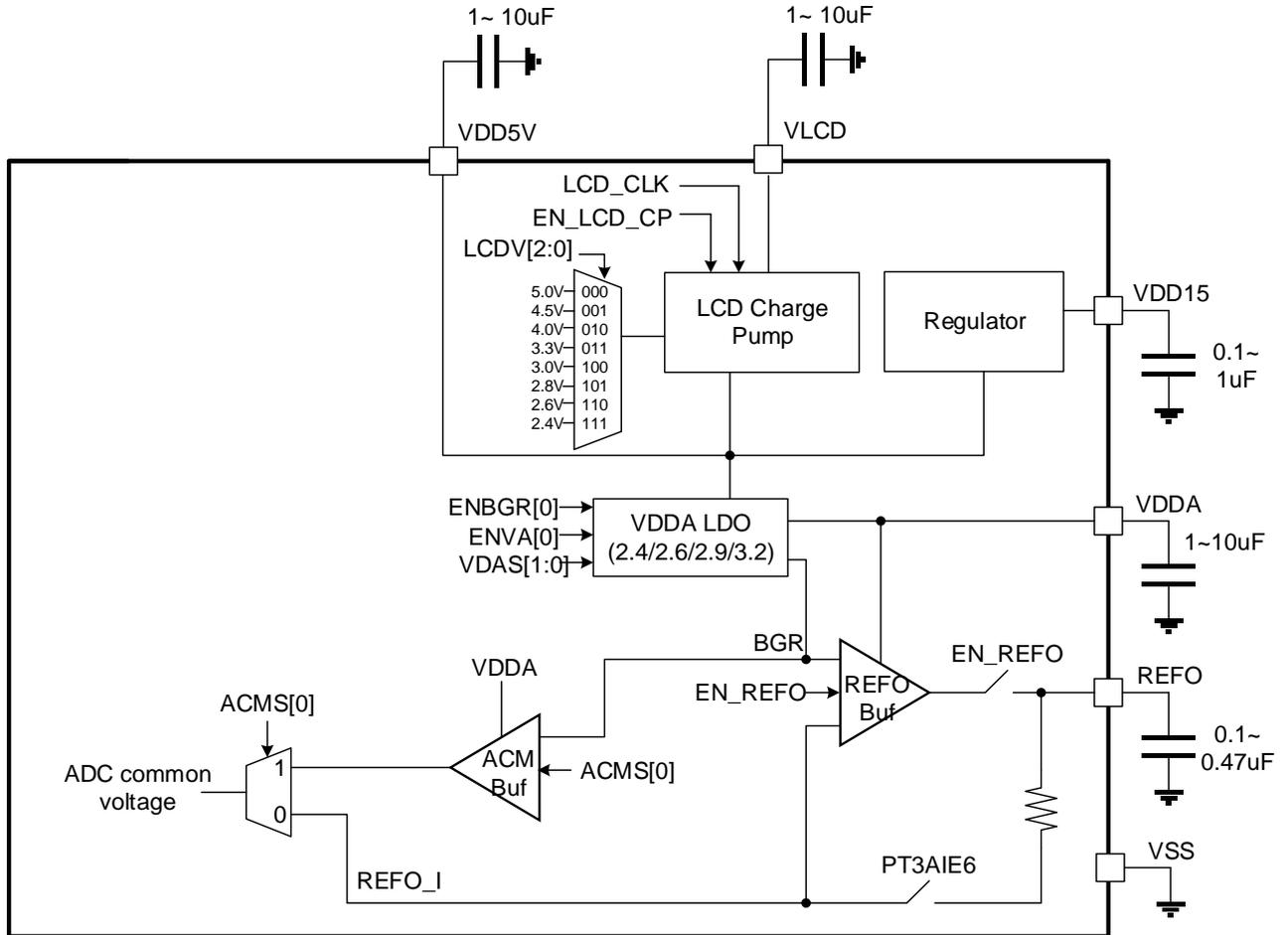
4.6. 24-bit ΣΔADC Network
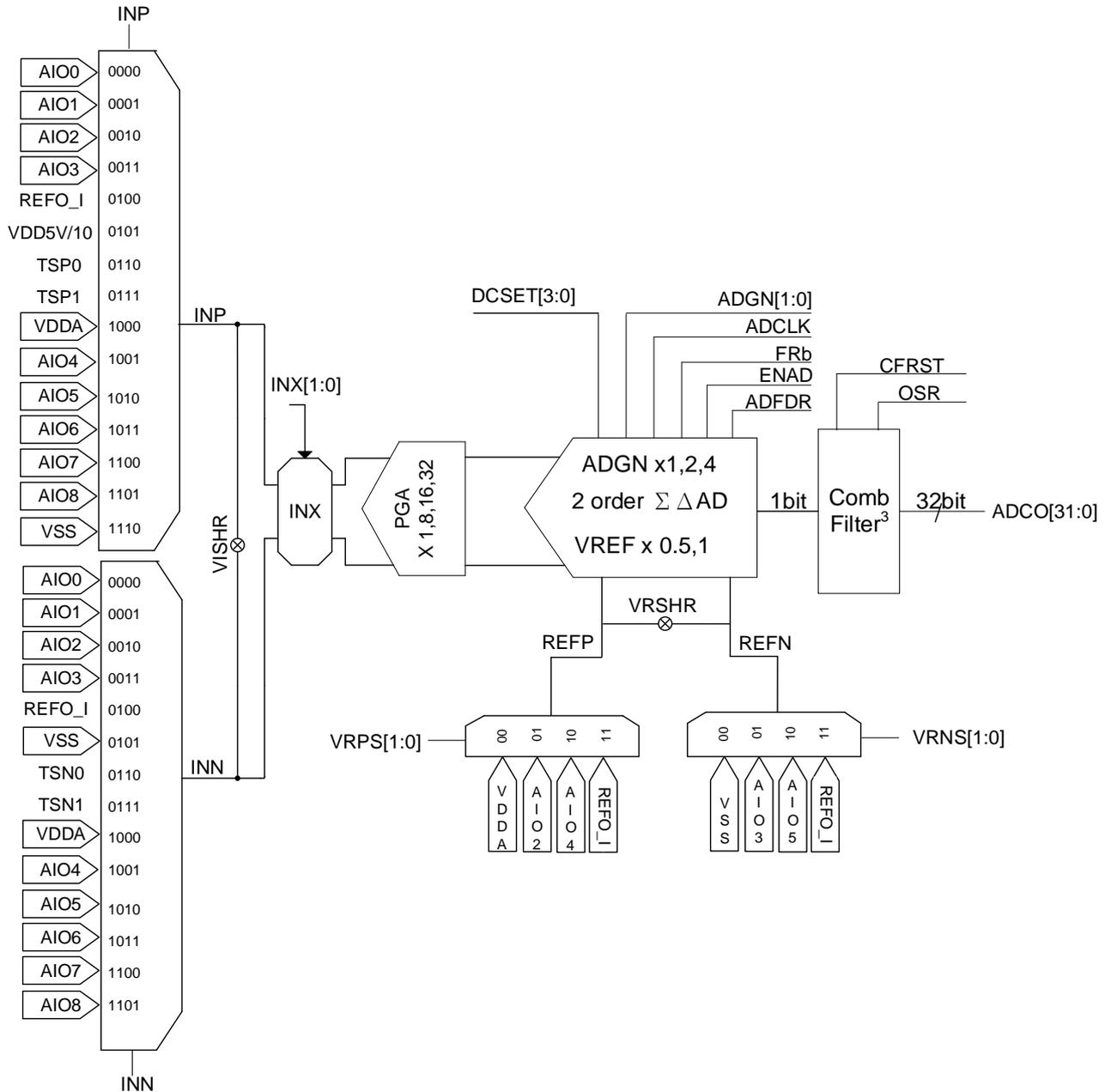
4.7. Low voltage Comparator Network
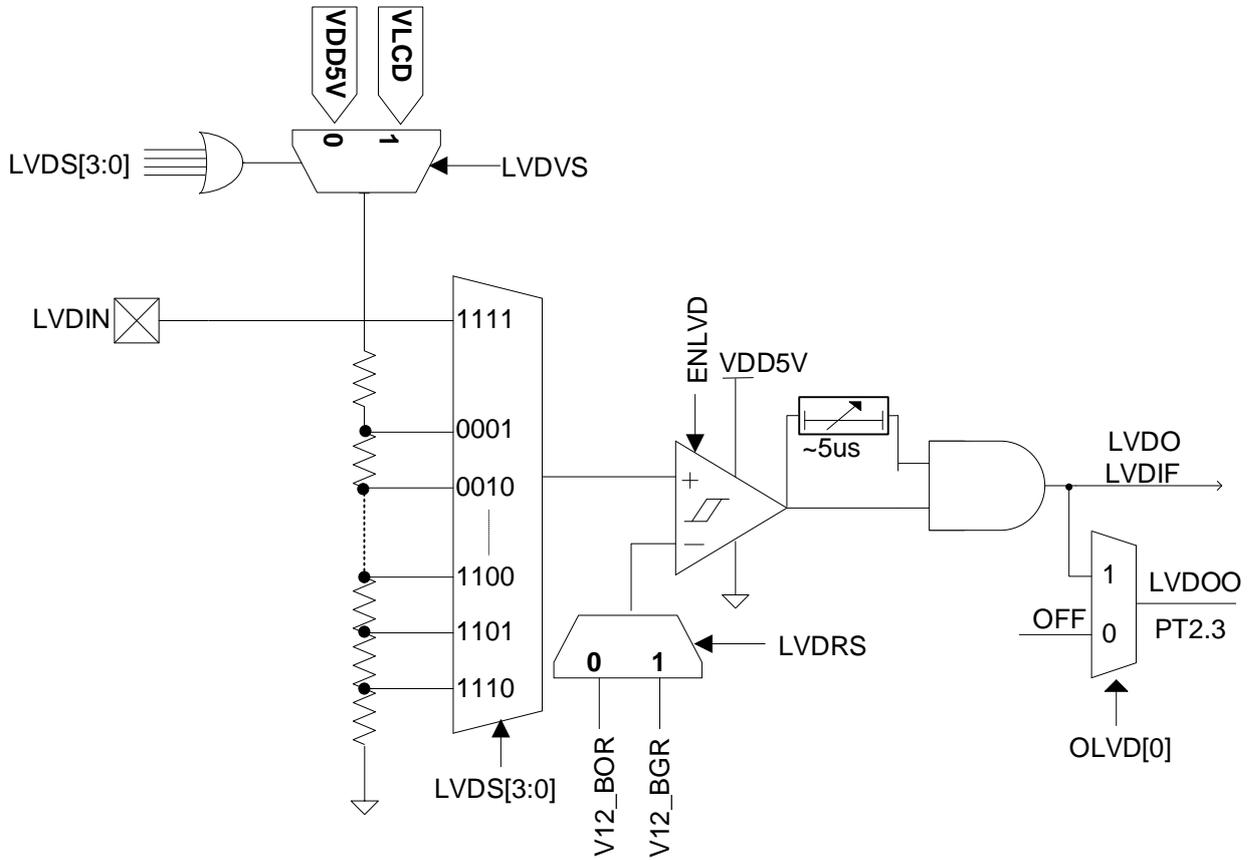
4.8. Watch Dog Timer Network
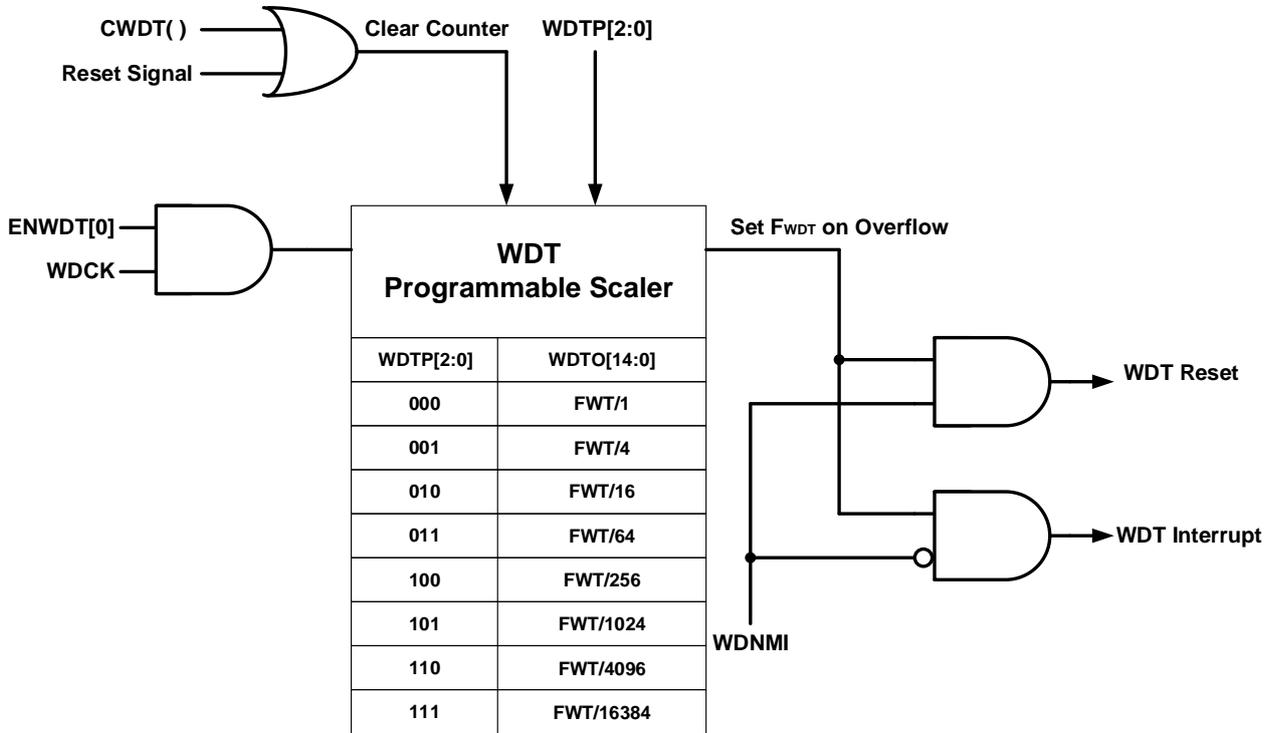
4.9. Timer A Network
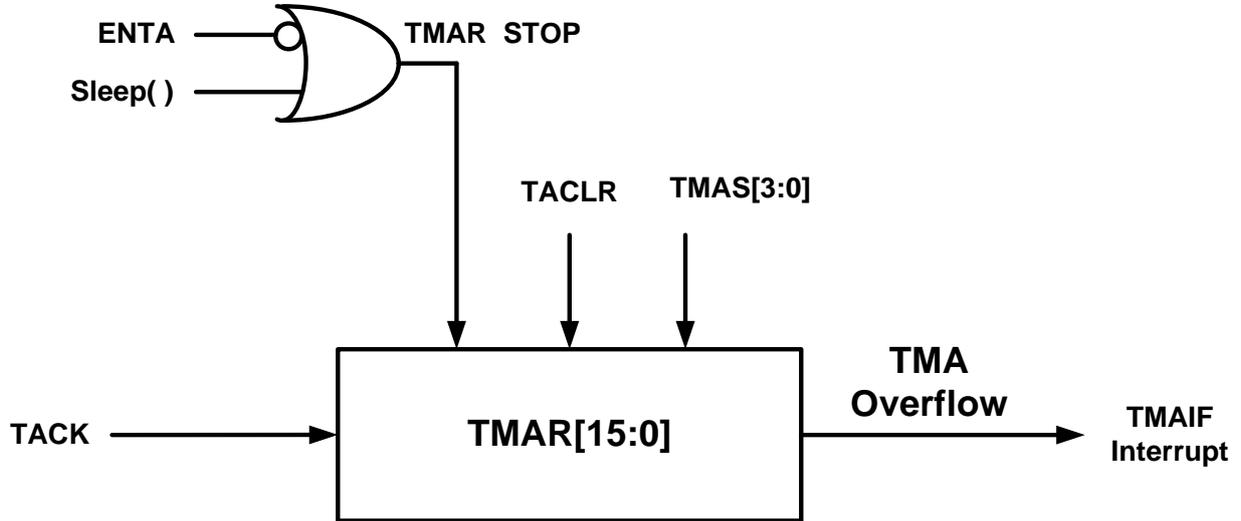
TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

4.10. Timer B Network
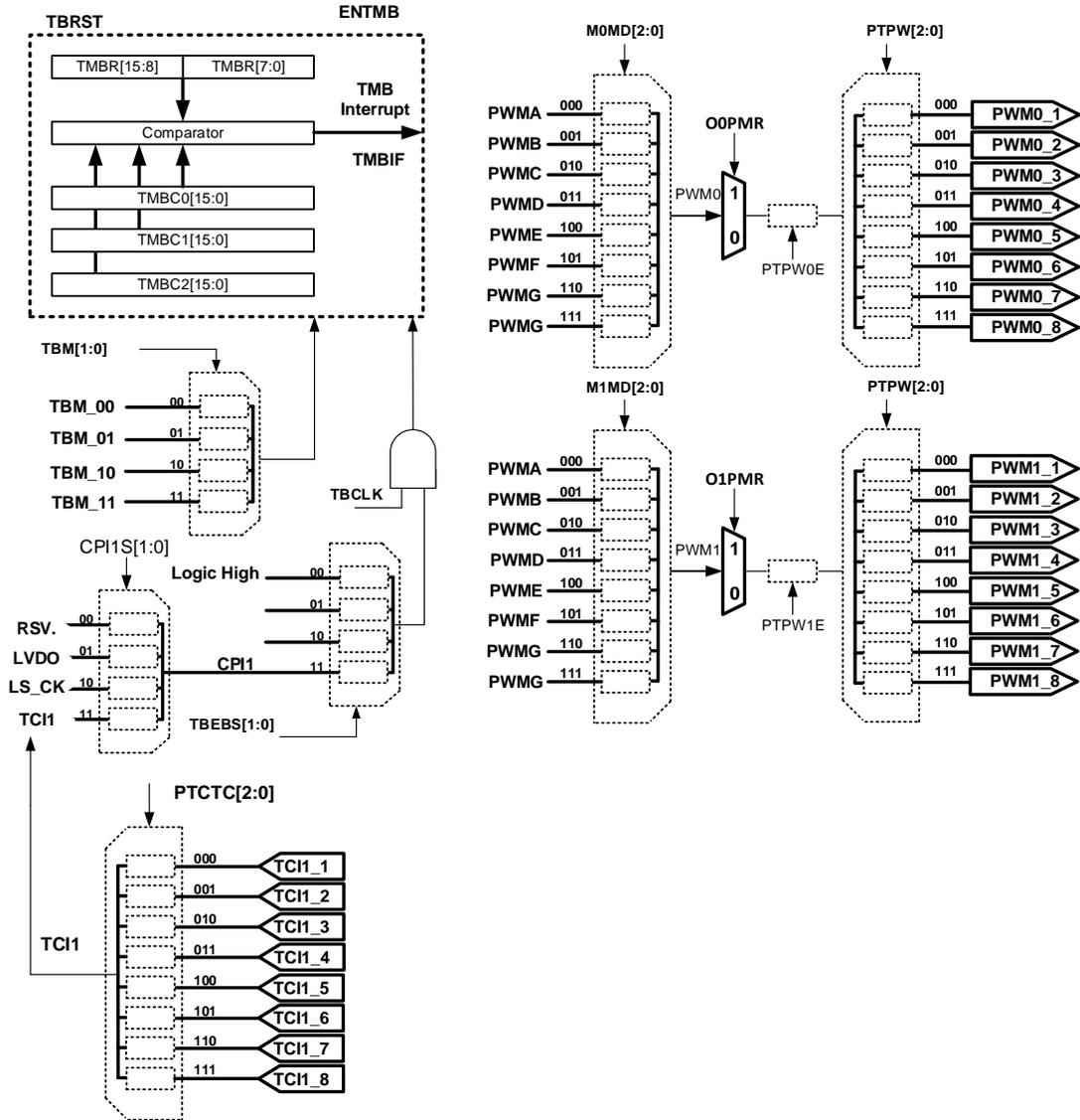
4.11. Timer C Network
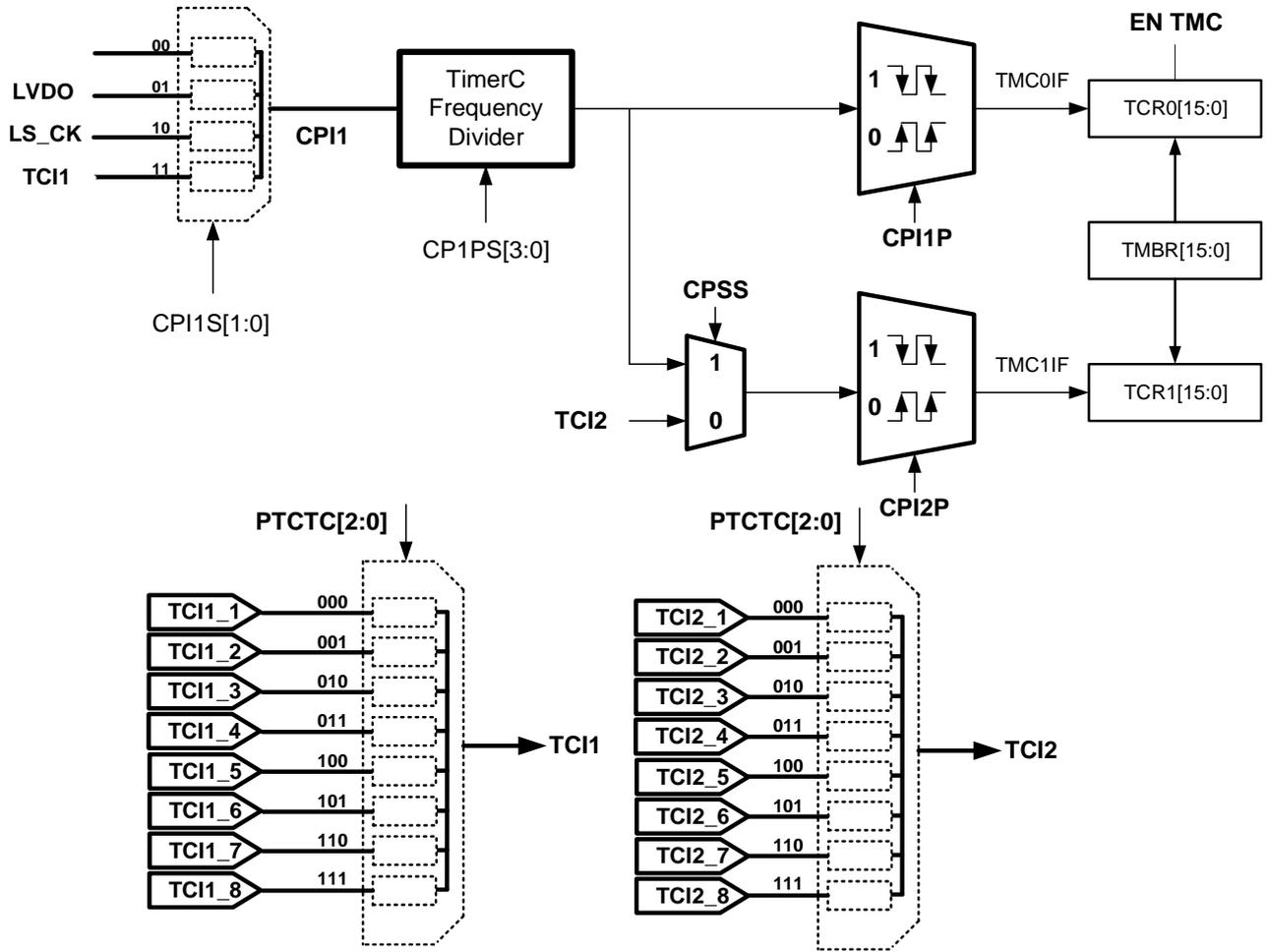
CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

4.12. Timer B2 Network

4.13. 32-bit SPI Diagram

Master   Slave

MSBit   LSBit   MSBit   LSBit

| shift register | SDIx   SDO | shift register |
                            MISO

| shift register | SDOx   SDI | shift register |
                            MISO

Read Buffer   Write Buffer

SPI Controller   SPI Clock Generator   SCKx   SCK

                            CSx   CS   SPI Controller
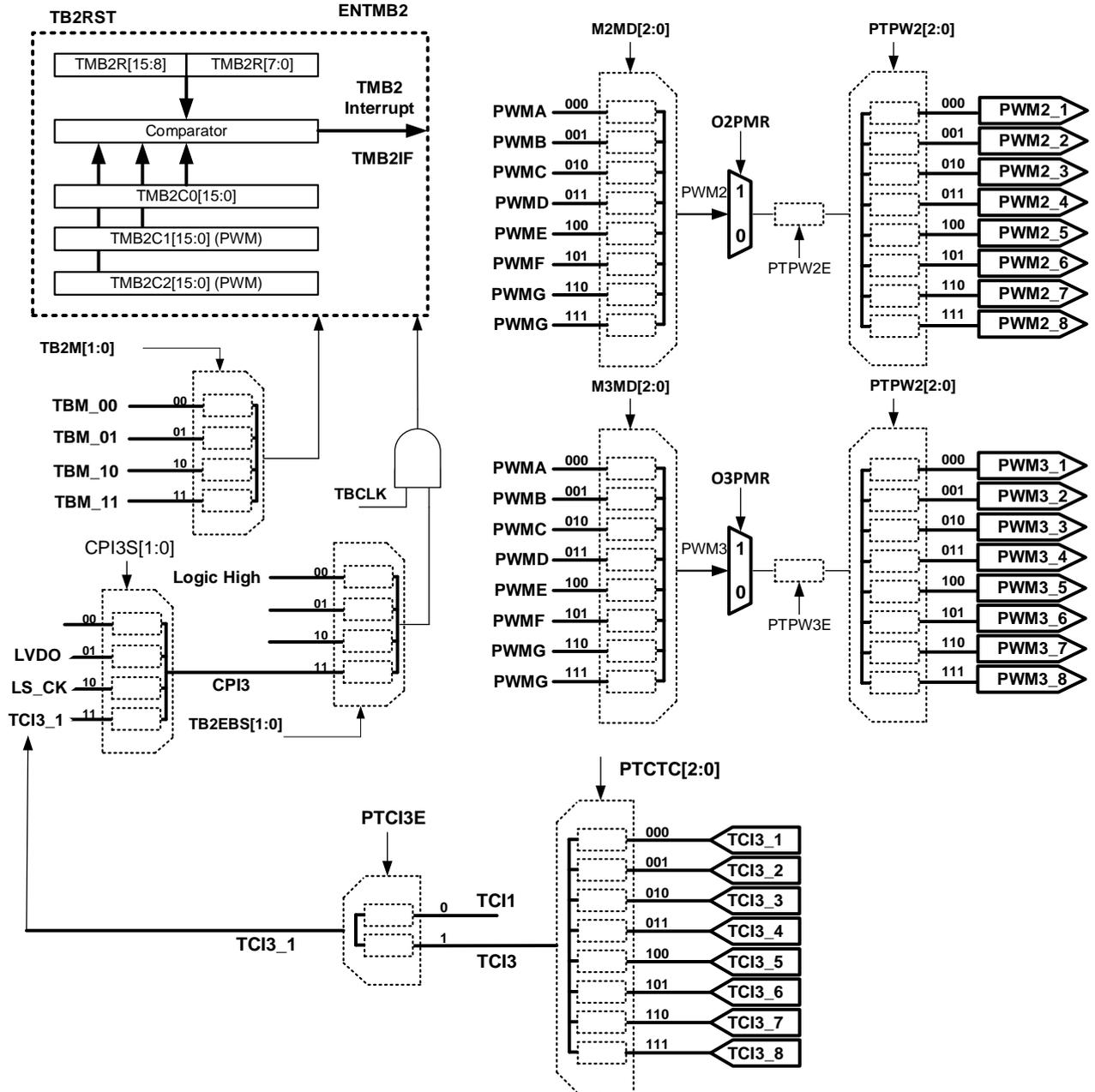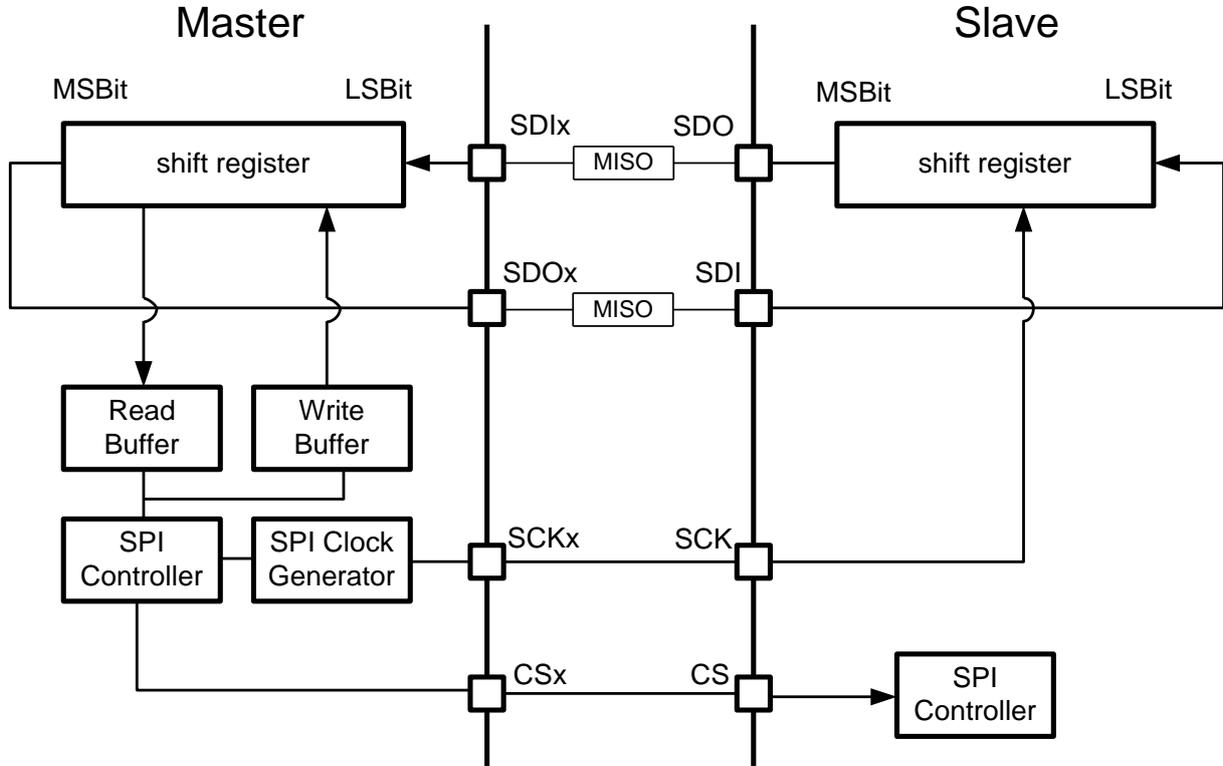
4.14. UART1/UART2 Block Diagram
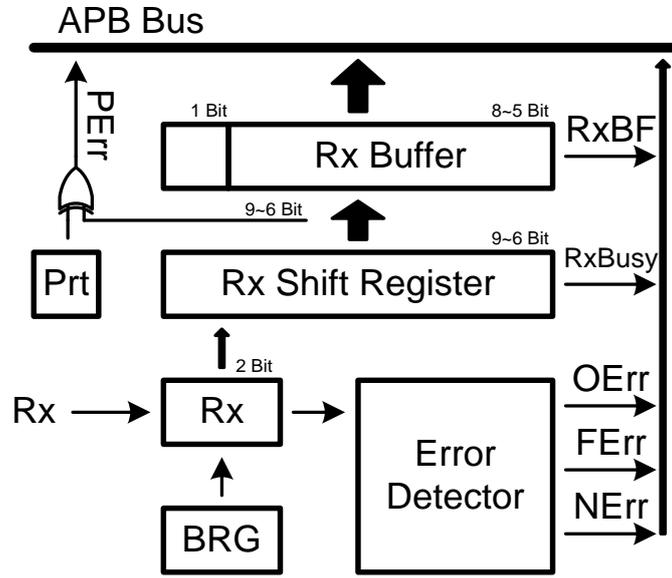
UART Receive Block Diagram

4.15. I²C Block Diagram
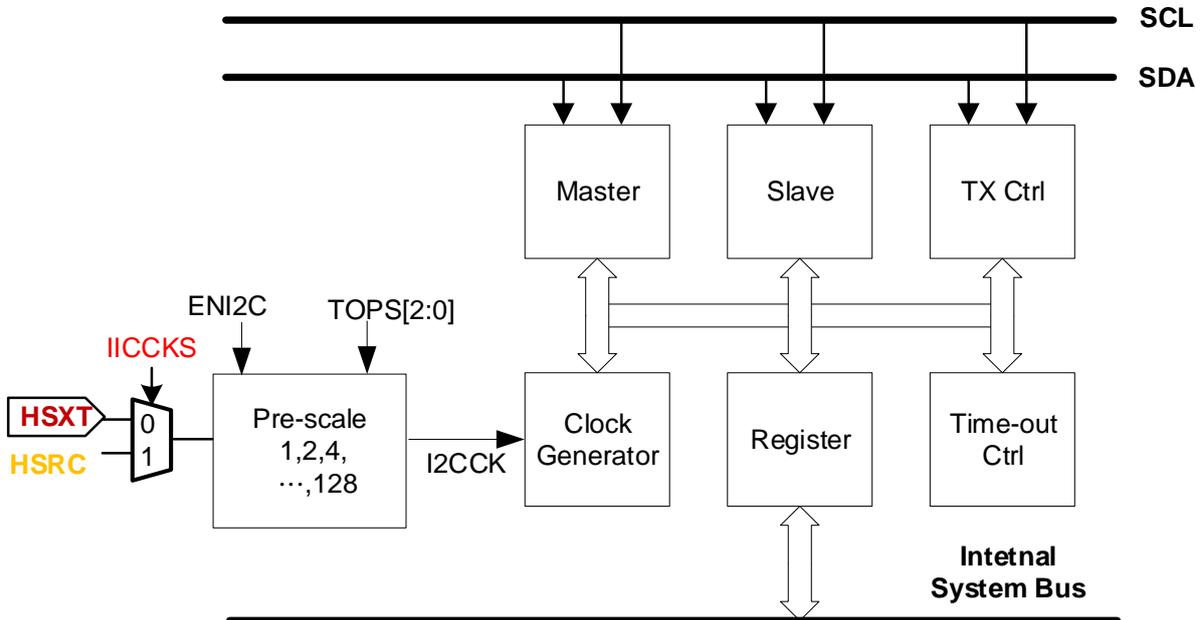
4.16. Hardware RTC Block Diagram
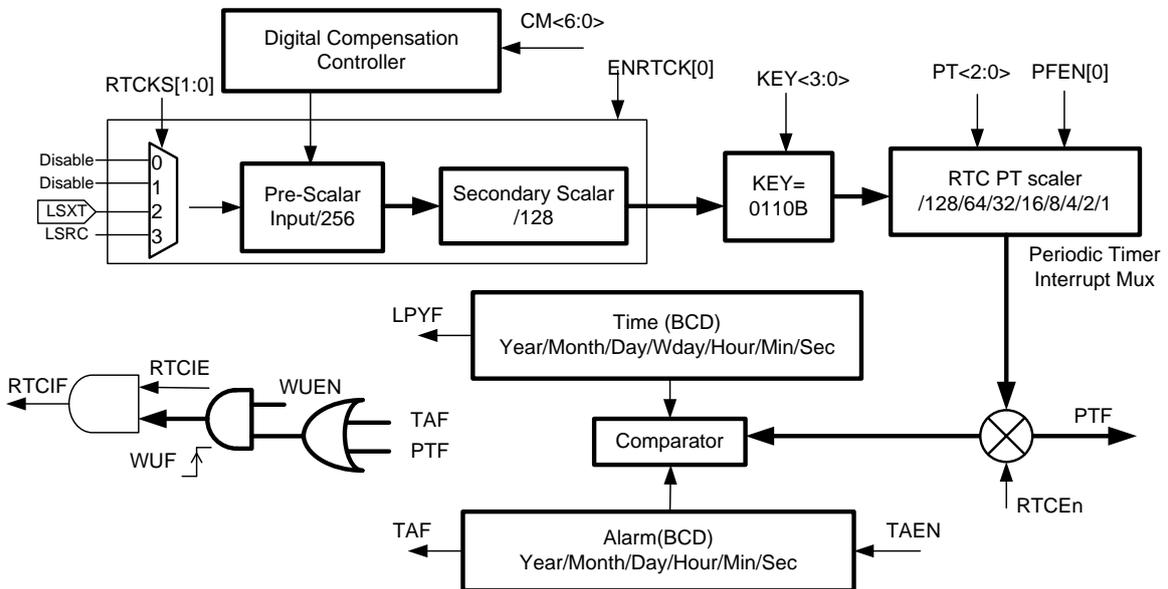
4.17. LCD Block Diagram
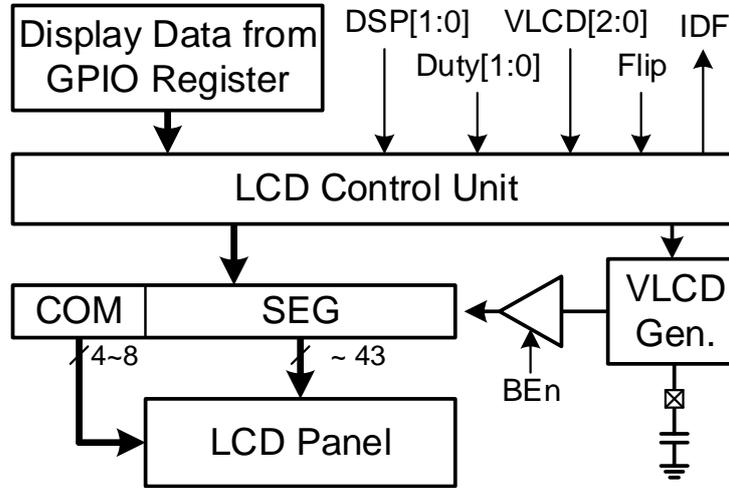
4.18. Reset/BOR1/BOR2 Block Diagram
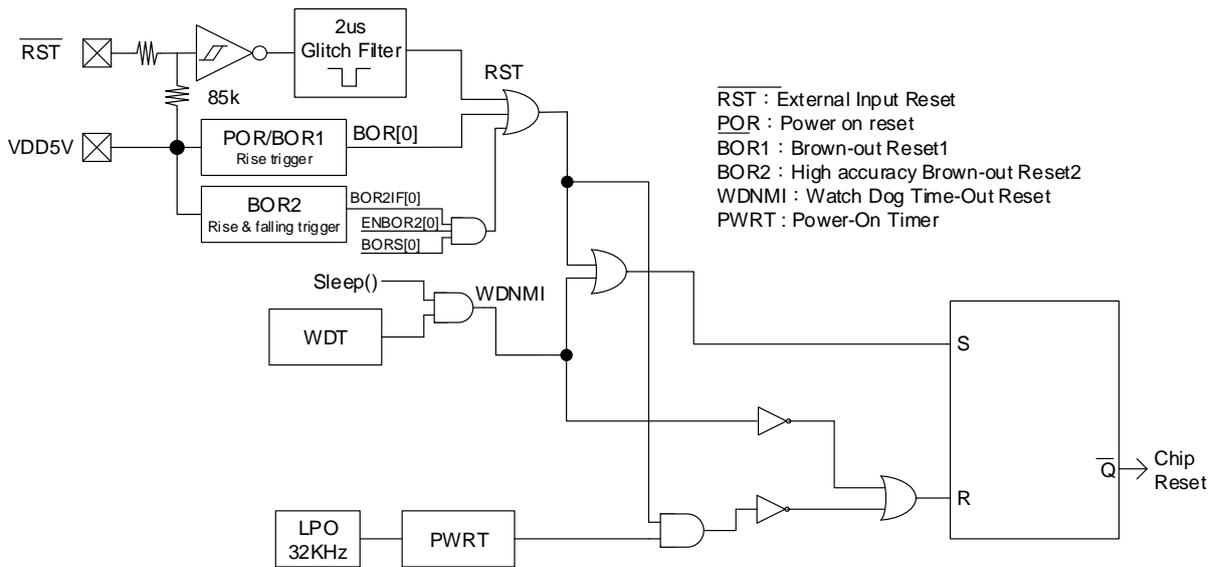
$\overline{RST}$: External Input Reset
$\overline{POR}$: Power on reset
BOR1 : Brown-out Reset1
BOR2 : High accuracy Brown-out Reset2
WDNMI : Watch Dog Time-Out Reset
PWRT : Power-On Timer

4.19. PT Port 1~2 Block Diagram
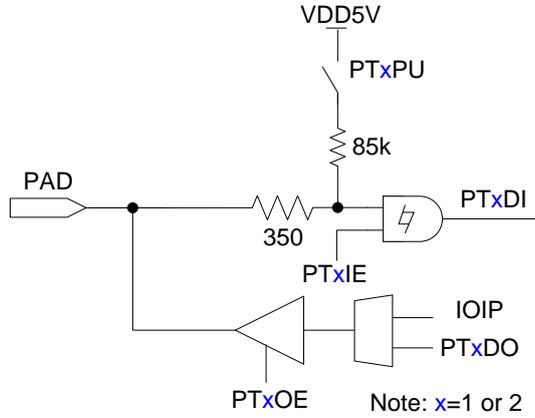
4.20. PT Port3 Block Diagram
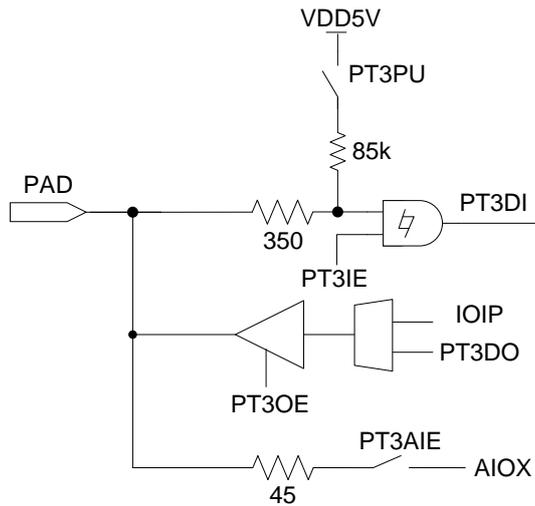
4.21. PT Port6~10、13 Block Diagram
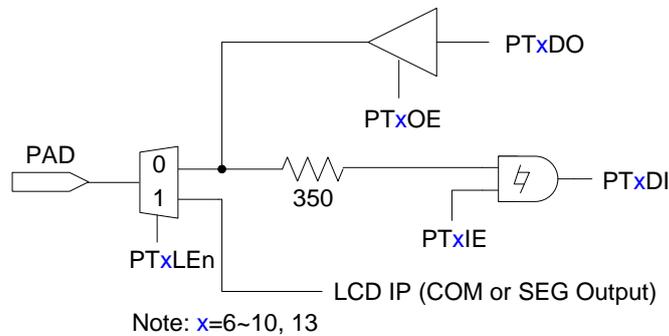
5. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD5V to VSS ……………………………………………………………−0.2 V to 6.0 V
Voltage applied to any pin …………………………………………………........... −0.2 V to VDD5V + 0.3 V
Diode current at any device terminal………………………….……..………………………………… ±2mA
Storage temperature, Tstg: (UN programmed device) .... −55℃ to 150℃

(Programmed device) ……………………………..………….. −40℃ to 85℃
Soldering Temperature (10 Sec) ……………………………………………………………………… +260°C
Maximum output current sink by any PORT1 to PORT13 I/O PIN ……….…………………………20mA

5.1. Recommended Operating Conditions

VDD= VDD5V= 3.0V, TA=25℃, Unless Otherwise Noted

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD5V	Digital power	2.0		5.5	V
Supply Voltage	VDDA	Analog power	2.4		3.6	V
Supply Current	I_Sleep	Sleep Mode, @BOR2 OFF, VDD15 low power mode		1.8	4	uA
	I_Idle01	LSRC=32KHz, MCCK= LSRC/1, LSRC(LPO) IDLE Mode		4.5	8	uA
	I_Idle02	LSXT=32768Hz MCCK= LSRC/1, LSXT IDLE Mode		6	12	uA
	I_Idle03	HSRC=4.147MHz, MCCK= HSRC /1, HSRC IDLE Mode		80	120	uA
	I_Idle04	HSRC=31.795MHz, MCCK= HSRC /2, HSRC IDLE Mode		275	410	uA
	I_Free Run01	HSRC=4.147MHz, MCCK= HSRC/1		0.7		mA
	I_Free Run02	HSRC=31.795MHz, MCCK= HSRC /2,		2.5		mA
Power Up Delay	$t_{PU,DLY}$	Power on or wake up from sleep mode		4.1	7	ms

Note: HSRC=31.795MHz, MCCK= HSRC /2, CPU operate at VDD5V>=3V.

5.2. Clock System

Typical values are at T_A=25℃ and VDD= VDD5V= 3.0V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
External High Speed Oscillator						
VDD5V	Operation voltage		2.0		5.5	V
F_{XHS}	High speed oscillator frequency	OHS_HS = 0b			4	MHz
		OHS_HS = 1b			8	MHz
		OHS_HS = 1b			16	MHz
I_{XHS}	High speed oscillator current	F_{XHS} = 16MHz, OHS_HS = 1b		130		uA
D_{XHS}	Duty of high oscillator		40		60	%
External Low Speed Oscillator						
F_{XLS}	Low speed oscillator frequency	VDD5V = 2.0V ~ 5.5V		32.768		KHz
I_{XLS}	Low speed oscillator current			2		uA
D_{XLS}	Duty of low speed oscillator		40		60	%
Internal High Speed Oscillator						
F_{HAO}	Internal high speed oscillator frequency	F_{HAO} = 4.147MHz, F_{HAO} = 4.147MHz, after trim	-10% -2%	4.147	+10% +2%	MHz
		F_{HAO} = 31.795MHz, F_{HAO} = 31.795MHz, after trim	-10% -2%	31.795	+10% +2%	MHz
	Voltage coefficient	VDD5V = 2.0V ~ 5.5 V		1		%
T_{HAO}	Temperature coefficient	-40~85℃		5		%
I_{HAO}	Internal high speed oscillator current	F_{HAO} = 4.147MHz		50		uA
		F_{HAO} = 31.795MHz (VDD5V>= 3.0V)		180		uA
D_{HAO}	Duty of oscillator		40		60	%
WT_{HAO}	Wake up time	F_{HAO} = 4.147MHz		15		us
Internal Low Speed Oscillator						
F_{LPO}	Internal low speed oscillator frequency		-20%	32	+20%	KHz
	Voltage coefficient	VDD5V = 2.0V ~ 5.5V		1		%
T_{LPO}	Temperature coefficient	-40~85℃		5		%
I_{LPO}	Internal low speed oscillator current			2.5		uA
D_{LPO}	Duty of low speed oscillator		40		60	%
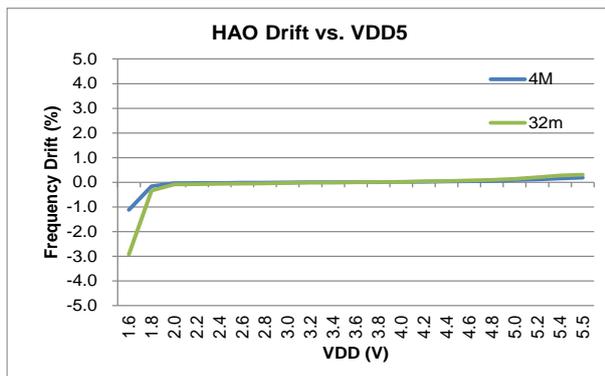
Figure5.2-1 HAO vs. VDD5V
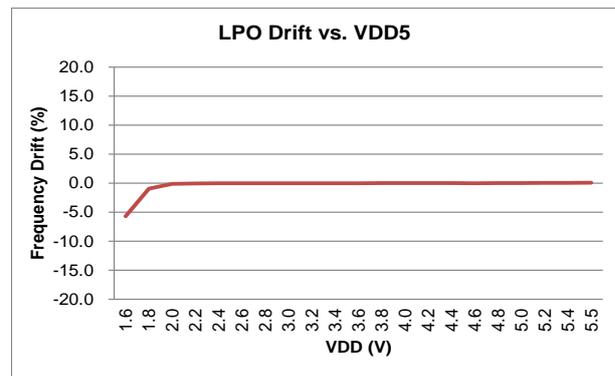
Figure5.2-2 LPO vs. VDD5V
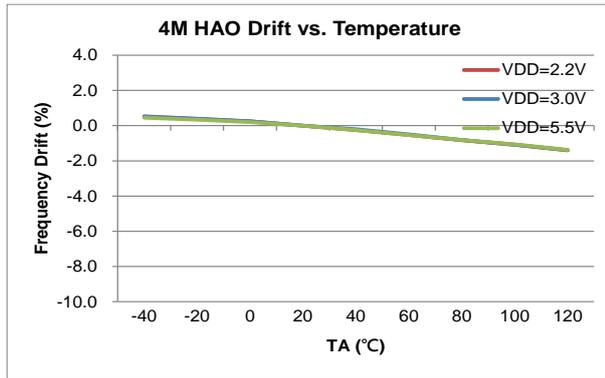
Figure5.2-3 HAO vs. Temperature
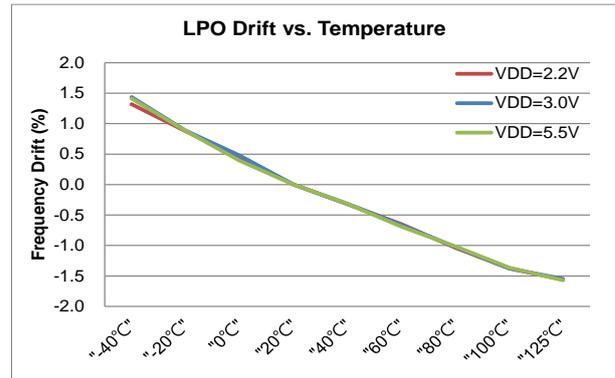
Figure5.2-4 LPO vs. Temperature

5.3. Power Management System

Typical values are at T_A=25℃ and VDD= VDD5V= 3.0V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA LDO (Analog power)						
	Output voltage error		-5		5	%
	Capacitor loading		0.1	1	10	uF
	Settling time	Capacitor loading = 0.1uF, 99% of VDDA		100		us
	Operation current	Bias + Band gap + VDDA LDO		35	50	uA
	Dropout voltage	VDD=2.9V, VDAS[1:0]=10b, I_L=10mA		0.4		V
	Select VDDA output voltage, VDD=5.5V, I_L=0.1mA	VDAS[1:0]=00b	-5%	2.4	+5%	V
		VDAS[1:0]=01b		2.6		
		VDAS[1:0]=10b		2.9		
		VDAS[1:0]=11b		3.2		
	Select VDDA output voltage, VDD=2.6V, I_L=10mA	VDAS[1:0]=00b	-6%	2.4	+5%	V
	Voltage coefficient	VDD5V = 2.5 ~ 3.6V		0.2		%/V
		VDD5V = 3.6 ~ 5.5V		0.2		%/V
	Temperature coefficient			100		ppm/℃
VDD15 LDO (Digital Core power)						
	Output voltage		1.35	1.5	1.65	V
	Capacitor loading		0.1	0.47	1	uF
	Dropout voltage	Load = 10mA		0.2		V
	Voltage coefficient	VDD5V= 2.0 ~ 3.6V		0.5		%/V
		VDD5V= 3.6 ~ 5.5V		1		%/V
	Temperature coefficient			200		ppm/℃
REFO Buffer (Bnadgap reference Buffer)						
	Output voltage		1.1	1.2	1.3	V
	Capacitor loading		0.022	0.1	1	uF
	Operation current			20		uA
	Output current		-1		1	mA
	Temperature coefficient	VDDA=2.9 V		80		ppm/℃
	Voltage coefficient	VDDA= 2.4V ~ 3.6V		0.2		%/V
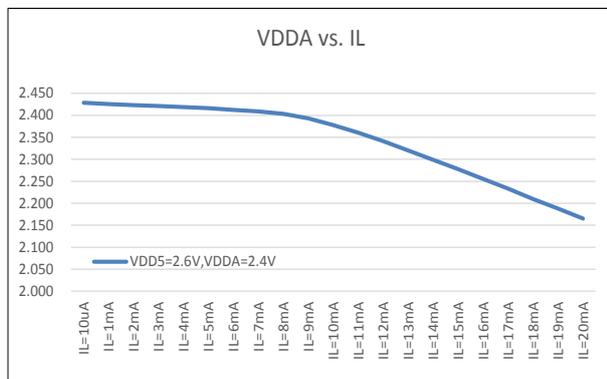
Figure5.3-1 VDDA vs. IL
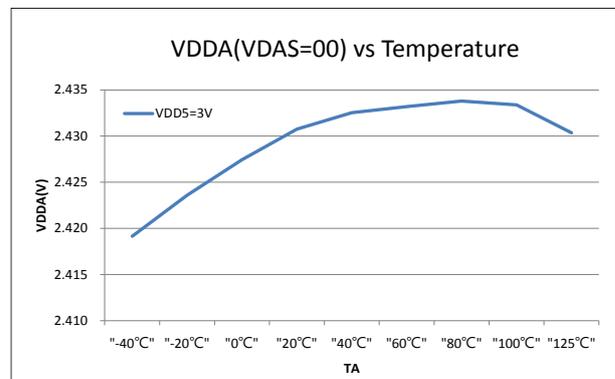
Figure5.3-2 VDDA vs. Temperature
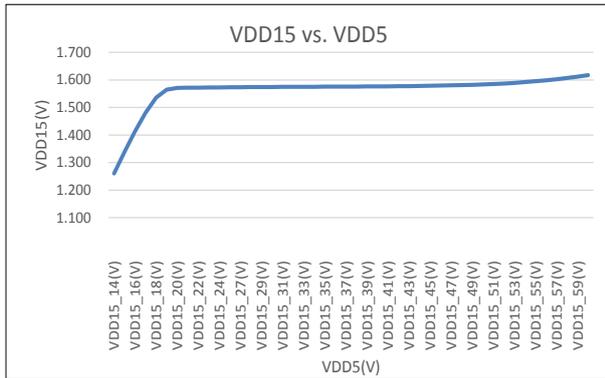
Figure5.3-3 VDD15 vs. VDD5V
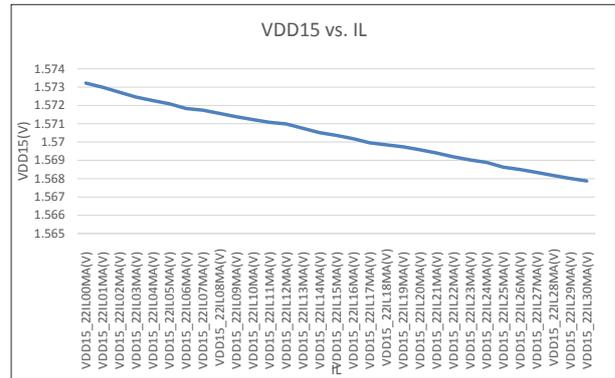

Figure5.3-4 VDD15 vs. IL
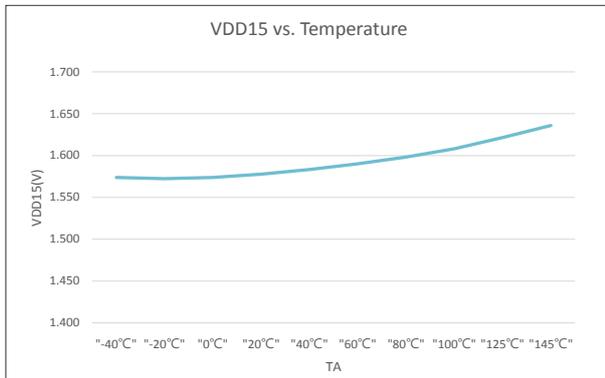
Figure5.3-5 VDD15 vs. Temperature
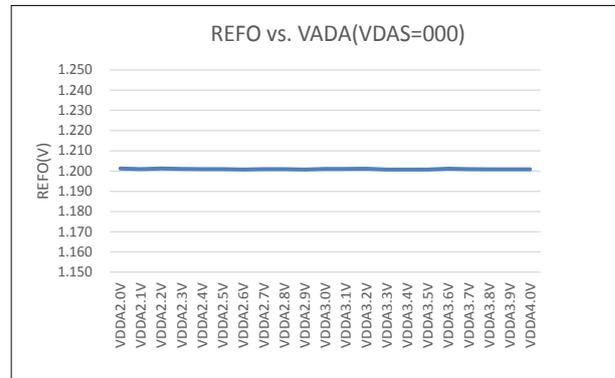
Figure5.3-6 REFO vs. VDDA
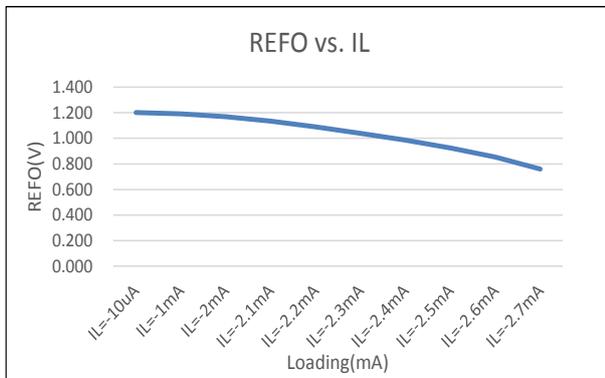
Figure5.3-7 REFO vs. IL
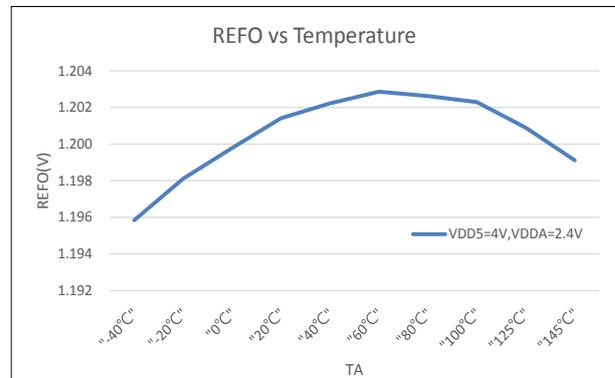
Figure5.3-8 REFO vs. Temperature

5.4. Reset Management System

Typical values are at T_A=25℃ and VDD= VDD5V= 3.0V, Unless otherwise noted.

Sym.	Parameter		Min.	Typ.	Max.	Unit
BOR1	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$		2			us
	V_{DD5V} Start Voltage to accepted reset internally (H➔L), V_{LVR1}		1.2	1.4	1.6	V
	Temperature drift, T_A=-40℃~85℃			30		%
	BOR1 current, I_{BOR1}, (include BOR1 and VDD15 LDO)			2.5	5	uA
BOR2	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR2}$		2			uS
	V_{DD5V} Start Voltage to accepted reset internally (L➔H), V_{HYS2}, and BORTH[2:0]:	000b		1.7		V
		001b		2.0		
		010b		2.2		
		011b		2.5		
		100b		2.7		
		101b		3.0		
		110b		3.6		
		111b		4.0		
	V_{DD} Start Voltage to accepted reset internally (H➔L), V_{LVR2}, and BORTH[2:0]:	000b~ 111b	13%	V_{HYS2}-0.06V	13%	V
	Hysteresis, $V_{HYS2\text{-}LVR2}$			60		mV
	BOR2 current, I_{BOR2}			10	15	uA
	Temperature Drift			5		%
RST	Pulse length needed as RST pin to accepted reset internally, $t_{d\text{-}RST}$		2			us
	Input Voltage to accepted reset voltage			1.1		V
	Reset release voltage			1.6		V

BOR1/BOR2：Brownout Reset 1/2

RST：External Reset pin
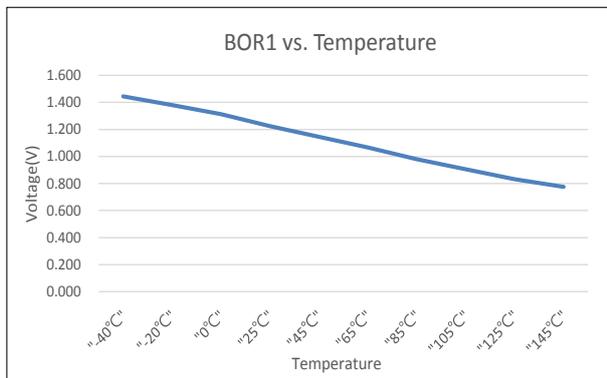
Figure5.4-1 BOR1 vs. Temperature
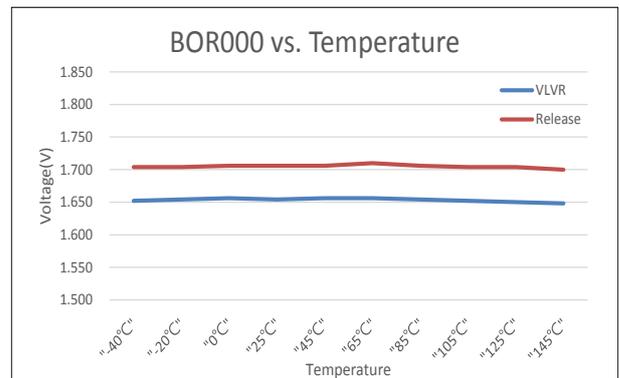
Figure5.4-2 BOR2 vs. Temperature

5.5. GPIO Port System

Typical values are at T_A=25℃ and VDD= VDD5V= 3.3V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PT 1 ~ 3 GPIO Port						
R_{PU}	Internal pull high resistor		65	85	105	kΩ
V_{IH}	Input high voltage		0.75*V_{DD5V}			V
V_{IL}	Input low voltage				0.3*V_{DD5V}	V
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*V_{DD5V}		V
I_{LKG}	Leakage Current				0.1	uA
V_{OH}	High-level output voltage	V_{DD5V} =3.3V, I_{OH}=-10mA,	V_{DD5V} -0.4			
		V_{DD5V} 5V, I_{OH}=-15mA,	V_{DD5V} -0.4			
V_{OL}	Low-level output voltage	V_{DD5V} =3.3V, I_{OL}=10mA			V_{SS} +0.4	
		V_{DD5V} =5V, I_{OL}=15mA			V_{SS} +0.4	
PT 6 ~ 10、13 GPIO Port						
R_{PU}	Internal pull high resistor			NA		
V_{IH}	Input high voltage		0.75*V_{DD5V}			V
V_{IL}	Input low voltage				0.3*V_{DD5V}	V
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*V_{DD5V}		V
I_{LKG}	Leakage Current				0.1	uA
V_{OH}	High-level output voltage	V_{DD5V} =3.3V, I_{OH}=10mA,	V_{DD5V} -0.5			
		V_{DD5V} =5V, I_{OH}=15mA,	V_{DD5V} -0.5			
V_{OL}	Low-level output voltage	V_{DD5V} =3.3V, I_{OL}=-10mA			V_{SS} +0.4	
		V_{DD5V} =5V, I_{OL}=-15mA			V_{SS} +0.4	
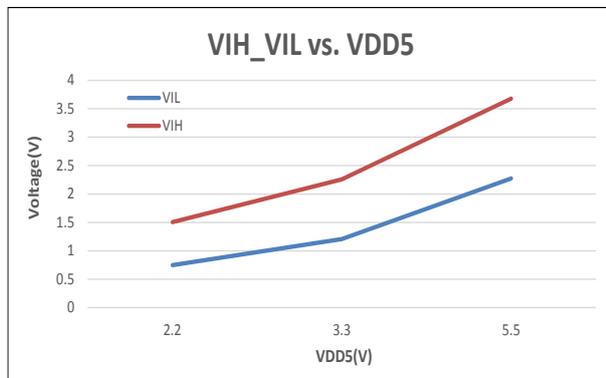
Figure5.4-1 VIH/VIL vs. VDD5V

5.6. ADC Management System

All specifications at T$_A$=-40℃ to +85℃, VDDA=REFP=2.4V, REFN=VSS, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Analog Inputs						
	Full-scale input voltage (VINP - AINN)	Considering ADC performance matches ADC ENOB table. REFP=VDDA, REFN=VSS VREF be set to 1/2 only		±0.5*VREF/Gain		V
		Considering ADC performance matches ADC ENOB table. REFP=REFO_I REFN=VSS VREF be set to 1 only		±VREF/Gain		
	Common-mode input range	Gain = 1, @25℃	VSS-0.2V		VDDA	V
System Performance						
	Resolution	No missing codes		24		Bits
	Data rate			ADC Clock /OSR		SPS
	Digital filter settling time	Full setting		3		Data
	Integral nonlinearity (INL)	Differential input End-point fit, OSR=65536		30		PPM
	ADC Gain drift			5	10	ppm/ ℃
	Normal-mode rejection	f$_{IN}$=60Hz ±1Hz, Output rate = 15 SPS		70		dB
	Common-mode rejection	ΔVDDA = 0.1V @ DC		80		dB
	Input-referred noise	Output rate= 31 SPS, ADC Gain=1		2.04		uV, rms
	Power-supply rejection	ΔVDDA = 0.1V @ DC		80		dB
Voltage Reference Input						
	Voltage reference input	VREF = REFP - REFN			VDDA	V
	Positive Reference Input	REFP, @25℃	VDDA/2		VDDA	V
	Negative Reference Input	REFN, @25℃	VSS		VDDA/2	V
ADC Modulator Current						
ADC	ADC Modulator	VDD5V=3.3V,VDDA=2.4V, ADC Clock=1Mhz		300		uA
PGA	ADC PGA	VDD5V=3.3V,VDDA=2.4V		700		uA

ADC ENOB and RMS Noise

Typical values are at TA=25℃ and VDD5V(VDD) = 3.3V, VDDA=2.4V and A/D Clock=4M/4=1MHz, unless

otherwise noted. HY16F3910 provides important input noise specification that aims at ΣΔADC. Below two Tables lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short with 1K load cell, voltage reference: 1.2V and 1024 records were sampled.

NOTE : Because the settable over-sampling rate (OSR) range is 64~32768, the output rate range that HY16F3910 can support is **15625Hz~31Hz**. Below two tables do not show the ADC ENOB and RMS Noise performance of each stage of OSR.

ENOB(RMS) with OSR/GAIN at CPUCK=4MHz, A/D Clock=4M/4=1MHz, VDDA=2.4V, VREF=AI2-AI3=VDDA-VSS,VRGN=0.5, Vin=AI0-AI1,ext short with 1K load cell									
OSR					**128**	**512**	**2048**	**8196**	**32768**
Output rate(Hz)					**7813**	**1953**	**488**	**122**	**31**
Gain	**=**	**PGAGN**	**x**	**ADGN**					
1	=	off	x	1	16.48	17.5	18.47	19.15	20.18
2	=	off	x	2	16.38	17.61	18.19	19	20.25
3	=	off	x	3	16.22	17.22	18.17	19.06	20.19
4	=	off	x	4	15.84	16.92	17.97	19	20.34
8	=	8	x	1	16.5	17.52	18.43	19.07	19.7
16	=	16	x	1	16.13	17.11	18.18	19.09	19.7
32	=	32	x	1	16.15	16.81	17.63	18.83	19.71
32	=	8	x	4	15.3	15.94	17.23	18	19.05
64	=	16	x	4	14.55	15.77	16.67	17.53	18.44
128	=	32	x	4	14.18	15.14	16.2	17.37	18.15

RMS Noise(uV) with OSR/GAIN at CPUCK=4MHz, A/D Clock=4M/4=1MHz, VDDA=2.4V, VREF=AI2-AI3=VDDA-VSS, VRGN=0.5; Vin=AI0-AI1, ext.short with 1K load cell									
OSR					**128**	**512**	**2048**	**8196**	**32768**
Output rate(Hz)					**7813**	**1953**	**488**	**122**	**31**
Gain	**=**	**PGAGN**	**x**	**ADGN**					
1	=	off	x	1	26.376	13.049	6.672	4.146	2.038
2	=	off	x	2	14.145	6.043	4.043	2.311	0.966
3	=	off	x	3	10.559	5.275	2.739	1.472	0.674
4	=	off	x	4	10.337	4.881	2.356	1.151	0.454
8	=	8	x	1	3.257	1.603	0.858	0.547	0.369
16	=	16	x	1	2.112	1.065	0.508	0.272	0.184
32	=	32	x	1	1.041	0.657	0.371	0.162	0.088
32	=	8	x	4	1.874	1.204	0.490	0.288	0.139
64	=	16	x	4	1.570	0.676	0.363	0.200	0.139
128	=	32	x	4	1.016	0.522	0.252	0.111	0.065

ADC Offset vs Temperature

VDD=3.3V, VDDA=2.4V
VR=AI2-AI3=ext.(VDDA-VSS)/2, OSR=32768
Vin=AI0-AI1, ext.Short (1KOhm load)
H/W Chopper

ADGN=1　ADGN=2　ADGN=3　ADGN=4

PGA Offset vs Temperature

VDD=3.3V, VDDA=2.4V
VR=AI2-AI3=ext.(VDDA-VSS)/2, OSR=32768
Vin=AI0-AI1, ext.Short (1KOhm load)
H/W Chopper

PGA=8　PGA=16　PGA=32　PGA 32 x ADGN 4

ADC Gain Ratio vs Temperature, VR=ext.1.2v
ADC Vin=0.6 x Full scale

VDD=3.3V, VDDA=2.4V,
Vin=AI0-AI1(FLUKE Diff. Input)
VR=AI2-AI3(Ext1.2v), VRGN=1, OSR=32768

ADGN1　ADGN2　ADGN3　ADGN4

PGA Gain Ratio vs Temperature, VR=ext.1.2v
PGA Vin=0.6 x Full scale

VDD=3.3V, VDDA=2.4V,
Vin=AI0-AI1(FLUKE Diff. Input)
VR=AI2-AI3(Ext1.2v), VRGN=1, OSR=32768

PGA8　PGA16　PGA32　PGA32 ADGN4
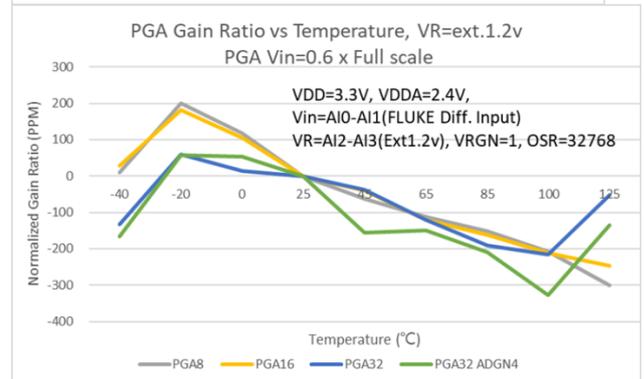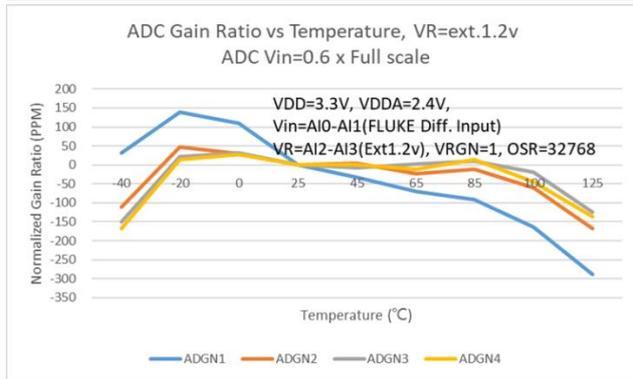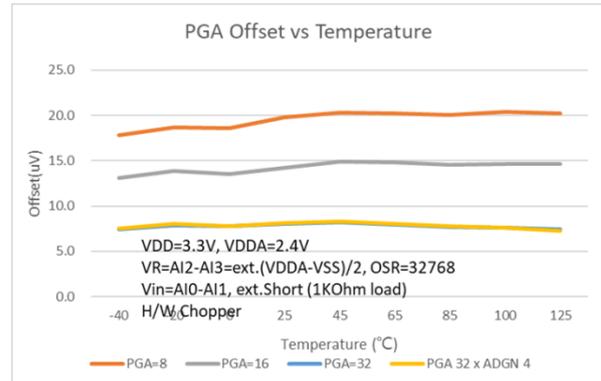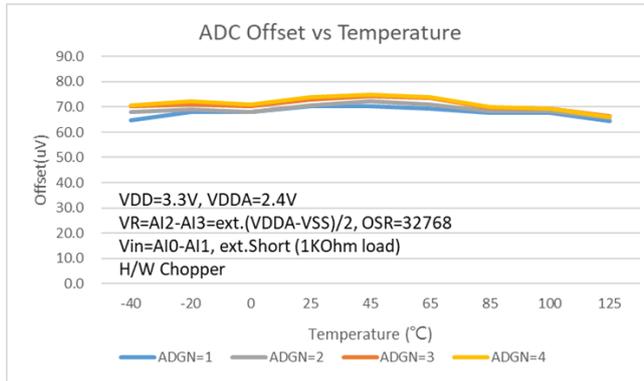
5.7. Internal Temperature Sensor

Typical values are at T_A=25℃, VDD= VDD5V= 3.0V, and VDDA=2.4V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			172		uV/℃
KT	Absolute temperature scale 0K			-286		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃
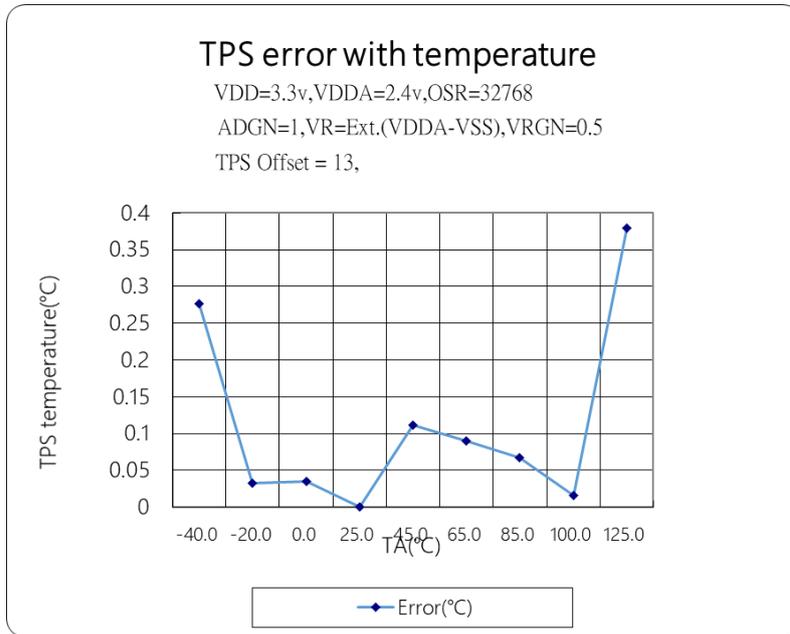
Figure5.8-1 ADC Temperature Sensor Error

5.8. LVD Comparator Management System

Typical values are at TA=25℃ and VDD= VDD5V= 3.0V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LVD	Operation current, I_{V12_BOR}			2.5		uA
	Operation current, I_{V12_BGR}			10		uA
	V12_BOR Reference Voltage		1.1	1.2	1.3	V
	V12_BOR Reference Voltage Temperature drift			200		PPM/℃
	V12_BOR Reference Voltage to VDD5V Voltage drift			±2		%/V
	V12_BGR Reference Voltage		1.15	1.2	1.25	V
	V12_BGR Reference Voltage Temperature drift			50		PPM/℃
	V12_BGR Reference Voltage to VDD5V Voltage drift			±2		%/V
	Compare reference voltage temperature drift, T_A = -40℃ ~ 85 ℃			50		ppm/℃
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1111b			LVDIN		V
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1110b			4.0		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1101b			3.6		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1100b			3.3		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1011b			3.0		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1010b			2.9		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1001b			2.8		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1000b		5%	2.7	5%	V
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0111b			2.6		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0110b			2.5		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0101b			2.4		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0100b			2.3		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0011b			2.2		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0010b			2.1		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0001b			2.0		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0000b			Off		

LVD：Low Voltage Detect
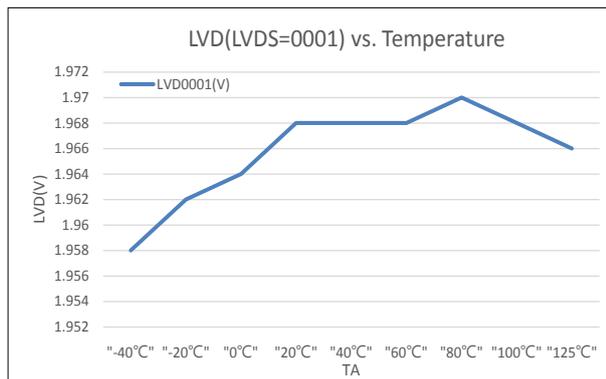
Figure5.8-1 LVD vs. Temperature

5.9. LCD System

Typical values are at T_A=25℃, VDD= VDD5V= 3.3V, and C_{VLCD}=4.7uF, Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LCD}	Operation Current Charge Pump Mode		W/O Panel		20		uA
V_{LCD}	Supply Voltage Range	VLCD	With Buffer, ENLCDP[0]=0b	2.5		5.5	V
		ENLCDP[0]=1b @VDD5V > 2.0V	VLCD=111b, @VDD5V>=2.75V		5.0		V
			VLCD=110b @VDD5V>=2.5V		4.5		
			VLCD=101b @VDD5V>=2.2V		3.94		
			VLCD=100b @VDD5V>=2V		3.3		
			VLCD=011b		3.0		
			VLCD=010b		2.8		
	VDD Voltage drift	ENLCDP[0]=1b			5		%
Z_{LCD}	Output Impedance With LCD Buffer	F_{LCD} = LS_CK/32/9, VLCD = 3 V			10		KΩ
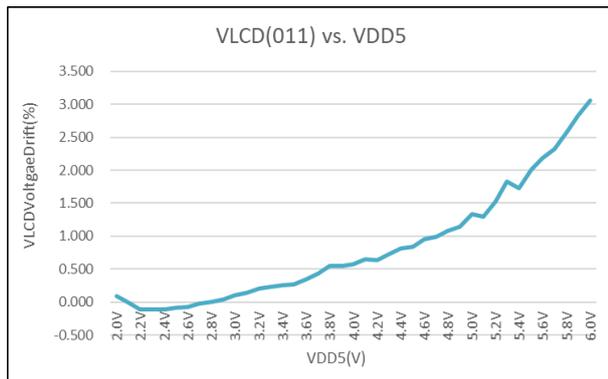
Figure5.9-1 VLCD vs. VDD5

5.10. Flash Memory

Typical values are at T_A=-40˚C~ 85˚C, VDD= VDD5V= 3.3V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	V_{DD5V} Supply voltage		2.0		5.5	V
	Program/Erase supply current				4	mA
	Data retention time		10			Years
	Number of program/Erase cycles(Endurance)		100			K Cycles
	Mass Erase time		10			ms
	Sector Erase time		2			ms
	Word Write time		20			us

6. Ordering Information

Order Name[1]	Package Type	Pin Number	PKG Type Description		Code No[2]	Shipment Type	Quantity Per Package	Material	MSL[3]
HY16F3910-N088	QFN	88	N	088	-	Tray	168	Green[4]	MSL-3
HY16F3910-L080	LQFP	80	L	080	-	Tray	160	Green[4]	MSL-3
HY16F3910-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3

HY16F3910-N088

IC Part Number   IC PKG Type

[1] Device No.: Model No. – Package Type Description – Code (Blank Code/ Standard/Customized Programming Code):

Ex: You request blank code in QFN88 package. The device No. will be HY16F3910-N088. and please clearly indicate the shipment packing type when placing orders.
Ex: Your customized programming code is 001 and you require products in QFN88 package. The device No. will be HY16F3910-N088-001. and please clearly indicate the shipment packing type when placing orders.

Ex: You request blank code in LQFP80 package. The device No. will be HY16F3910-L080. and please clearly indicate the shipment packing type when placing orders.
Ex: Your customized programming code is 005 and you require products in LQFP80 package. The device No. will be HY16F3910-L080-005. and please clearly indicate the shipment packing type when placing orders.

[2] Code:
"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] MSL:
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] Green (RoHS & no Cl/Br):
HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

## 7. Package Information

7.1. QFN88(N088) (TYPE 1)

7.1.1. Package Dimensions QFN88(10x10)
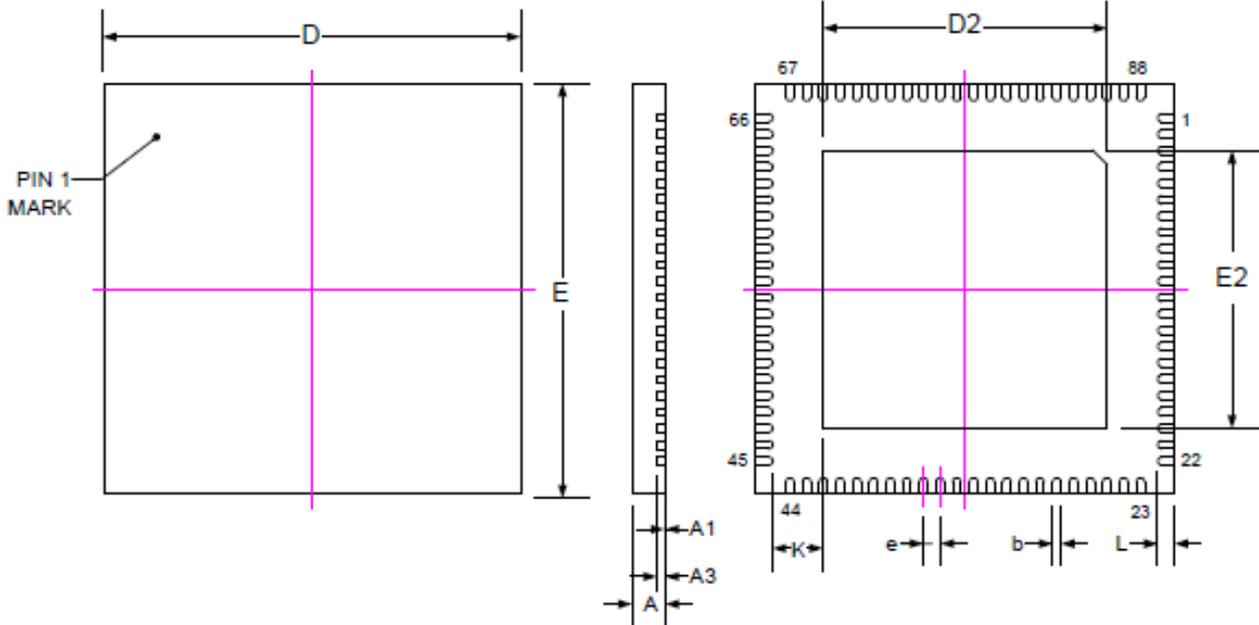
Unit: mm

SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	10.00 BSC		
E	10.00 BSC		
e	0.40 BSC		
D2	6.75	6.80	6.85
E2	6.75	6.80	6.85
L	0.30	0.40	0.50
K	1.08	1.20	1.33

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.

2. Do not include Mold Flash or Protrusions.

3. Unit: mm

4. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

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7.1.2. Land Pattern Design Recommendations
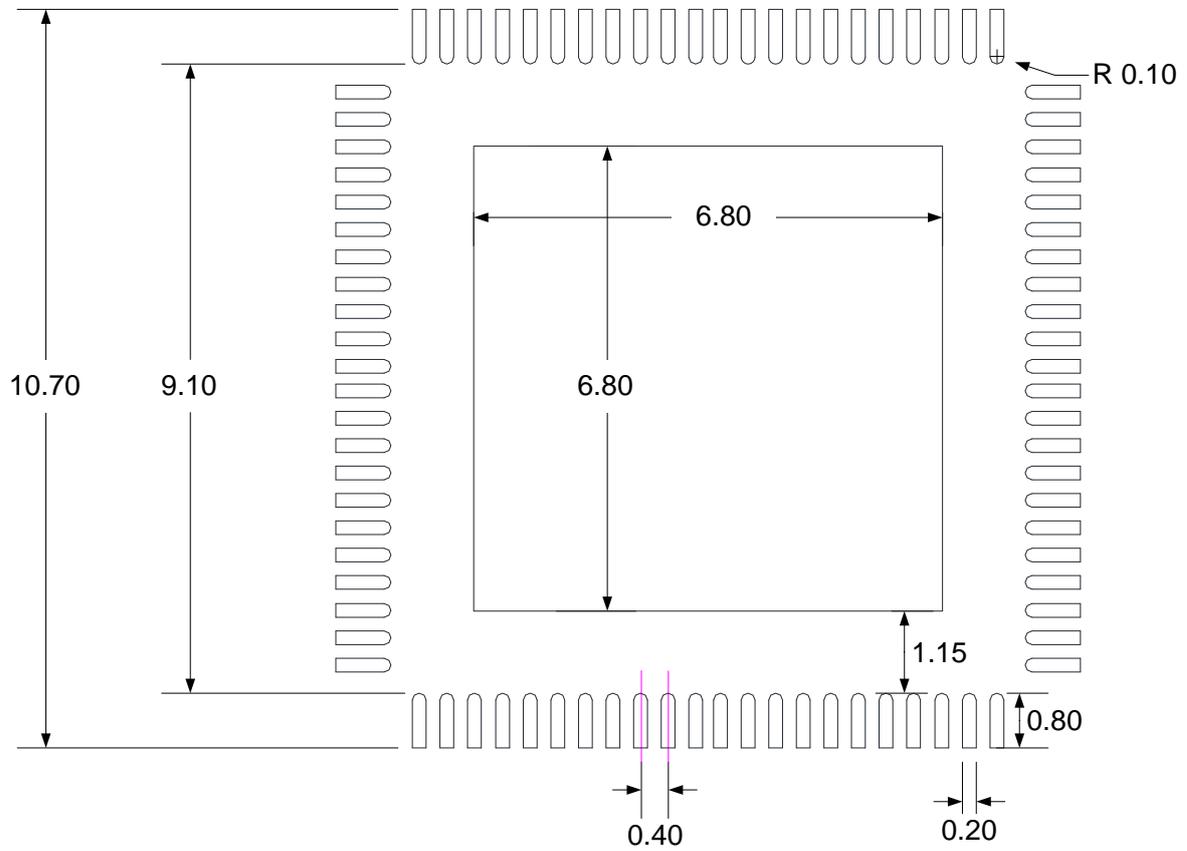
Note:

1. Publication IPC-7351 is recommended for alternate designs

2. Unit : mm

7.2. QFN88(N088) (TYPE 2)
7.2.1. Package Dimensions QFN88(10x10)
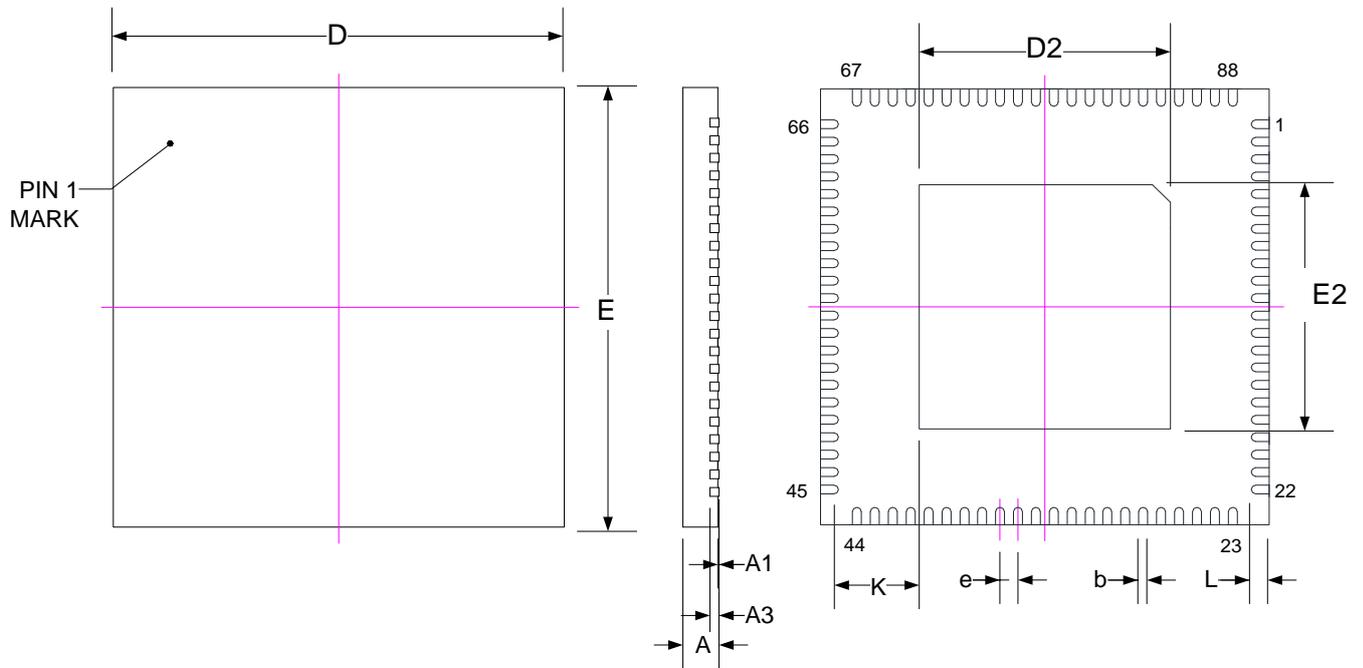
Unit: mm

SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	10.00 BSC		
E	10.00 BSC		
e	0.40 BSC		
D2	5.45	5.60	5.75
E2	5.45	5.60	5.75
L	0.30	0.40	0.50
K	1.62	1.80	1.98

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.

2. Do not include Mold Flash or Protrusions.

3. Unit: mm.

4. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

7.2.2. Land Pattern Design Recommendations
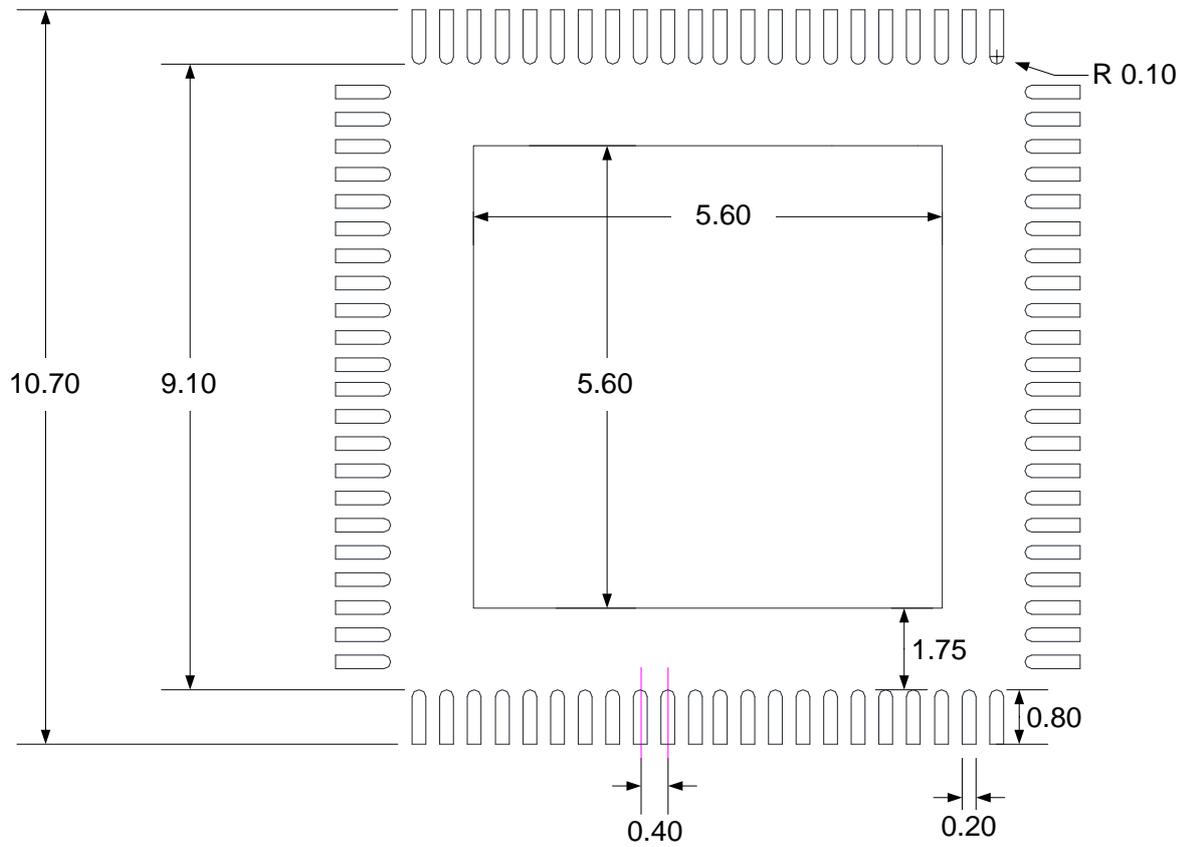
Note:

1. Publication IPC-7351 is recommended for alternate designs

2. Unit : mm

7.3. LQFP80(L080)

7.3.1. Package Dimensions LQFP80(10x10)

Unit: mm
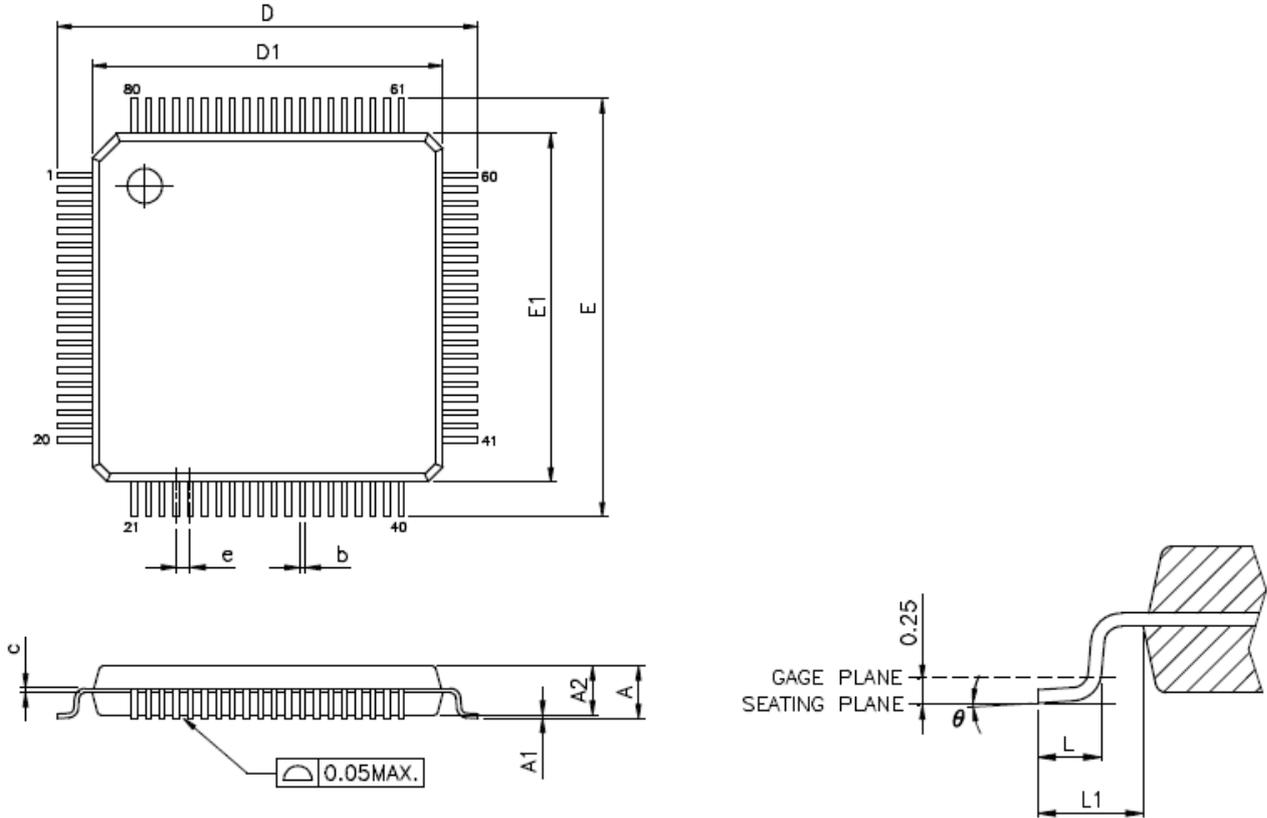
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.

2. Do not include Mold Flash or Protrusions.

3. Unit: mm.

7.4. LQFP64(L064)

7.4.1. Package Dimensions LQFP64(7x7)

Unit: mm
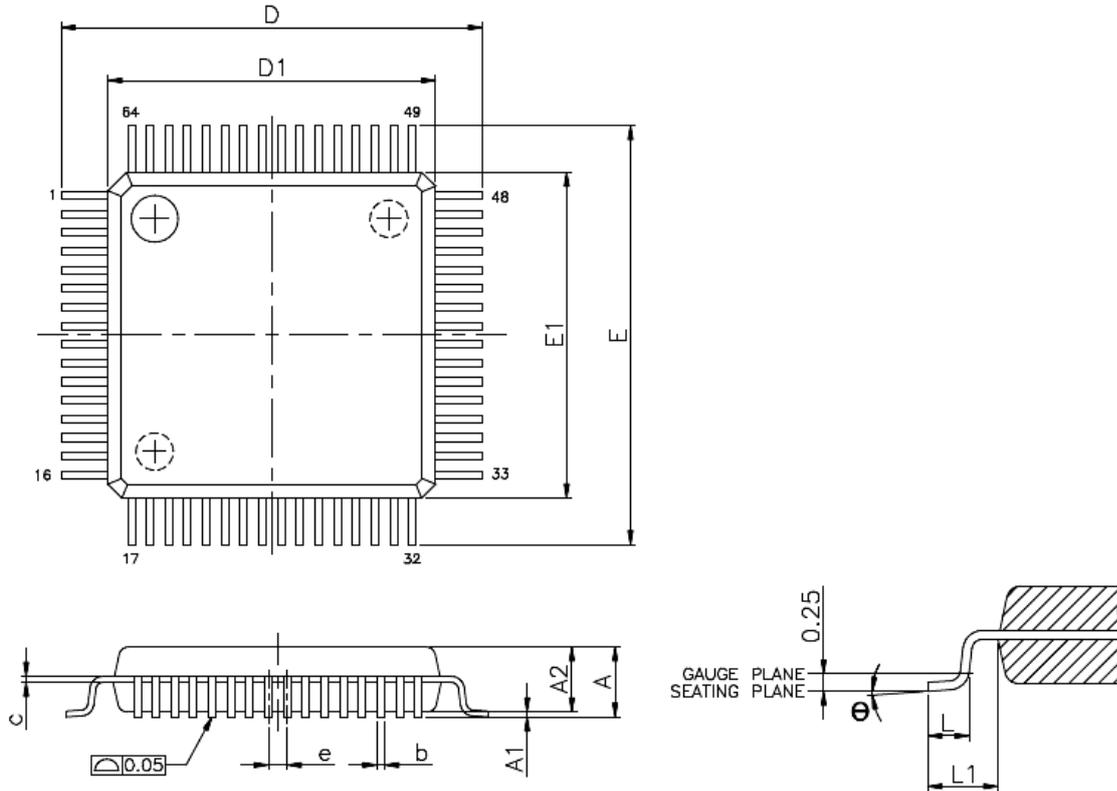
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
Θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.

2. Do not include Mold Flash or Protrusions.

3. Unit: mm.

8. Revision Record

Major differences are stated thereinafter.

Version	Page	Date	Revision Summary
V01	ALL	2022/02/17	First edition
V02	ALL	2022/09/15	1. The table on page 8: Package Revise to Pin. 2. Remove link http://www.hycontek.com/attachments/MSP/OJTI-HM-2013-002.pdf 3. Description of the additional ADC ENOB table. 4. The pin descriptions of SDRV1 and SDRV2 are revised to Reserved.
V04	ALL	2022/11/09	1. Modify the frequency sources configuration of HSXT for UART and UART2 in Chapter 4.4, and add a description. 2. Modify the frequency division configuration of WDTO in CH4.8 3. Removed GPIO in CH4.8 4. The capacitor connected to VDD15 is changed from 0.1uF to 1uF. 5. A 0.1uF filter capacitor is added to the VDD5V of the application circuit in CH3.1 and CH3.2, and the VDD15 is changed to a 1uF capacitor. In CH3.2, the pin3 and pin1/pin6 of the pressure sensor are disconnected.