HY16F3910
Datasheet

高精密混合信号处理控制器
4X44 ~ 8X40 LCD Driver
32-bit 低功耗微控制器
21-bit ENOB ΣΔADC
128KB Flash ROM

目录

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1. 特性

数字特性

- 32-bit 1T Andes Core E801 内核
- 支持 AndesSight C IDE 开发环境指令集
- 宽工作电压 2.0V to 5.5V
- 工作温度-40 to 85℃
- 低功耗:
  - 运行模式：0.8mA@HSRC=4.147MHz
  - 待机模式：5uA@LSRC=32KHz
  - 休眠模式：Typ.2.5uA
- 128KB Flash ROM
  - Write/Erase 的周期次数为：100,000 次
  - Write/Read/Erase 的操作电压 ≧2.0V
  - 内建硬件 ISP 功能，可在线更新 Flash
- 8KB SRAM
- 16-bit Timer A, Timer B(X2), Timer C, WDT
- 16-bit PWM 控制器及信号捕抓功能
- 硬件实现 I²C/32-bit SPI/UART(X2) 通讯接口
- 硬件实现时钟 RTC 万年历功能
- 高达 72 个可编程复用型 I/O
  - 24 个通用型数字输出输入端口
  - 48 个可选择 LCD 端口或数字输出输入端口
- 4x44 ~ 8x40 LCD 液晶驱动器
  - 1/3、1/4、1/5、1/6、1/8Duty
  - 1/3 及 1/4 Bias 选择
  - 支持 R Type 驱动方式
  - 内建 Charge Pump 稳压线路，可提供 6 段 VLCD 偏压，分别为 2.8V, 3.0V, 3.3V, 3.9V, 4.5V 及 5.0V

模拟特性

- 模拟工作电压为 2.4V to 3.6V
- 内建低噪声 24-bit Σ ADC
  - ADC 支持 x1~x4 信号放大
  - 内建低噪声放大器 x8,x16,x32 信号放大
  - 输入参考信号可解析至 65nVrms (Gain=128)
  - 最高转换率高达 15K sps
  - 低温飘系数与内置绝对温度传感
- 外部高速晶震频率高达 16MHz
- 外部低速晶震低至 32768Hz
- 内建 RC 高速震荡器频率
  - 频率可达 4.147MHz 及 31.795MHz
  - CPU 执行速度最高可达 16MHz
- 内建 RC 低速震荡器频率低至 32KHz
- 电源模块
  - 内建四段可调整稳压电源(VDDA)
  - 1.2V 带隙参考电压(REFO)
- 多功能比较器 Comparator
  - 支持外部电压输入比较
  - 支持 15 段 LVD 低电压检测电路

Part No.	24-b ΣΔADC	Flash (byte)	SRAM (byte)	Temp. Sensor	RTC	I/O	PWM	Serial Interface	LCD	ISP Mode	Package
HY16F3910-N088	9-CH	128K	8K	Y	1	24+48	4-CH	2*UART 32bits SPI I²C	4x44 6x42 8x40	Y	QFN88
HY16F3910-L080	9-CH	128K	8K	Y	1	24+44	4-CH	2*UART 32bits SPI I²C	4x40 6x38 8x36	Y	LQFP80
HY16F3910-L064	9-CH	128K	8K	Y	1	24+30	4-CH	2*UART 32bits SPI I²C	4x26 6x24 8x22	Y	LQFP64

2. 引脚名称定义

2.1. HY16F3910 引脚图

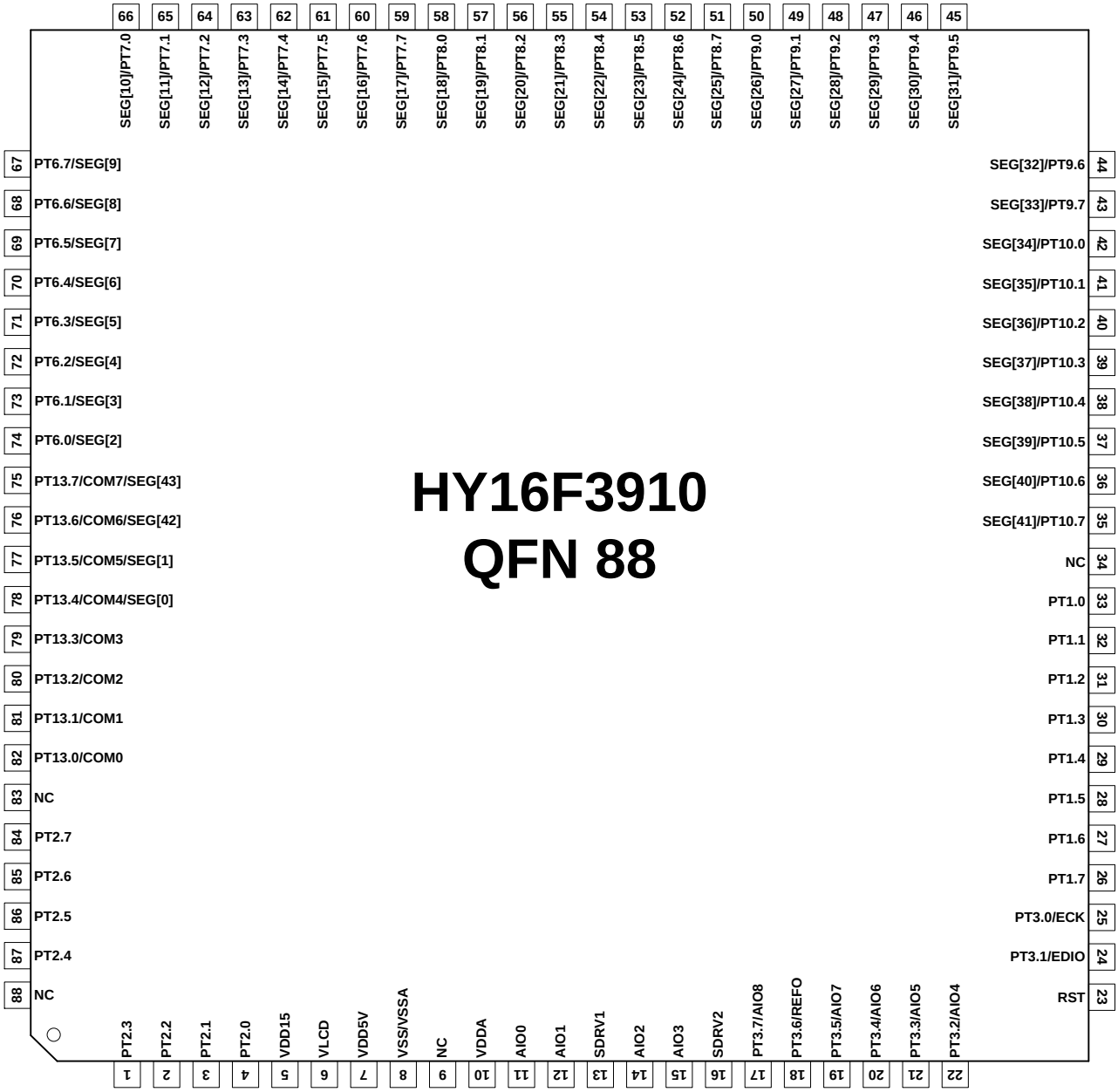


图 2-1-1 HY16F3910 QFN 88 引脚图

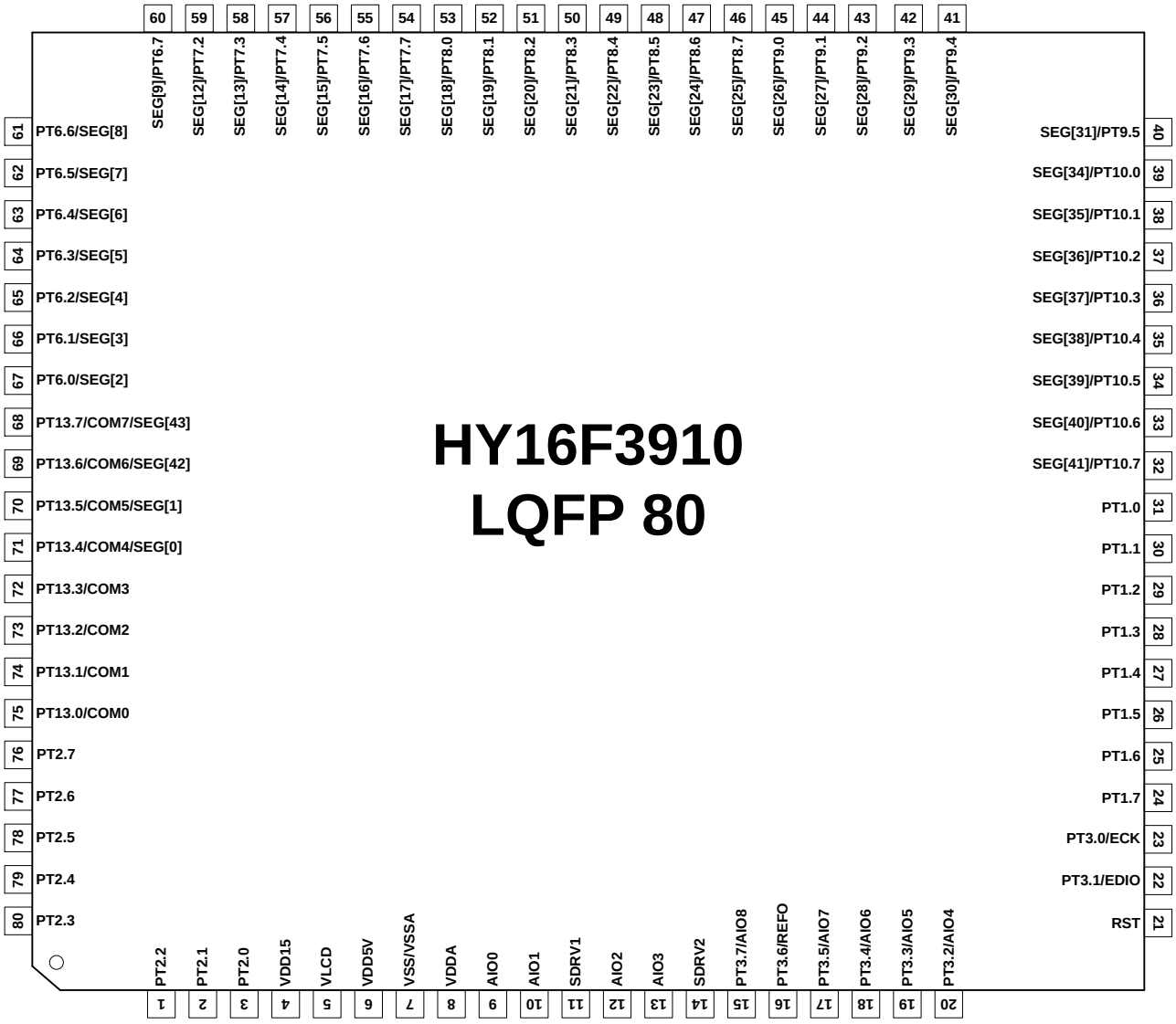


图 2-1-2 HY16F3910 LQFP 80 引脚图

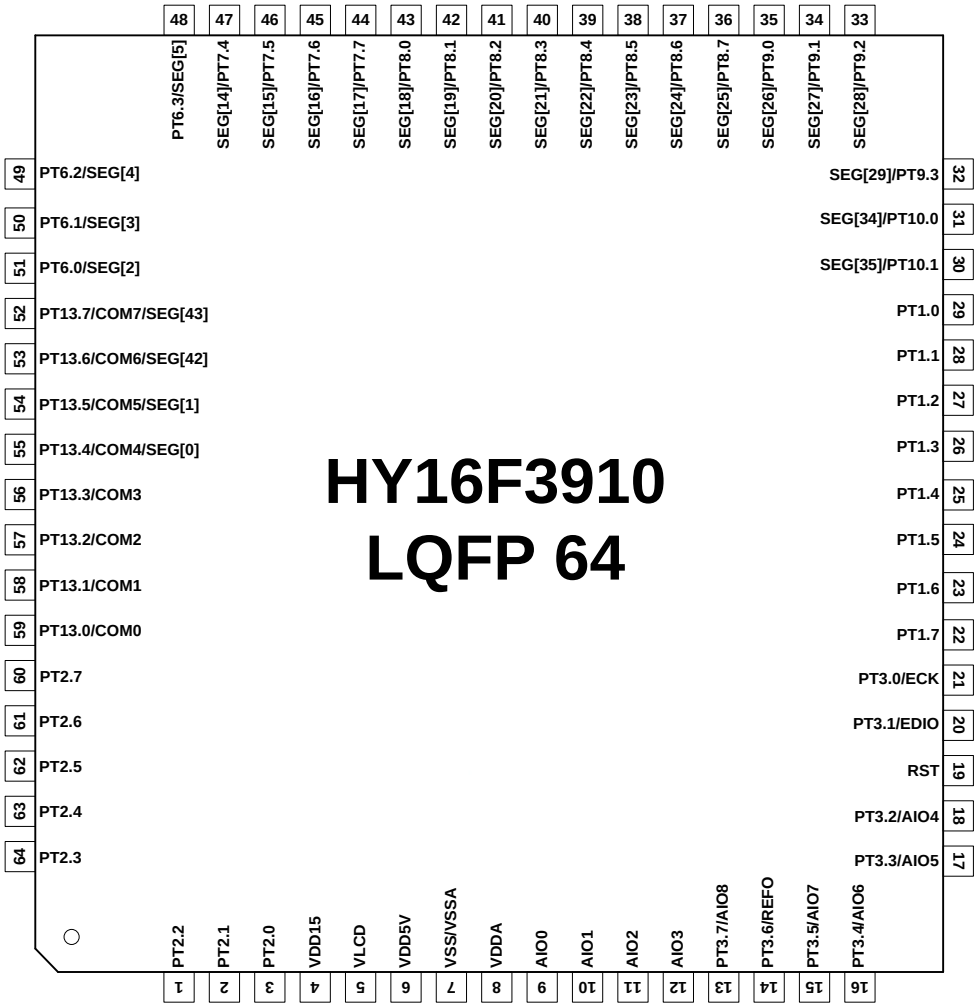


图 2-1-3 HY16F3910 LQFP 64 引脚图

2.2. 引脚定义与功能描述

2.2.1. 引脚定义

"I": Input ,"O": Output, "A": Analog, "S": Smith triggers, "C": CMOS I/O,"P": Power Source,"/": or ,"X": Ignorable.

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
1	80	64	PT2.3	I/O	S/C	通用数字输入/输出引脚
			INT2.3	I	S	外部中断源 INT2.3 输入引脚
			LVDOO	O	C	低电压比较器 LVDO 状态输出引脚
			PWM3_3	O	C	TimerB2, PWM3_3 输出引脚
			MOSI_3	O	C	SPI 通讯数据线引脚 MOSI_3(主机输出，从机输入)
			RX2_3	I	S	EUART2 通讯接收线引脚 RX2_3
			TCI2_6	I	S	捕捉比较器输入源引脚 TCI2_6
			SDA_6	I/O	S/C	I^2C 通讯数据线引脚 SDA_6
2	1	1	PT2.2	I/O	S/C	通用数字输入/输出引脚
			INT2.2	I	S	外部中断源 INT2.2 输入引脚
			PWM2_3	O	C	TimerB2, PWM2_3 输出引脚
			MISO_3	I	S	SPI 通讯数据线引脚 MISO_3(主机输入，从机输出)
			TX2_3	O	C	EUART2 通讯发送线引脚 TX2_3
			TCI1_6	I	S	捕捉比较器输入源引脚 TCI1_6
			SCL_6	I/O	S/C	I^2C 通讯时钟线引脚 SCL_6
3	2	2	PT2.1	I/O	S/C	通用数字输入/输出引脚
			INT2.1	I	S	外部中断源 INT2.1 输入引脚
			PWM1_3	O	C	TimerB, PWM1_3 输出引脚
			CK_3	O	C	SPI 通讯时钟线引脚 CK_3
			RX_3	I	S	EUART 通讯接收线引脚 RX_3
			TCI2_5	I	S	捕捉比较器输入源引脚 TCI2_5
			SDA_5	I/O	S/C	I^2C 通讯数据线引脚 SDA_5
4	3	3	PT2.0	I/O	S/C	通用数字输入/输出引脚
			INT2.0	I	S	外部中断源 INT2.0 输入引脚
			PWM0_3	O	C	TimerB, PWM0_3 输出引脚
			CS_3	I	S	SPI 通讯使能引脚 CS_3
			TX_3	O	C	EUART 通讯发送线引脚 TX_3
			TCI1_5	I	S	捕捉比较器输入源引脚 TCI1_5
			SCL_5	I/O	S/C	I^2C 通讯时钟线引脚 SCL_5
5	4	4	VDD15	I	P	芯片数字电路电源电压引脚，需外接 1uf 对地电容

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
6	5	5	VLCD	I/O	P	LCD 稳压电源输出/LCD 电源输入，需外接 10Uf 对地电容
7	6	6	VDD5V	I	P	芯片工作电源电压输入引脚 ，需外接对地的 0.1uF 滤波电容及稳压电容
8	7	7	VSS	I	PP	数字接地端引脚
			VSSA	I	P	模拟比接地端引脚
10	8	8	VDDA	I/O	P	仿真电压源输入/输出端，需外接 1~10Uf 对地电容
11	9	9	AIO0	I	A	ADC 模拟输入引脚 AIO0
12	10	10	AIO1	I	A	ADC 模拟输入引脚 AIO1
13	11	-	SDRV1	O	P	Reserved，内部使用，不需要连接，保持空接即可
14	12	11	AIO2	I	A	ADC 模拟输入引脚 AIO2
15	13	12	AIO3	I	A	ADC 模拟输入引脚 AIO3
16	14	-	SDRV2	O	P	Reserved，内部使用，不需要连接，保持空接即可
17	15	13	PT3.7	I/O	S/C	通用数字输入/输出引脚
			INT3.7	I	S	外部中断源 INT3.7 输入引脚
			LVDIN	I	A	低电压比较器外部输入引脚 LVDIN
			AIO8	I	A	ADC 模拟输入引脚 AIO8
18	16	14	PT3.6	I/O	S/C	通用数字输入/输出引脚
			INT3.6	I	S	外部中断源 INT3.6 输入引脚
			REFO	I/O	P	仿真参考电压 1.2V 输出引脚，需外接 0.1Uf 对地电容
19	17	15	PT3.5	I/O	S/C	通用数字输入/输出引脚
			INT3.5	I	S	外部中断源 INT3.5 输入引脚
			AIO7	I/O	A	ADC 模拟输入引脚 AIO7
20	18	16	PT3.4	I/O	S/C	通用数字输入/输出引脚
			INT3.4	I	S	外部中断源 INT3.4 输入引脚

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
			AIO6	I/O	A	ADC 模拟输入引脚 AIO6
21	19	17	PT3.3 INT3.3 AIO5	I/O I I/O	S/C S A	通用数字输入/输出引脚 外部中断源 INT3.3 输入引脚 ADC 模拟输入引脚 AIO5
22	20	18	PT3.2 INT3.2 AIO4	I/O I I/O	S/C S A	通用数字输入/输出引脚 外部中断源 INT3.2 输入引脚 ADC 模拟输入引脚 AIO4
23	21	19	RST	I	D	复位引脚(低电位有效) 需外接 10Nf 对地电容
24	22	20	PT3.1 INT3.1 EDIO	I/O I I/O	S/C S D	通用数字输入/输出引脚 外部中断源 INT3.1 输入引脚 开发调试通讯口(EDM)数据线输入/输出引脚，RST=L 时可动作
25	23	21	PT3.0 INT3.0 ECK	I/O I I/O	S/C S D	通用数字输入/输出引脚 外部中断源 INT3.0 输入引脚 开发调试通讯口(EDM)时钟线引脚， RST=L 时可动作
26	24	22	PT1.7 INT1.7 PWM3_2 MOSI_2 RX2_2 TCI2_4	I/O I O O I I	S/C S C C S S	通用数字输入/输出引脚 外部中断源 INT1.7 输入引脚 TimerB2, PWM3_2 输出引脚 SPI 通讯数据线引脚 MOSI_2(主机输出，从机输入) EUART2 通讯接收线引脚 RX2_2 捕捉比较器输入源引脚 TCI2_4

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
			SDA_4	I/O	S/C	I²C 通讯数据线引脚 SDA_4
27	25	23	PT1.6	I/O	S/C	通用数字输入/输出引脚
			INT1.6	I	S	外部中断源 INT1.6 输入引脚
			PWM2_2	O	C	TimerB2, PWM2_2 输出引脚
			MISO_2	I	S	SPI 通讯数据线引脚 MISO_2(主机输入，从机输出)
			TX2_2	O	C	EUART2 通讯发送线引脚 TX2_2
			TCI1_4	I	S	捕捉比较器输入源引脚 TCI1_4
			SCL_4	I/O	S/C	I²C 通讯时钟线引脚 SCL_4
28	26	24	PT1.5	I/O	S/C	通用数字输入/输出引脚
			INT1.5	I	S	外部中断源 INT1.5 输入引脚
			PWM1_2	O	C	TimerB, PWM1_2 输出引脚
			CK_2	O	C	SPI 通讯时钟线引脚 CK_2
			RX_2	I	S	EUART 通讯接收线引脚 RX_2
			TCI2_3	I	S	捕捉比较器输入源引脚 TCI2_3
			SDA_3	I/O	S/C	I²C 通讯数据线引脚 SDA_3
29	27	25	PT1.4	I/O	S/C	通用数字输入/输出引脚
			INT1.4	I	S	外部中断源 INT1.4 输入引脚
			PWM0_2	O	C	TimerB, PWM0_2 输出引脚
			CS_2	I	S	SPI 通讯使能引脚 CS_2
			TX_2	O	C	EUART 通讯发送线引脚 TX_2
			TCI1_3	I	S	捕捉比较器输入源引脚 TCI1_3
			SCL_3	I/O	S/C	I²C 通讯时钟线引脚 SCL_3
30	28	26	PT1.3	I/O	S/C	通用数字输入/输出引脚
			INT1.3	I	S	外部中断源 INT1.3 输入引脚
			PWM3_1	O	C	TimerB2, PWM3_1 输出引脚
			MOSI_1	O	C	SPI 通讯数据线引脚 MOSI_1(主机输出，从机输入)
			RX2_1	I	S	EUART2 通讯接收线引脚 RX2_1
			TCI2_2	I	S	捕捉比较器输入源引脚 TCI2_2
			SDA_2	I/O	S/C	I²C 通讯数据线引脚 SDA_2
31	29	27	PT1.2	I/O	S/C	通用数字输入/输出引脚
			INT1.2	I	S	外部中断源 INT1.2 输入引脚
			PWM2_1	O	C	TimerB2, PWM2_1 输出引脚
			MISO_1	I	S	SPI 通讯数据线引脚 MISO_1(主机输入，从机输出)
			TX2_1	O	C	EUART2 通讯发送线引脚 TX2_1
			TCI1_2	I	S	捕捉比较器输入源引脚 TCI1_2

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
			SCL_2	I/O	S/C	I²C 通讯时钟线引脚 SCL_2
32	30	28	PT1.1	I/O	S/C	通用数字输入/输出引脚
			INT1.1	I	S	外部中断源 INT1.1 输入引脚
			PWM1_1	O	C	TimerB, PWM1_1 输出引脚
			CK_1	O	C	SPI 通讯时钟线引脚 CK_1
			RX_1	I	S	EUART 通讯接收线引脚 RX_1
			TCI2_1	I	S	捕捉比较器输入源引脚 TCI2_1
			SDA_1	I/O	S/C	I²C 通讯数据线引脚 SDA_1
33	31	29	PT1.0	I/O	S/C	通用数字输入/输出引脚
			INT1.0	I	S	外部中断源 INT1.0 输入引脚
			PWM0_1	O	C	TimerB, PWM0_1 输出引脚
			CS_1	I	S	SPI 通讯使能引脚 CS_1
			TX_1	O	C	EUART 通讯发送线引脚 TX_1
			TCI1_1	I	S	捕捉比较器输入源引脚 TCI1_1
			SCL_1	I/O	S/C	I²C 通讯时钟线引脚 SCL_1
34	-	-	NC	-	-	不需要连接，保持空接即可
35	32	-	PT10.7	I/O	S/C	通用数字输入/输出引脚
			SEG41	O	A	LCD Segment 41 输出
36	33	-	PT10.6	I/O	S/C	通用数字输入/输出引脚
			SEG40	O	A	LCD Segment 40 输出
			TCI3_8	I	S	TimerB2 输入源引脚 TCI3_8
37	34	-	PT10.5	I/O	S/C	通用数字输入/输出引脚
			SEG39	O	A	LCD Segment 39 输出
38	35	-	PT10.4	I/O	S/C	通用数字输入/输出引脚
			SEG38	O	A	LCD Segment 38 输出
			TCI3_7	I	S	TimerB2 输入源引脚 TCI3_7
39	36	-	PT10.3	I/O	S/C	通用数字输入/输出引脚
			SEG37	O	A	LCD Segment 37 输出
40	37	-	PT10.2	I/O	S/C	通用数字输入/输出引脚
			SEG36	O	A	LCD Segment 36 输出
41	38	30	PT10.1	I/O	S/C	通用数字输入/输出引脚
			SEG35	O	A	LCD Segment 35 输出
42	39	31	PT10.0	I/O	S/C	通用数字输入/输出引脚
			SEG34	O	A	LCD Segment 34 输出

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
			PT9.7	I/O	S/C	通用数字输入/输出引脚
43	-	-	SEG33	O	A	LCD Segment 33 输出
			PT9.6	I/O	S/C	通用数字输入/输出引脚
44	-	-	SEG32	O	A	LCD Segment 32 输出
			PT9.5	I/O	S/C	通用数字输入/输出引脚
45	40	-	SEG31	O	A	LCD Segment 31 输出
			PT9.4	I/O	S/C	通用数字输入/输出引脚
46	41	-	SEG30	O	A	LCD Segment 30 输出
			PT9.3	I/O	S/C	通用数字输入/输出引脚
			SEG29	O	A	LCD Segment 29 输出
			PWM3_7	O	C	TimerB2, PWM3_7 输出引脚
47	42	32	MOSI_7	O	C	SPI 通讯数据线引脚 MOSI_7(主机输出，从机输入)
			RX2_7	I	S	EUART2 通讯接收线引脚 RX2_7
			PT9.2	I/O	S/C	通用数字输入/输出引脚
			SEG28	I	S	LCD Segment 28 输出
			PWM2_7	O	C	TimerB2, PWM2_7 输出引脚
48	43	33	MISO_7	I	S	SPI 通讯数据线引脚 MISO_7(主机输入，从机输出)
			TX2_7	O	C	EUART2 通讯发送线引脚 TX2_7
			TCI3_6	I	S	TimerB2 输入源引脚 TCI3_6
			PT9.1	I/O	S/C	通用数字输入/输出引脚
			SEG27	I	S	LCD Segment 27 输出
			PWM1_7	O	C	TimerB, PWM1_7 输出引脚
49	44	34	CK_7	O	C	SPI 通讯时钟线引脚 CK_7
			RX_7	I	S	EUART 通讯接收线引脚 RX_7
			PT9.0	I/O	S/C	通用数字输入/输出引脚
			SEG26	I	S	LCD Segment 26 输出
			PWM0_7	O	C	TimerB, PWM0_1 输出引脚
50	45	35	CS_7	I	S	SPI 通讯使能引脚 CS_1
			TX_7	O	C	EUART 通讯发送线引脚 TX_1
			TCI3_5	I	S	TimerB2 输入源引脚 TCI3_5
			PT8.7	I/O	S/C	通用数字输入/输出引脚
51	46	36	SEG25	O	A	LCD Segment 25 输出
			PT8.6	I/O	S/C	通用数字输入/输出引脚
52	47	37	SEG24	O	A	LCD Segment 24 输出

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
			PT8.5	I/O	S/C	通用数字输入/输出引脚
53	48	38	SEG23	O	A	LCD Segment 23 输出
			PT8.4	I/O	S/C	通用数字输入/输出引脚
54	49	39	SEG22	O	A	LCD Segment 22 输出
			PT8.3	I/O	S/C	通用数字输入/输出引脚
			SEG21	O	A	LCD Segment 21 输出
			PWM3_8	O	C	TimerB2, PWM3_8 输出引脚
55	50	40	MOSI_8	O	C	SPI 通讯数据线引脚 MOSI_8(主机输出，从机输入)
			RX2_8	I	S	EUART2 通讯接收线引脚 RX2_8
			PT8.2	I/O	S/C	通用数字输入/输出引脚
			SEG20	I	S	LCD Segment 20 输出
			PWM2_8	O	C	TimerB2, PWM2_8 输出引脚
56	51	41	MISO_8	I	S	SPI 通讯数据线引脚 MISO_8(主机输入，从机输出)
			TX2_8	O	C	EUART2 通讯发送线引脚 TX2_8
			PT8.1	I/O	S/C	通用数字输入/输出引脚
			SEG19	I	S	LCD Segment 19 输出
			PWM1_8	O	C	TimerB, PWM1_8 输出引脚
57	52	42	CK_8	O	C	SPI 通讯时钟线引脚 CK_8
			RX_8	I	S	EUART 通讯接收线引脚 RX_8
			PT8.0	I/O	S/C	通用数字输入/输出引脚
			SEG18	I	S	LCD Segment 18 输出
			PWM0_8	O	C	TimerB, PWM0_8 输出引脚
58	53	43	CS_8	I	S	SPI 通讯使能引脚 CS_8
			TX_8	O	C	EUART 通讯发送线引脚 TX_8
			PT7.7	I/O	S/C	通用数字输入/输出引脚
			SEG17	O	A	LCD Segment 17 输出
			PWM3_6	O	C	TimerB2, PWM3_6 输出引脚
59	54	44	MOSI_6	O	C	SPI 通讯数据线引脚 MOSI_6(主机输出，从机输入)
			RX2_6	I	S	EUART2 通讯接收线引脚 RX2_6
			PT7.6	I/O	S/C	通用数字输入/输出引脚
			SEG16	I	S	LCD Segment 16 输出
			PWM2_6	O	C	TimerB2, PWM2_6 输出引脚
60	55	45	MISO_6	I	S	SPI 通讯数据线引脚 MISO_6(主机输入，从机输出)
			TX2_6	O	C	EUART2 通讯发送线引脚 TX2_6
			TCI3_4	I	S	TimerB2 输入源引脚 TCI3_4

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
61	56	46	PT7.5	I/O	S/C	通用数字输入/输出引脚
			SEG15	O	A	LCD Segment 15 输出
			PWM1_6	O	C	TimerB, PWM1_6 输出引脚
			CK_6	O	C	SPI 通讯时钟线引脚 CK_6
			RC_6	I	S	EUART 通讯接收线引脚 RX_6
62	57	47	PT7.4	I/O	S/C	通用数字输入/输出引脚
			SEG14	O	A	LCD Segment 14 输出
			PWM0_6	O	C	TimerB, PWM0_6 输出引脚
			CS_6	O	C	SPI 通讯时钟线引脚 CS_6
			TX_6	I	S	EUART 通讯发送线引脚 TX_6
			TCI3_3	I	S	TimerB2 输入源引脚 TCI3_3
63	58	-	PT7.3	I/O	S/C	通用数字输入/输出引脚
			SEG13	O	A	LCD Segment 13 输出
64	59	-	PT7.2	I/O	S/C	通用数字输入/输出引脚
			SEG12	O	A	LCD Segment 12 输出
65	-	-	PT7.1	I/O	S/C	通用数字输入/输出引脚
			SEG11	O	A	LCD Segment 11 输出
66	-	-	PT7.0	I/O	S/C	通用数字输入/输出引脚
			SEG10	O	A	LCD Segment 10 输出
67	60	-	PT6.7	I/O	S/C	通用数字输入/输出引脚
			SEG9	O	A	LCD Segment 9 输出
68	61	-	PT6.6	I/O	S/C	通用数字输入/输出引脚
			SEG8	O	A	LCD Segment 8 输出
69	62	-	PT6.5	I/O	S/C	通用数字输入/输出引脚
			SEG7	O	A	LCD Segment 7 输出
70	63	-	PT6.4	I/O	S/C	通用数字输入/输出引脚
			SEG6	O	A	LCD Segment 6 输出
71	64	48	PT6.3	I/O	S/C	通用数字输入/输出引脚
			SEG5	O	A	LCD Segment 5 输出
			PWM3_5	O	C	TimerB2, PWM3_5 输出引脚
			MOSI_5	O	C	SPI 通讯数据线引脚 MOSI_5(主机输出，从机输入)
			RX2_5	I	S	EUART2 通讯接收线引脚 RX2_5
72	65	49	PT6.2	I/O	S/C	通用数字输入/输出引脚
			SEG4	O	A	LCD Segment 4 输出
			PWM2_5	O	C	TimerB2, PWM2_5 输出引脚

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
			MISO_5	I	S	SPI 通讯数据线引脚 MISO_5(主机输入，从机输出)
			TX2_5	O	C	EUART2 通讯发送线引脚 TX2_5
			TCI3_2	I	S	TimerB2 输入源引脚 TCI3_2
73	66	50	PT6.1	I/O	S/C	通用数字输入/输出引脚
			SEG3	O	A	LCD Segment 3 输出
			PWM1_5	O	C	TimerB, PWM1_5 输出引脚
			CK_5	O	C	SPI 通讯时钟线引脚 CK_5
			RX_5	I	S	EUART 通讯接收线引脚 RX_5
74	67	51	PT6.0	I/O	S/C	通用数字输入/输出引脚
			SEG2	O	A	LCD Segment 2 输出
			PWM0_5	O	C	TimerB, PWM0_5 输出引脚
			CS_5	I	S	SPI 通讯使能引脚 CS_5
			TX_5	O	C	EUART 通讯发送线引脚 TX_5
			TCI3_1	I	S	TimerB2 输入源引脚 TCI3_1
75	68	52	PT13.7	I/O	S/C	通用数字输入/输出引脚
			SEG43	O	A	LCD Segment 43 输出
			COM7	O	A	LCD Common 7 输出
76	69	53	PT13.6	I/O	S/C	通用数字输入/输出引脚
			SEG42	O	A	LCD Segment 42 输出
			COM6	O	A	LCD Common 6 输出
77	70	54	PT13.5	I/O	S/C	通用数字输入/输出引脚
			SEG1	O	A	LCD Segment 1 输出
			COM5	O	A	LCD Common 5 输出
78	71	55	PT13.4	I/O	S/C	通用数字输入/输出引脚
			SEG0	O	A	LCD Segment 0 输出
			COM4	O	A	LCD Common 4 输出
79	72	56	PT13.3	I/O	S/C	通用数字输入/输出引脚
			COM3	O	A	LCD Common 3 输出
80	73	57	PT13.2	I/O	S/C	通用数字输入/输出引脚
			COM2	O	A	LCD Common 2 输出
81	74	58	PT13.1	I/O	S/C	通用数字输入/输出引脚
			COM1	O	A	LCD Common 1 输出
82	75	59	PT13.0	I/O	S/C	通用数字输入/输出引脚
			COM0	O	A	LCD Common 0 输出

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
84	76	60	PT2.7	I/O	S/C	通用数字输入/输出引脚
			HS_XOUT	A	A	外部高速晶震 2~16MHz 输出引脚
			INT2.7	I	S	外部中断源 INT2.7 输入引脚
			PWM3_4	O	C	TimerB2, PWM3_4 输出引脚
			MOSI_4	O	C	SPI 通讯数据线引脚 MOSI_4(主机输出，从机输入)
			RX2_4	I	S	EUART2 通讯接收线引脚 RX2_4
			TCI2_8	I	S	捕捉比较器输入源引脚 TCI2_8
			SDA_8	I/O	S/C	I2C 通讯数据线引脚 SDA_8
85	77	61	PT2.6	I/O	S/C	通用数字输入/输出引脚
			HS_XIN	A	A	外部高速晶震 2~16MHz 输入引脚
			INT2.6	I	S	外部中断源 INT2.6 输入引脚
			PWM2_4	O	C	TimerB2, PWM2_4 输出引脚
			MISO_4	I	S	SPI 通讯数据线引脚 MISO_4(主机输入，从机输出)
			TX2_4	O	C	EUART2 通讯发送线引脚 TX2_4
			TCI1_8	I	S	捕捉比较器输入源引脚 TCI1_8
			SCL_8	I/O	S/C	I2C 通讯时钟线引脚 SCL_8
86	78	62	PT2.5	I/O	S/C	通用数字输入/输出引脚
			LS_XIN	A	A	外部低速晶震 32768Hz 输出引脚
			INT2.5	I	S	外部中断源 INT2.5 输入引脚
			PWM1_4	O	C	TimerB, PWM1_4 输出引脚
			CK_4	O	C	SPI 通讯时钟线引脚 CK_4
			RX_4	I	S	EUART 通讯接收线引脚 RX_4
			TCI2_7	I	S	捕捉比较器输入源引脚 TCI2_7
			SDA_7	I/O	S/C	I2C 通讯数据线引脚 SDA_7
87	79	63	PT2.4	I/O	S/C	通用数字输入/输出引脚
			LS_XOUT	A	A	外部低速晶震 32768Hz 输入引脚
			INT2.4	I	S	外部中断源 INT2.4 输入引脚
			PWM0_4	O	C	TimerB2, PWM0_4 输出引脚
			CS_4	O	C	SPI 通讯使能引脚 CS_4
			TX_4	O	C	EUART 通讯发送线引脚 TX_4
			TCI1_8	I	S	捕捉比较器输入源引脚 TCI1_7
			SCL_7	I/O	S/C	I2C 通讯时钟线引脚 SCL_7
9	-	-	NC	-	-	不需要连接，保持空接即可

封装 / 引脚编号			引脚名称	特性		功能说明
QFN88	LQFP80	LQFP64		型态	缓冲	
34						
83						
88						

表 2-1 引脚定义及引脚功能描述

2.3. 引脚复用功能及复用功能优先级

Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT1.0	INT1.0	DIO	TCI1_1		CS_1	SCL_1	Tx_1		PWM0_1
PT1.1	INT1.1	DIO	TCI2_1		CK_1	SDA_1	Rx_1		PWM1_1
PT1.2	INT1.2	DIO	TCI1_2		MISO_1	SCL_2	Tx2_1		PWM2_1
PT1.3	INT1.3	DIO	TCI2_2		MOSI_1	SDA_2	Rx2_1		PWM3_1
PT1.4	INT1.4	DIO	TCI1_3		CS_2	SCL_3	Tx_2		PWM0_2
PT1.5	INT1.5	DIO	TCI2_3		CK_2	SDA_3	Rx_2		PWM1_2
PT1.6	INT1.6	DIO	TCI1_4		MISO_2	SCL_4	Tx2_2		PWM2_2
PT1.7	INT1.7	DIO	TCI2_4		MOSI_2	SDA_4	Rx2_2		PWM3_2
PT2.0	INT2.0	DIO	TCI1_5		CS_3	SCL_5	Tx_3		PWM0_3
PT2.1	INT2.1	DIO	TCI2_5		CK_3	SDA_5	Rx_3		PWM1_3
PT2.2	INT2.2	DIO	TCI1_6		MISO_3	SCL_6	Tx2_3		PWM2_3
PT2.3	INT2.3	DIO	TCI2_6	LVDOO	MOSI_3	SDA_6	Rx2_3		PWM3_3
PT2.4	INT2.4	DIO	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4		PWM0_4
PT2.5	INT2.5	DIO	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4		PWM1_4
PT2.6	INT2.6	DIO	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4		PWM2_4
PT2.7	INT2.7	DIO	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4		PWM3_4
PT3.0	INT3.0	DIO		**ECK**					
PT3.1	INT3.1	DIO		**EDIO**					
PT3.2	INT3.2	DIOAI						AIO4	
PT3.3	INT3.3	DIOAI						AIO5	
PT3.4	INT3.4	DIOAI						AIO6	
PT3.5	INT3.5	DIOAI						AIO7	
PT3.6	INT3.6	DIOAIO						REFO	
PT3.7	INT3.7	DIOAI						AIO8/LVDIN	
AIO0		AI						AIO0	
AIO1		AI						AIO1	
AIO2		AI						AIO2	
AIO3		AI						AIO3	
PT13.0		DIOAO		COM 0					

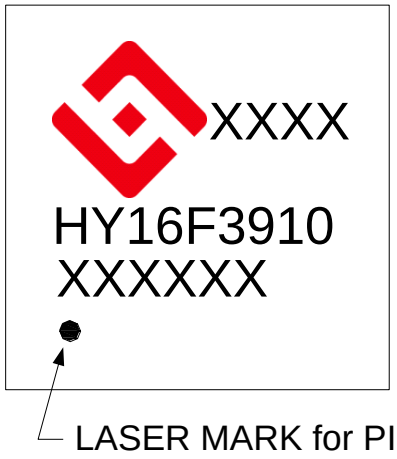
Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT13.1		DIOAO		COM 1					
PT13.2		DIOAO		COM 2					
PT13.3		DIOAO		COM 3					
PT13.4		DIOAO		COM 4/SEG 0					
PT13.5		DIOAO		COM 5/SEG 1					
PT13.6		DIOAO		COM 6/SEG 42					
PT13.7		DIOAO		COM 7/SEG 43					
PT6.0		DIOAO	TCI3_1	SEG 2	CS_5		Tx_5		PWM0_5
PT6.1		DIOAO		SEG 3	CK_5		Rx_5		PWM1_5
PT6.2		DIOAO	TCI3_2	SEG 4	MISO_5		Tx2_5		PWM2_5
PT6.3		DIOAO		SEG 5	MOSI_5		Rx2_5		PWM3_5
PT6.4		DIOAO		SEG 6					
PT6.5		DIOAO		SEG 7					
PT6.6		DIOAO		SEG 8					
PT6.7		DIOAO		SEG 9					
PT7.0		DIOAO		SEG 10					
PT7.1		DIOAO		SEG 11					
PT7.2		DIOAO		SEG 12					
PT7.3		DIOAO		SEG 13					
PT7.4		DIOAO	TCI3_3	SEG 14	CS_6		Tx_6		PWM0_6
PT7.5		DIOAO		SEG 15	CK_6		Rx_6		PWM1_6
PT7.6		DIOAO	TCI3_4	SEG 16	MISO_6		Tx2_6		PWM2_6
PT7.7		DIOAO		SEG 17	MOSI_6		Rx2_6		PWM3_6
PT8.0		DIOAO		SEG 18	CS_8		Tx_8		PWM0_8
PT8.1		DIOAO		SEG 19	CK_8		Rx_8		PWM1_8
PT8.2		DIOAO		SEG 20	MISO_8		Tx2_8		PWM2_8
PT8.3		DIOAO		SEG 21	MOSI_8		Rx2_8		PWM3_8
PT8.4		DIOAO		SEG 22					

Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT8.5		DIOAO		SEG 23					
PT8.6		DIOAO		SEG 24					
PT8.7		DIOAO		SEG 25					
PT9.0		DIOAO	TCI3_5	SEG 26	CS_7		Tx_7		PWM0_7
PT9.1		DIOAO		SEG 27	CK_7		Rx_7		PWM1_7
PT9.2		DIOAO	TCI3_6	SEG 28	MISO_7		Tx2_7		PWM2_7
PT9.3		DIOAO		SEG 29	MOSI_7		Rx2_7		PWM3_7
PT9.4		DIOAO		SEG 30					
PT9.5		DIOAO		SEG 31					
PT9.6		DIOAO		SEG 32					
PT9.7		DIOAO		SEG 33					
PT10.0		DIOAO		SEG 34					
PT10.1		DIOAO		SEG 35					
PT10.2		DIOAO		SEG 36					
PT10.3		DIOAO		SEG 37					
PT10.4		DIOAO	TCI3_7	SEG 38					
PT10.5		DIOAO		SEG 39					
PT10.6		DIOAO	TCI3_8	SEG 40					
PT10.7		DIOAO		SEG 41					

表 2-2 引脚复用功能及优先级描述

2.4. 封装片丝印信息

2.4.1. QFN 封装片丝印信息

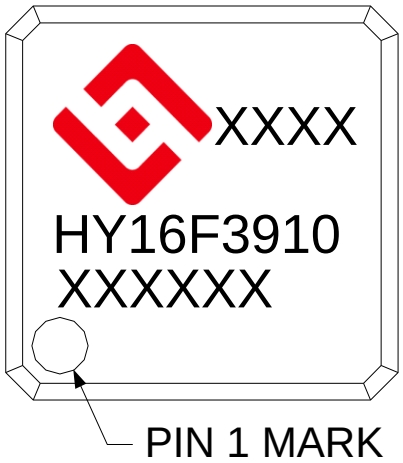


宏康Logo + 生产识别码

产品名称:HY16F3910

产品批号

2.4.2. LQFP 封装片丝印信息



宏康Logo + 生产识别码

产品名称:HY16F3910

产品批号

3. 应用电路

3.1. 桥式传感器应用电路

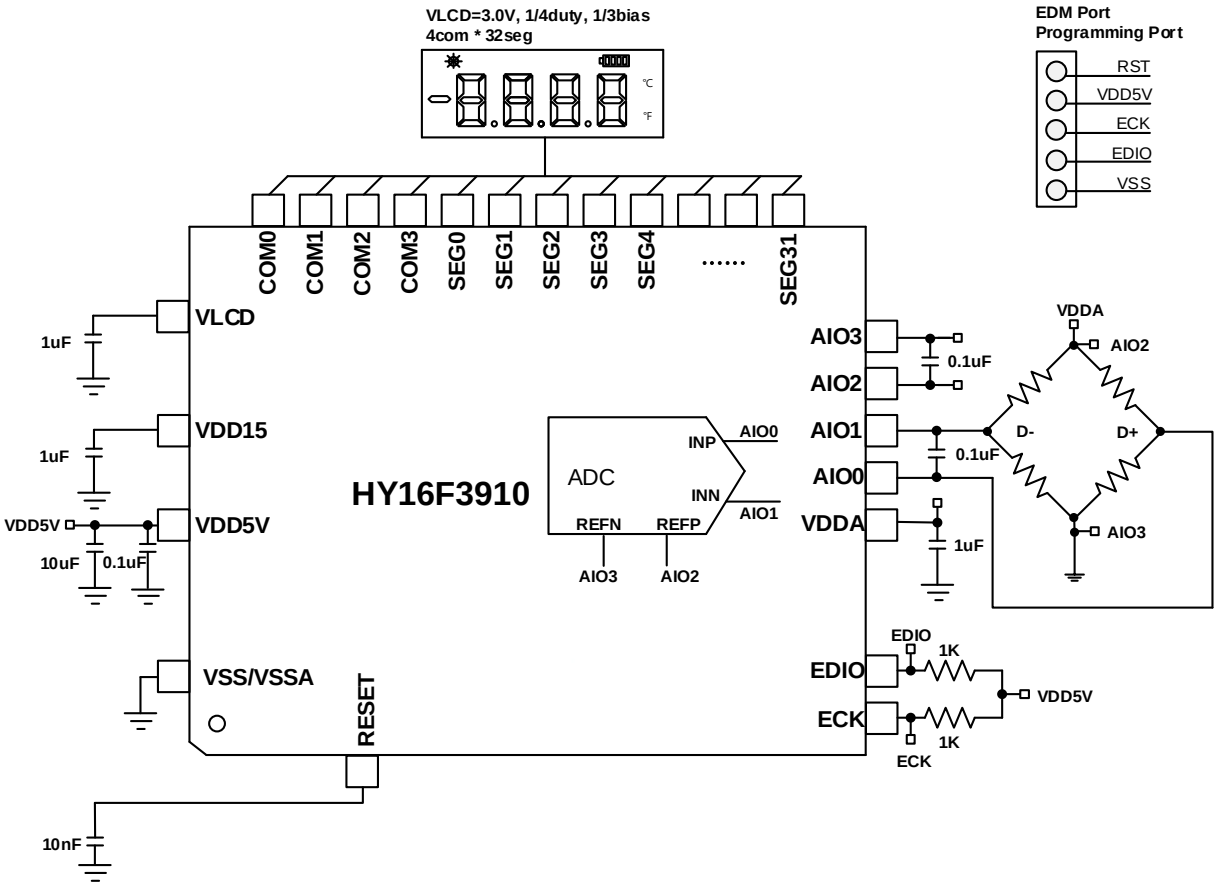


图 3-1 桥式传感器应用电路

3.2. 血压传感器应用电路

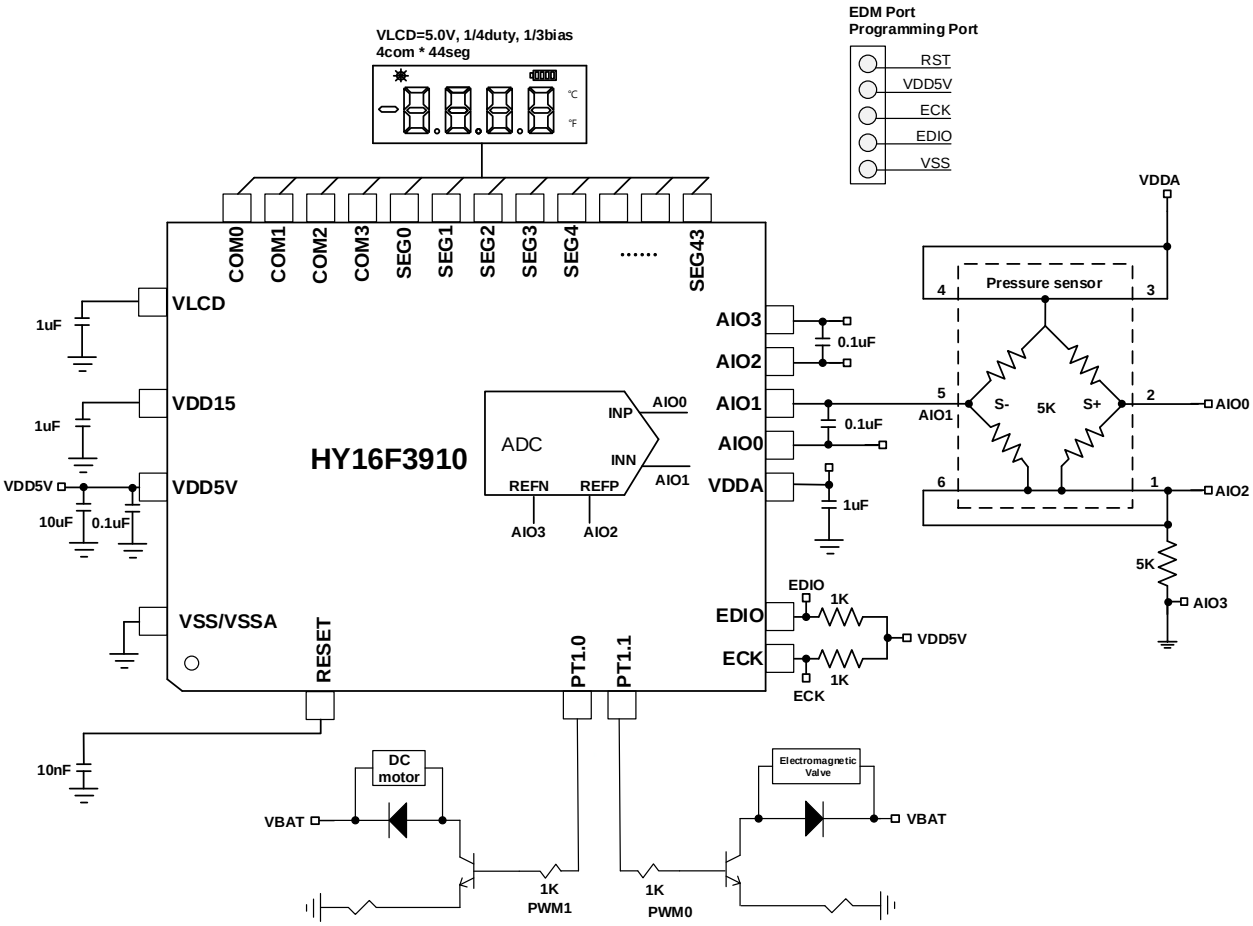


图 3-2 血压传感器应用电路

4. 功能概述

4.1. 内部框图

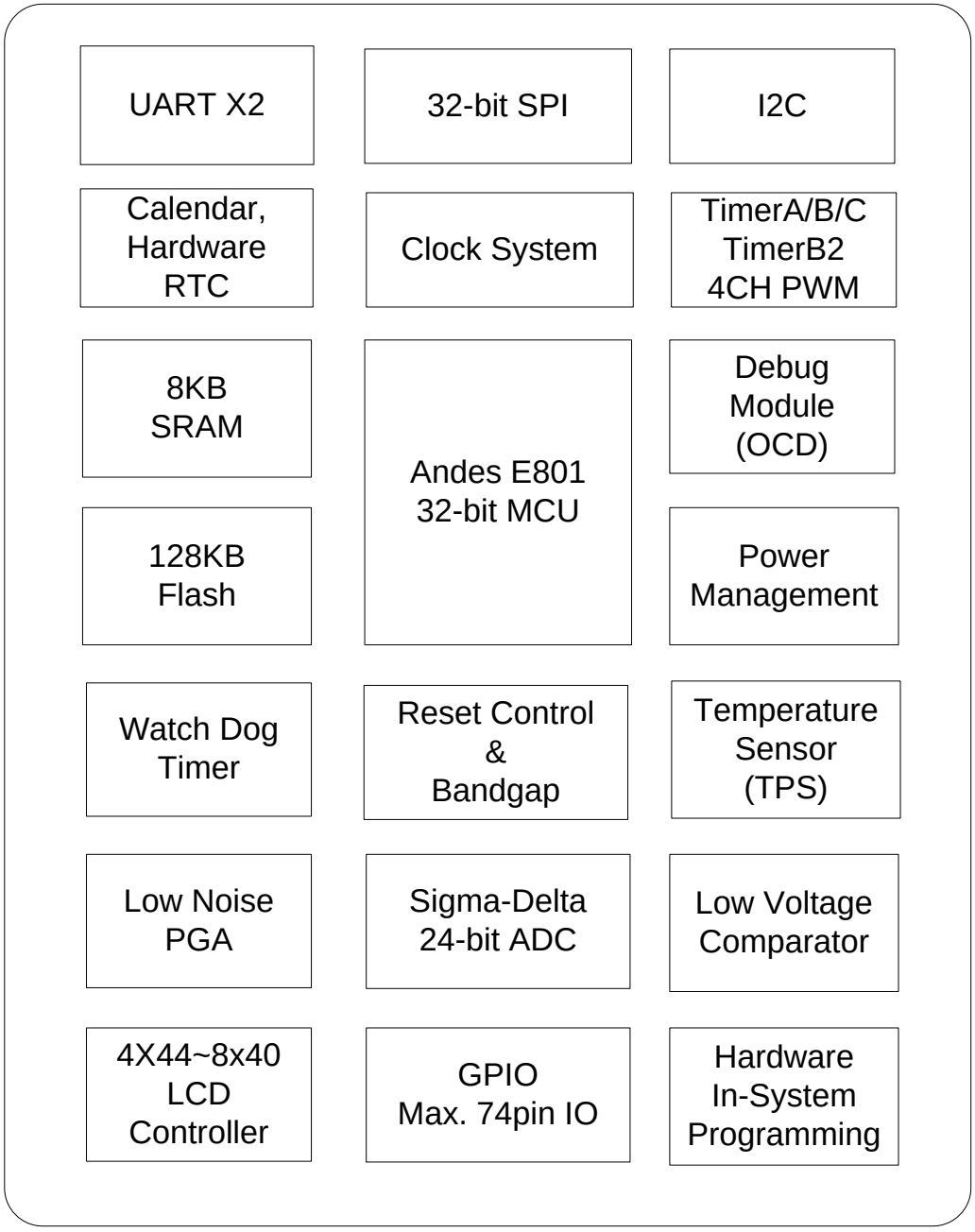


图4-1 HY16F3910 内部框图

4.2. 中央处理器核心方框图

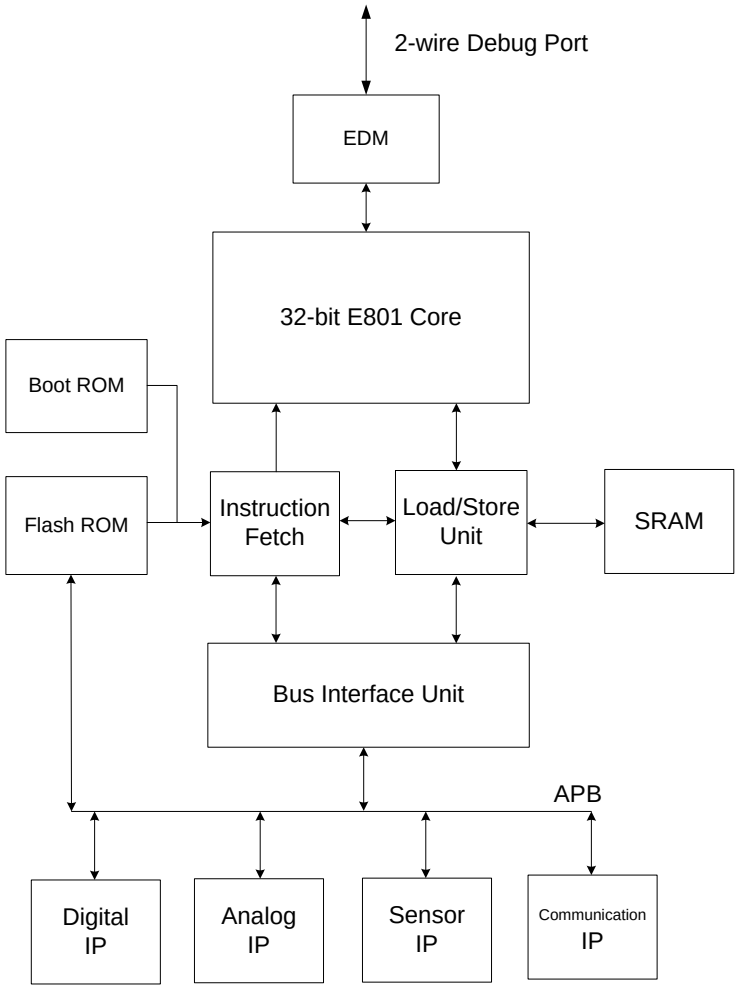
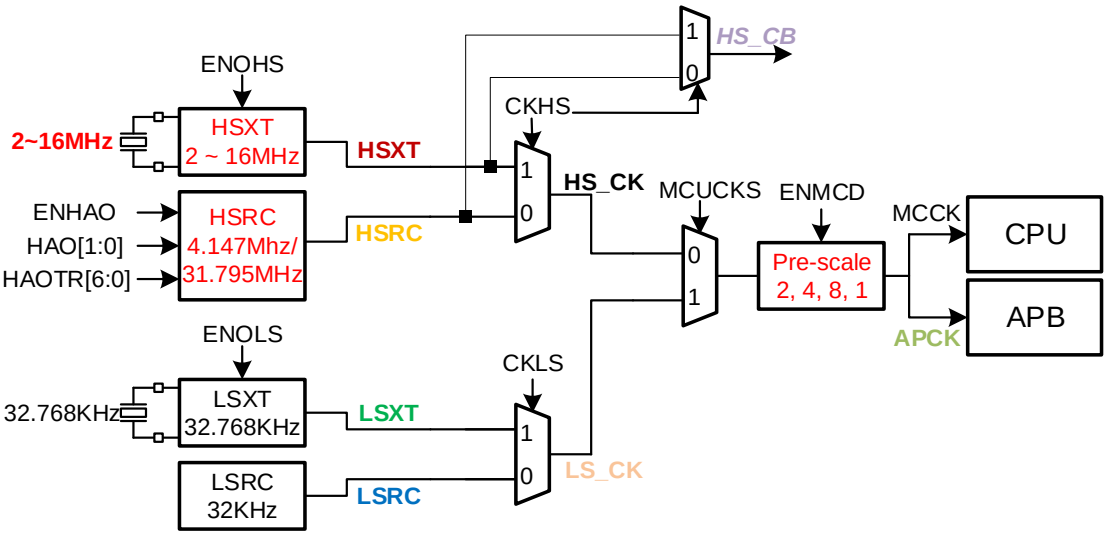


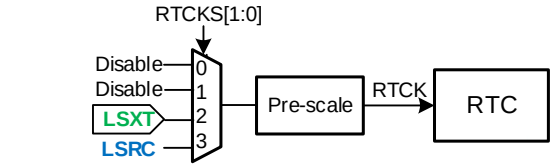
图4-2 中央处理器核心方框图

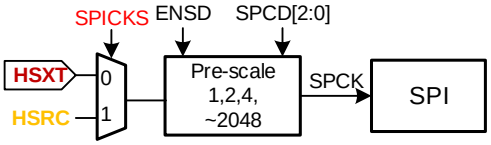
4.3. 相关的支持文档

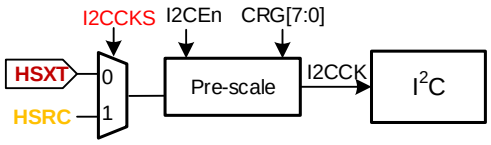
文件名	描述
UG-HY16F3910	HY16F3910 系列用户手册
APD-HY16IDE0xx	HY16F3910 C 函数库手册
APD-HY16IDE0xx	HY16F3910 各 IP 使用说明书
APD-HY16IDE001	HY16F 系列 IDE 软件使用说明书/ HY16F Series Device 安装程序
APD-HY16IDE0xx	HY16F3910 ICE 硬件使用说明书
APD-HY16IDE006	HY16F 系列烧录器使用说明书

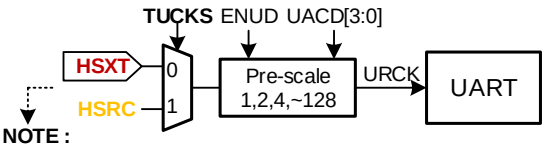
4.4. 时钟系统网络



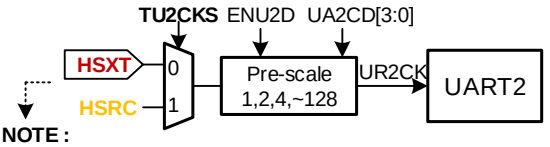




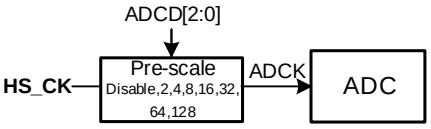


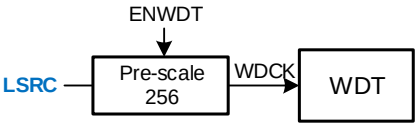


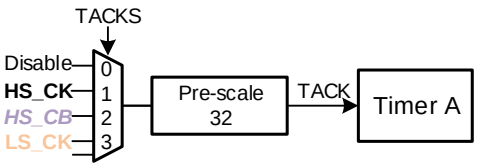
NOTE :
Workable condition : CPU clock have to equal to UART clock
OK example1 : MCUCKS=HS_CK, CKHS=HSXT, TUCKS=HSXT
OK example2 : MCUCKS=HS_CK, CKHS=HSRC, TUCKS=HSRC
NG example1 : MCUCKS=HS_CK, CKHS=HSRC, TUCKS=HSXT
NG example2 : MCUCKS=HS_CK, CKHS=HSXT, TUCKS=HSRC

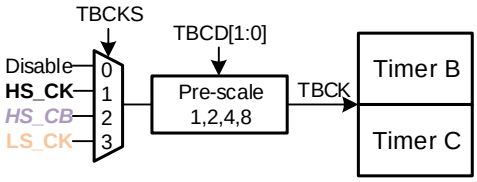


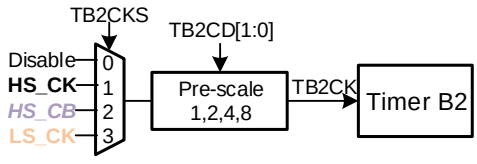
NOTE :
Workable condition : CPU clock have to equal to UART2 clock
OK example1 : MCUCKS=HS_CK, CKHS=HSXT, TU2CKS=HSXT
OK example2 : MCUCKS=HS_CK, CKHS=HSRC, TU2CKS=HSRC
NG example1 : MCUCKS=HS_CK, CKHS=HSRC, TU2CKS=HSXT
NG example2 : MCUCKS=HS_CK, CKHS=HSXT, TU2CKS=HSRC

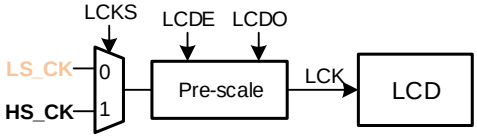




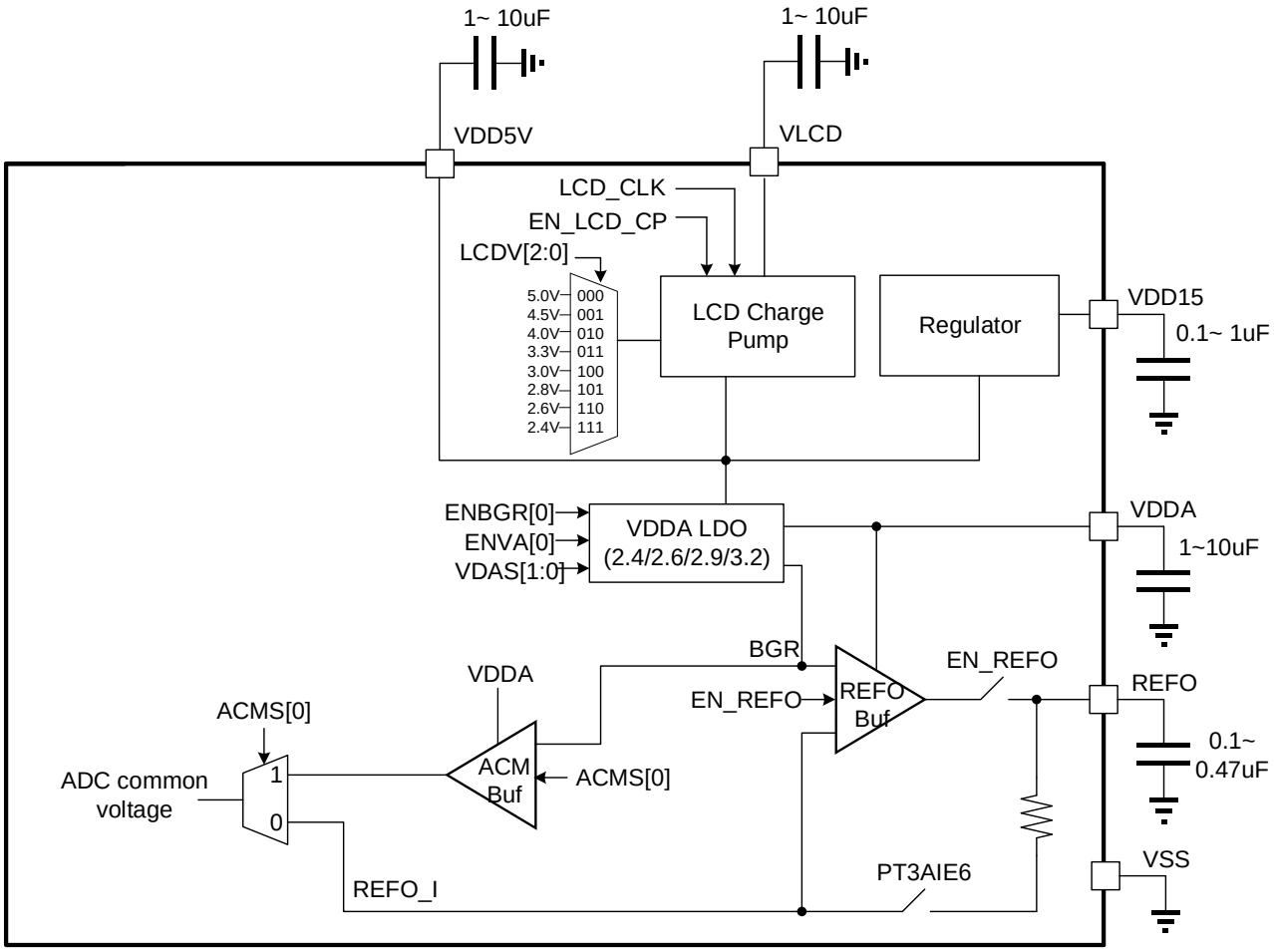




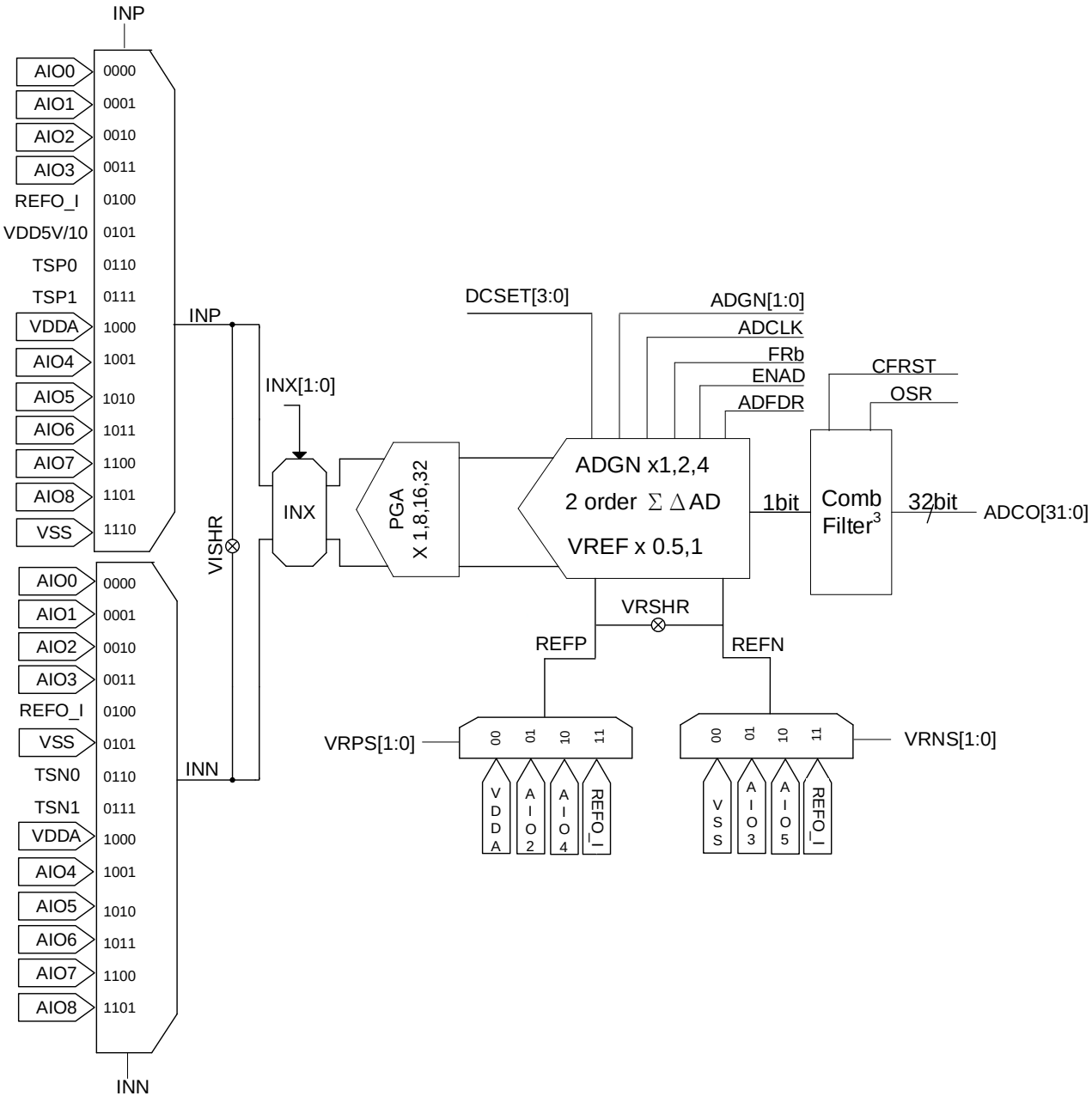




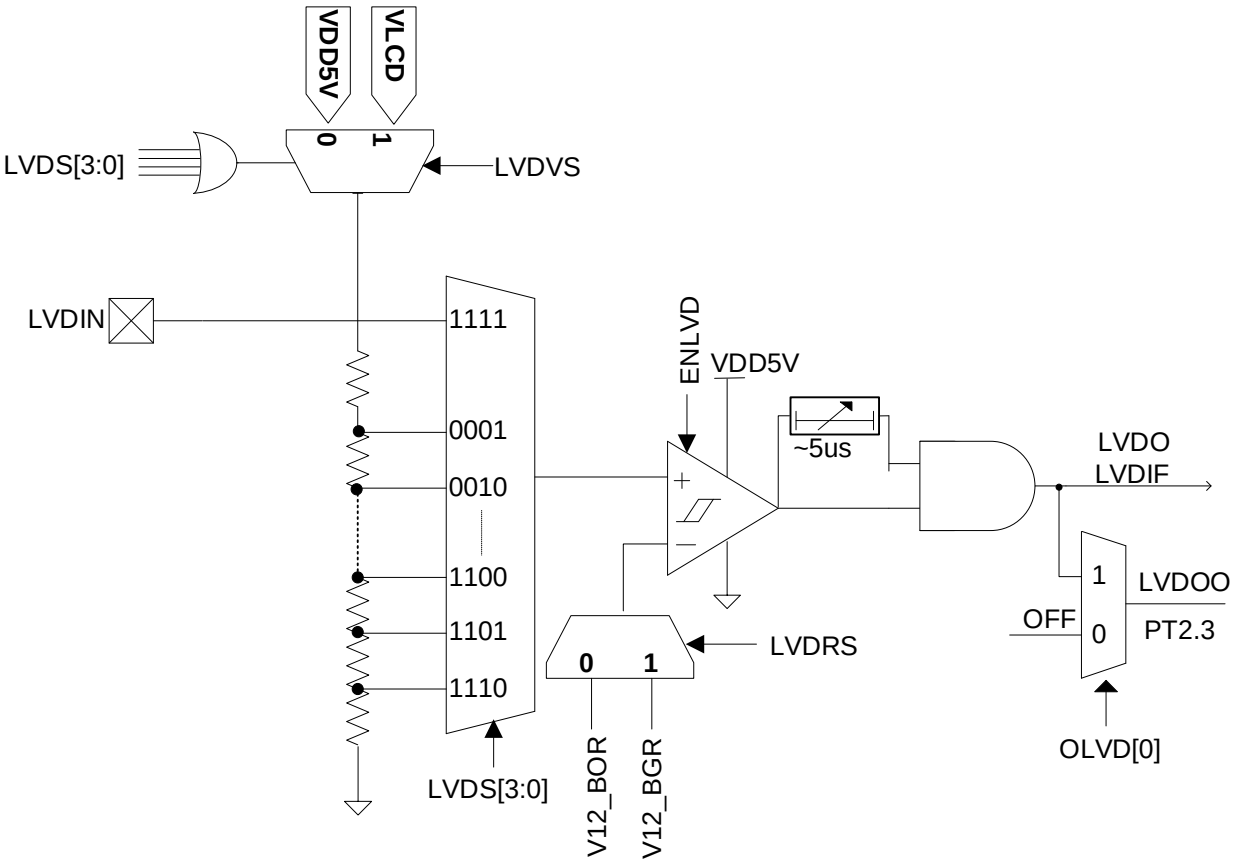
4.5. 电源系统网络


1~ 10uF
1~ 10uF
VDD5V
VLCD
LCD_CLK
EN_LCD_CP
LCDV[2:0]
5.0V 000
4.5V 001
4.0V 010
3.3V 011
3.0V 100
2.8V 101
2.6V 110
2.4V 111
LCD Charge Pump
Regulator
VDD15
0.1~ 1uF
ENBGR[0]
ENVA[0]
VDAS[1:0]
VDDA LDO
(2.4/2.6/2.9/3.2)
VDDA
1~10uF
BGR
EN_REFO
REFO Buf
EN_REFO
REFO
0.1~
0.47uF
VDDA
ACMS[0]
ADC common voltage
1
0
ACM Buf
ACMS[0]
VSS
PT3AIE6
REFO_I

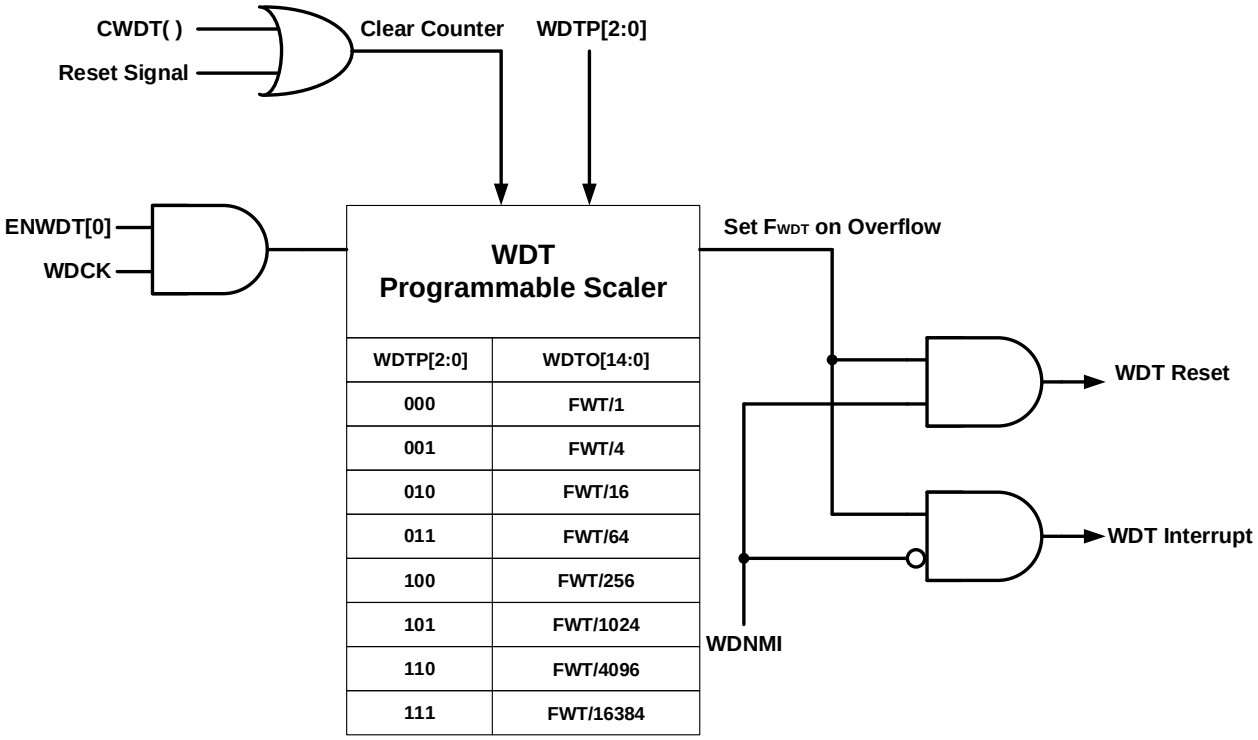
4.6. 24-bit ΣΔADC 网络



4.7. 低电压比较器网络

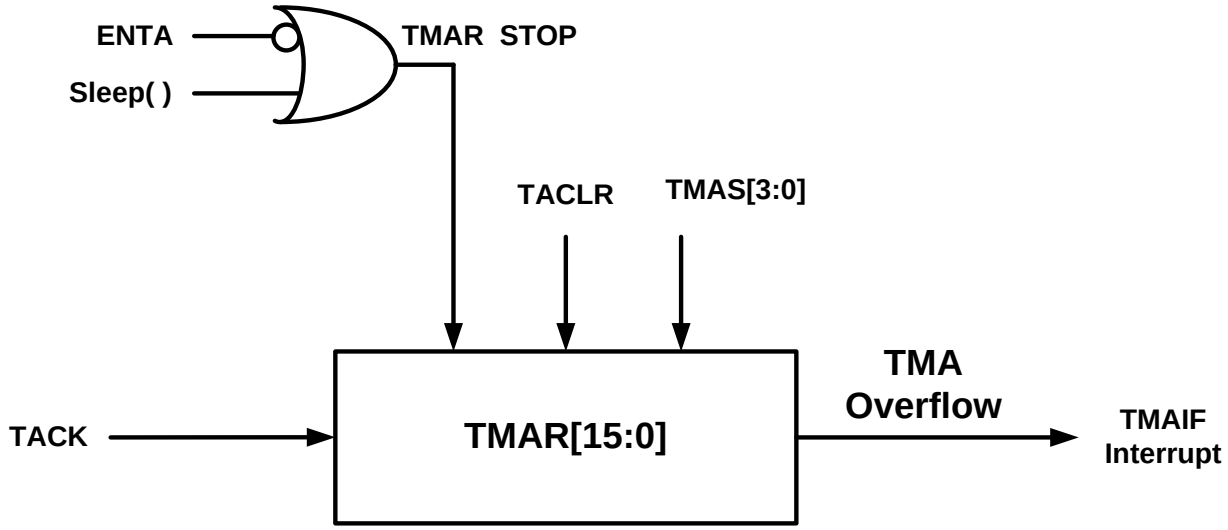

VDD5V
VLCD
0
1
LVDS[3:0]
LVDVS
LVDIN
1111
0001
0010
1100
1101
1110
LVDS[3:0]
ENLVD
VDD5V
~5us
LVDO
LVDIF
1
0
LVDOO
PT2.3
OFF
OLVD[0]
LVDRS
0
1
V12_BOR
V12_BGR

4.8. 看门狗(WDT)网络



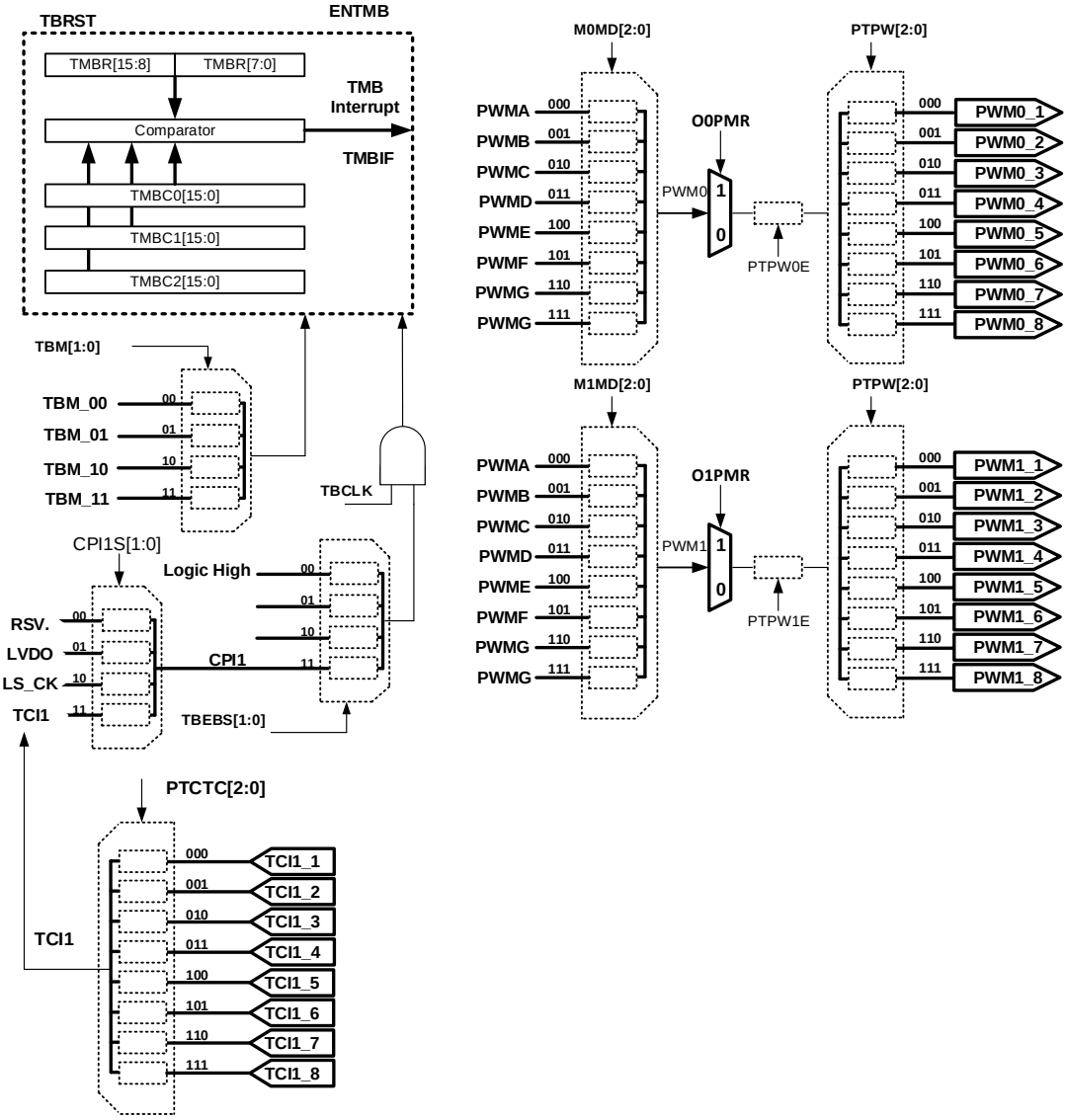
WDTP[2:0]	WDTO[14:0]
000	FWT/1
001	FWT/4
010	FWT/16
011	FWT/64
100	FWT/256
101	FWT/1024
110	FWT/4096
111	FWT/16384

4.9. 定时计数器 A 网络

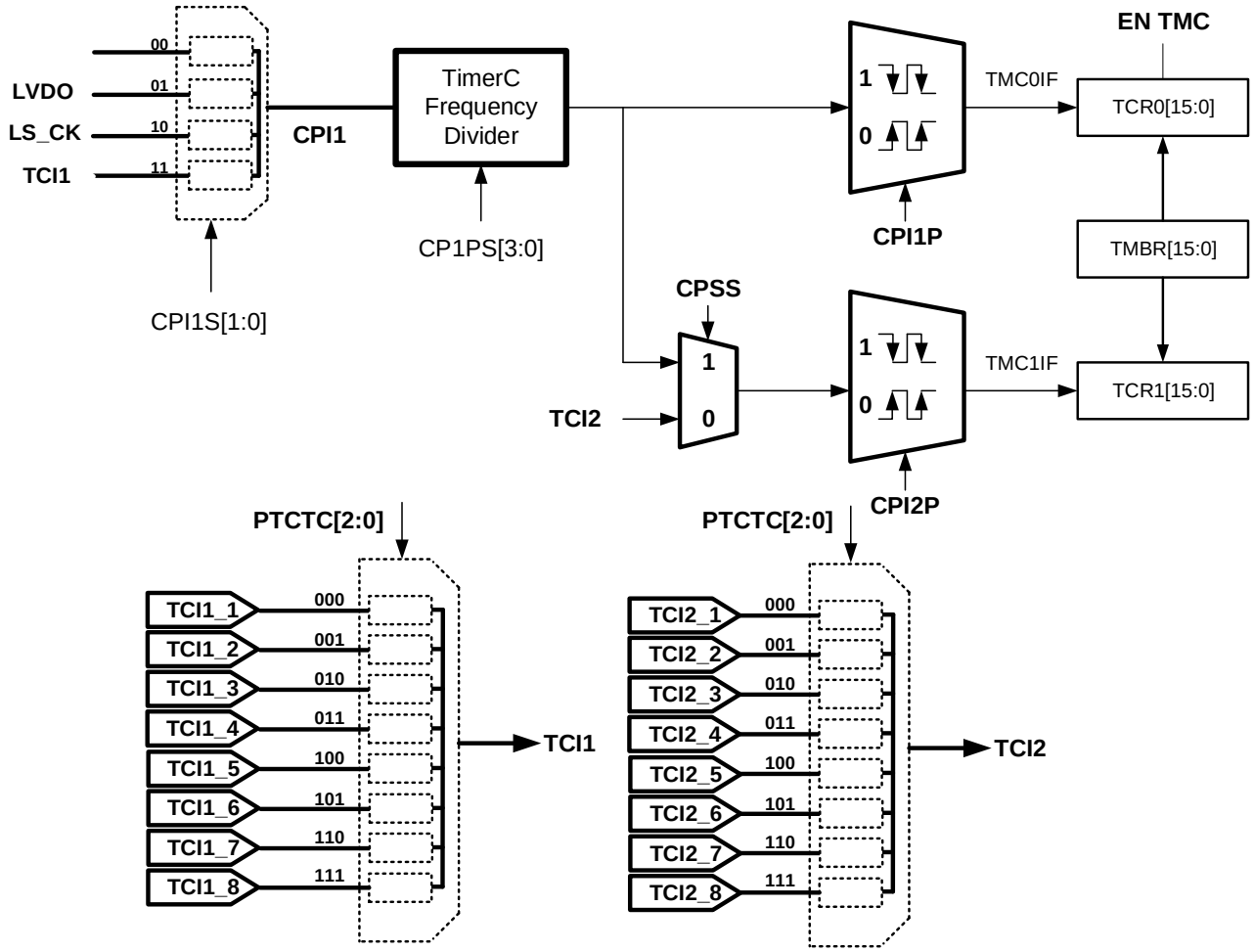


TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

4.10. 定时计数器 B 网络

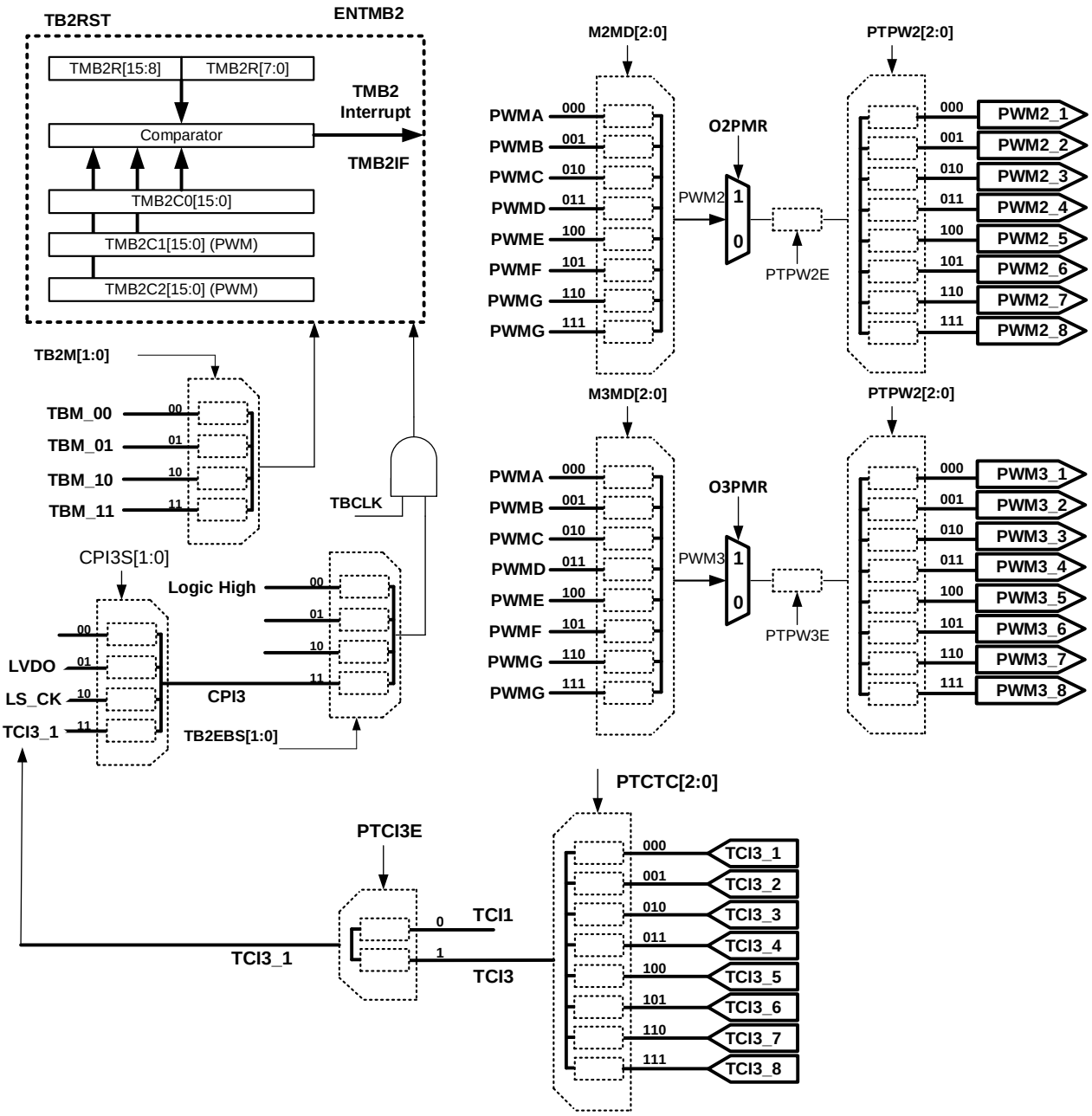


4.11. 定时计数器 C 网络

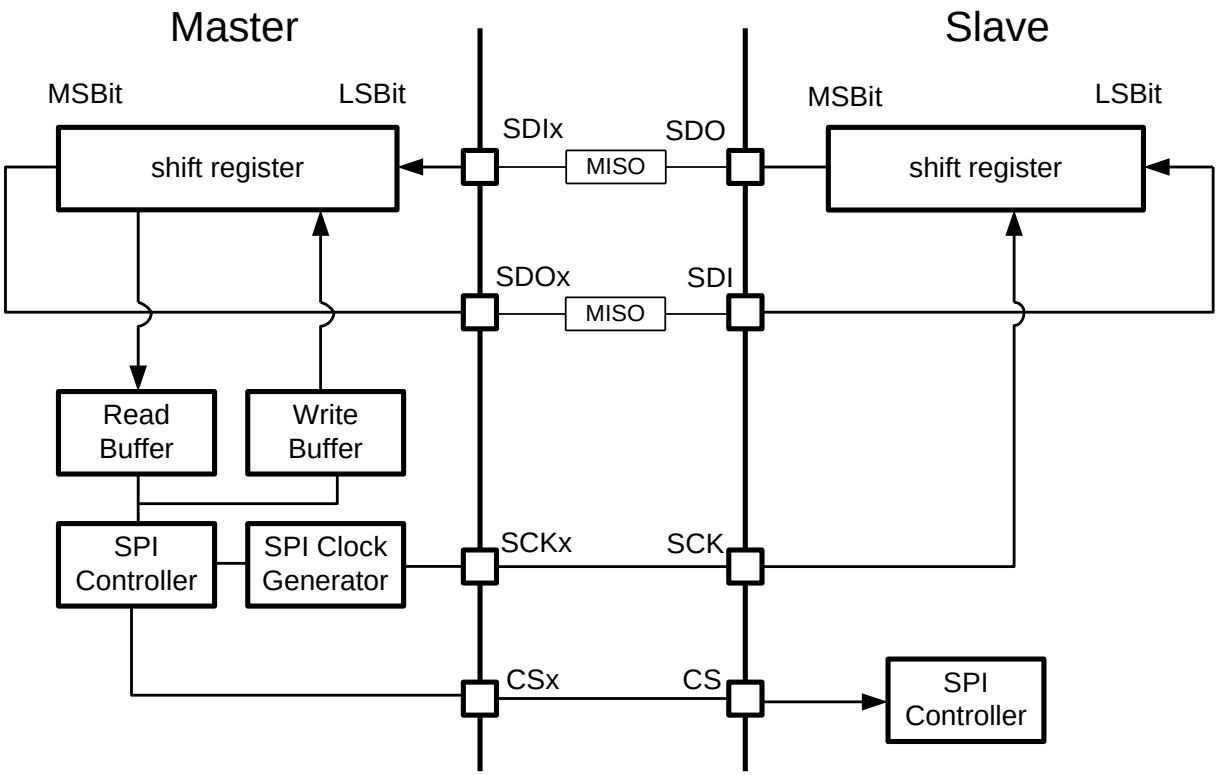


CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

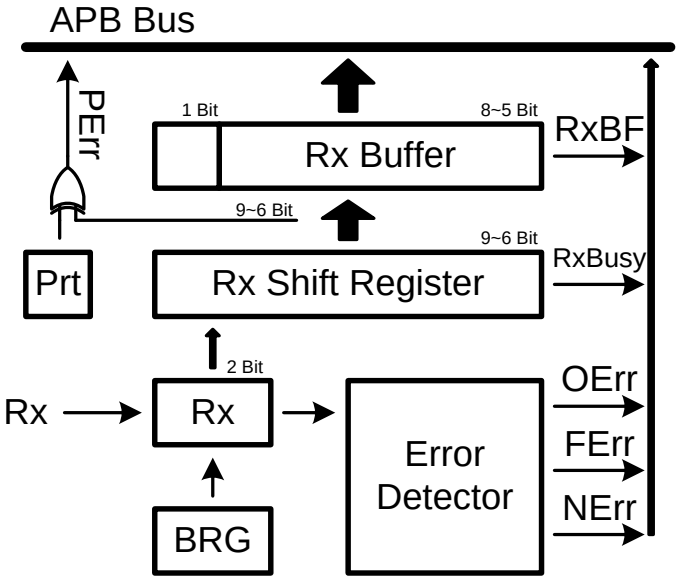
4.12. 定时计数器 B2 网络



4.13. 32-bit SPI 网络

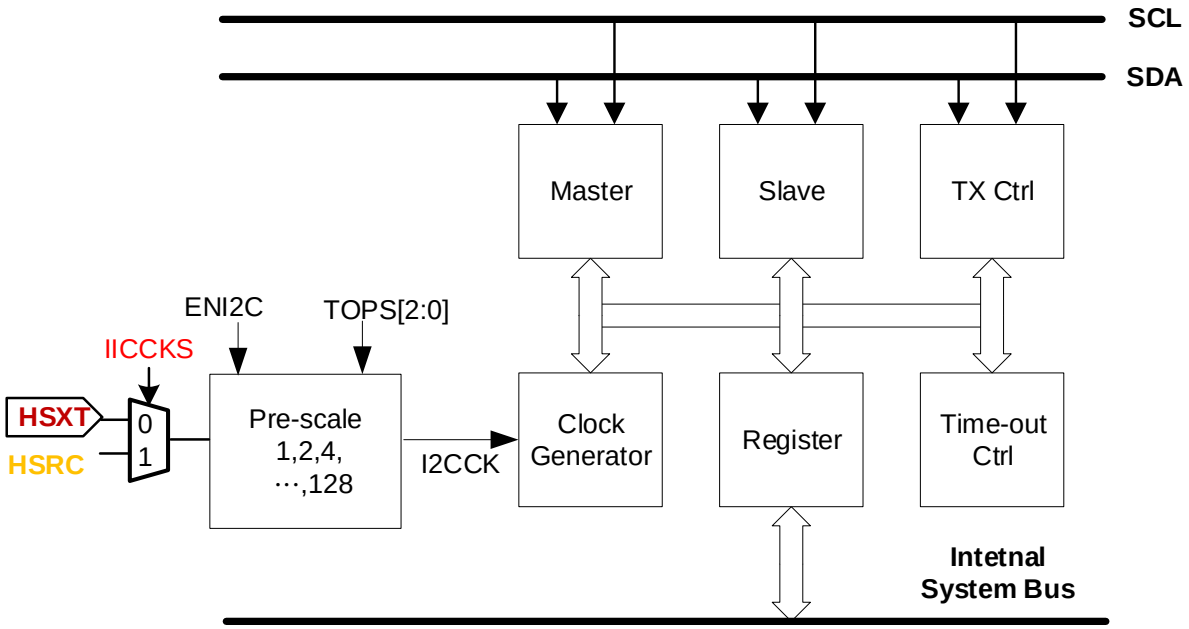


4.14. UART1/UART2 网络

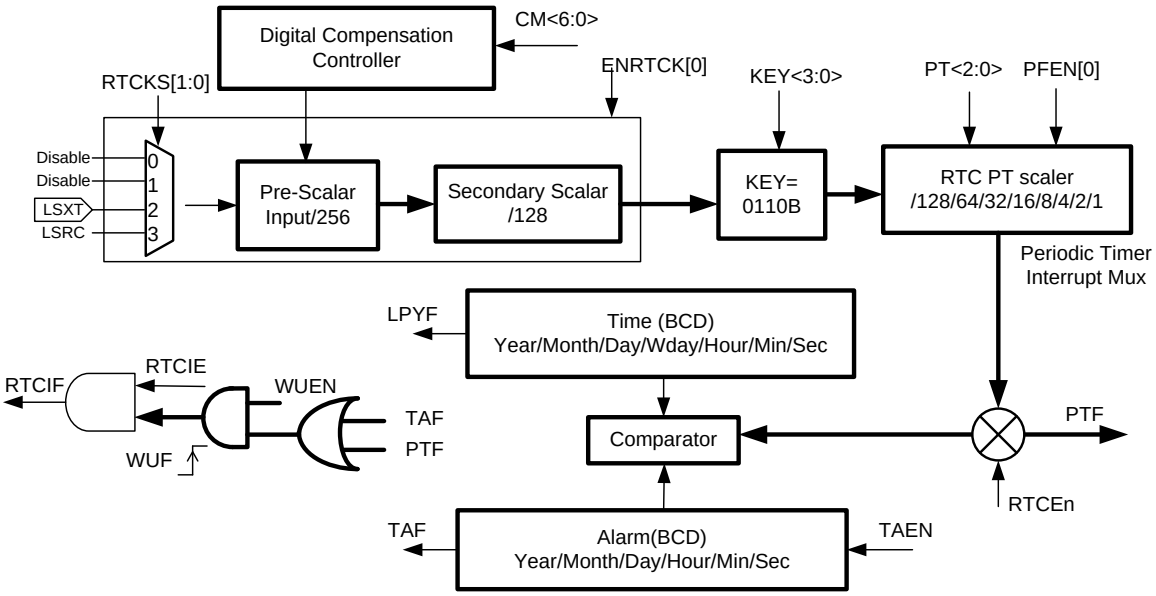


UART Receive Block Diagram

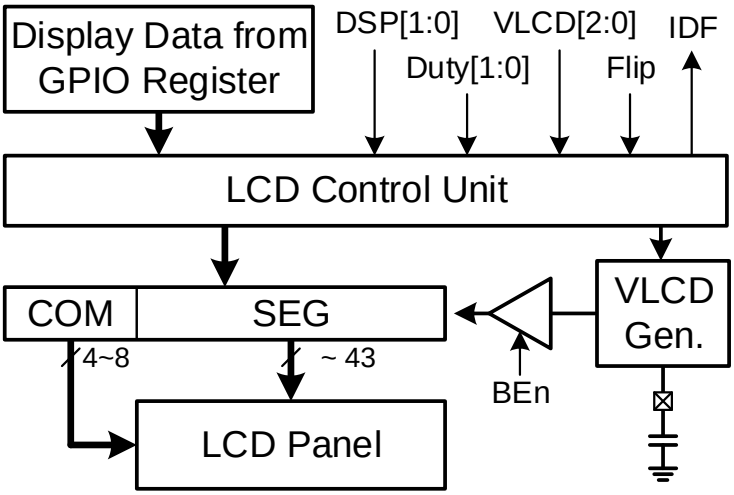
4.15. I²C 网络



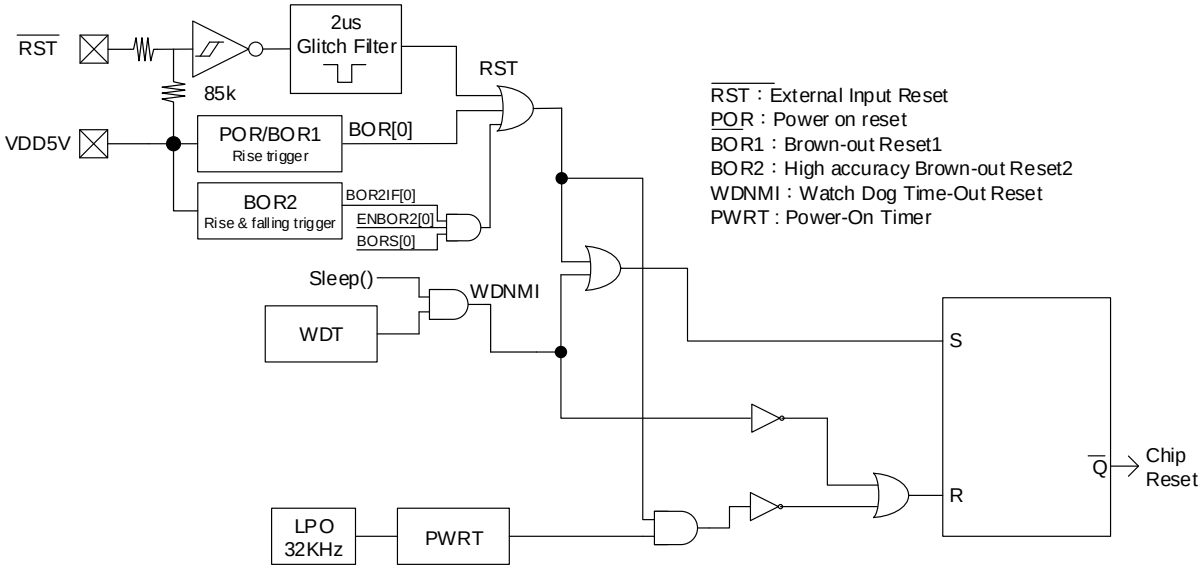
4.16. 硬件万年历 RTC 网络



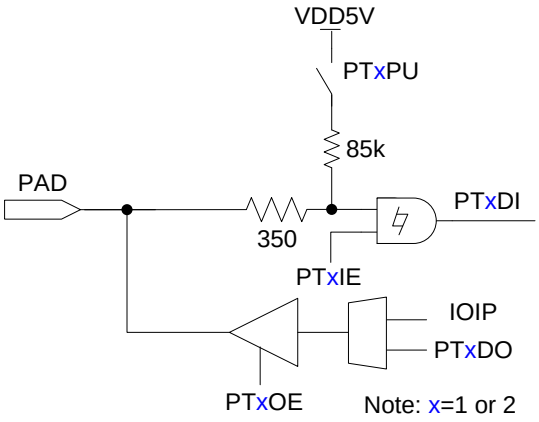
4.17. LCD 网络



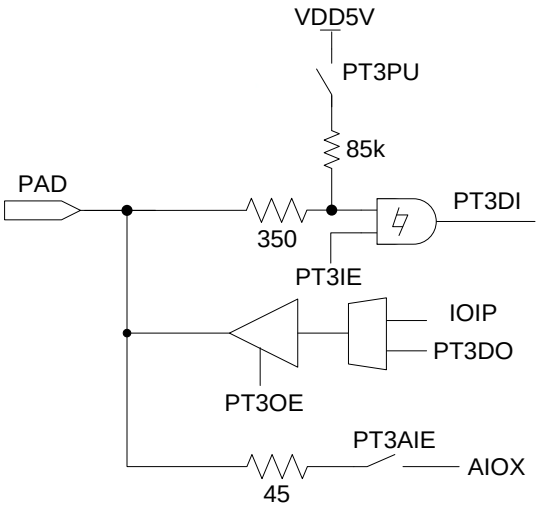
4.18. Reset/BOR1/BOR2 网络



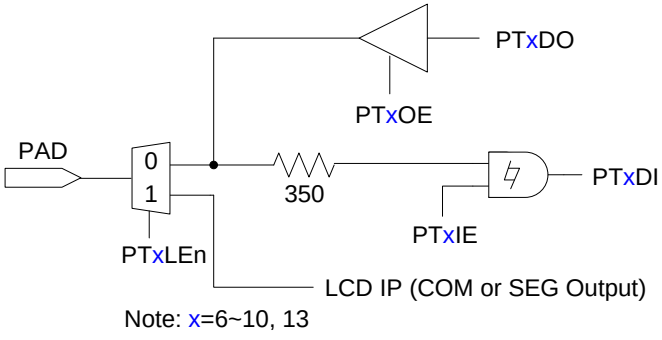
4.19. PT Port 1~2 网络



4.20. PT Port3 网络



4.21. PT Port6~10、13 网络



5. 电气特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)
Voltage applied at VDD5V to VSS ……—0.2 V to 6.0 V
Voltage applied to any pin …….... −0.2 V to VDD5V + 0.3 V
Diode current at any device terminal……..…..…….. ±2Ma
Storage temperature, Tstg: (UN programmed device) ..... −55℃ to 150℃
(Programmed device) ……..…….. −40℃ to 85℃
Soldering Temperature (10 Sec) ……. +260°C
Maximum output current sink by any PORT1 to PORT13 I/O PIN ……20Ma

5.1. Recommended Operating Conditions

VDD= VDD5V= 3.0V, TA=25℃, Unless Otherwise Noted

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD5V	Digital power	2.0		5.5	V
Supply Voltage	VDDA	Analog power	2.4		3.6	V
Supply Current	I_Sleep	Sleep Mode, @BOR2 OFF, VDD15 low power mode		1.8	4	uA
	I_Idle01	LSRC=32KHz, MCCK= LSRC/1, LSRC(LPO) IDLE Mode		4.5	8	uA
	I_Idle02	LSXT=32768Hz MCCK= LSRC/1, LSXT IDLE Mode		6	12	uA
	I_Idle03	HSRC=4.147MHz, MCCK= HSRC /1, HSRC IDLE Mode		80	120	uA
	I_Idle04	HSRC=31.795MHz, MCCK= HSRC /2, HSRC IDLE Mode		275	410	uA
	I_Free Run01	HSRC=4.147MHz, MCCK= HSRC/1		0.7		mA
	I_Free Run02	HSRC=31.795MHz, MCCK= HSRC /2,		2.5		mA
Power Up Delay	$t_{PU,DLY}$	Power on or wake up from sleep mode		4.1	7	ms

Note: HSRC=31.795MHz, MCCK= HSRC /2, CPU operate at VDD5V>=3V.

5.2. Clock System

typical values are at T_A=25℃ and VDD5V = 3.0V.Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
External High Speed Oscillator						
VDD5V	Operation voltage		2.0		5.5	V
F_{XHS}	High speed oscillator frequency	ohs_HS = 0b			4	MHz
		ohs_HS = 1b			8	MHz
		ohs_HS = 1b			16	MHz
I_{XHS}	High speed oscillator current	F_{XHS} = 16MHz, ohs_HS = 1b		130		uA
D_{XHS}	Duty of high oscillator		40		60	%
External Low Speed Oscillator						
F_{XLS}	Low speed oscillator frequency	VDD5V = 2.0V ~ 5.5V		32.768		KHz
I_{XLS}	Low speed oscillator current			2		uA
D_{XLS}	Duty of low speed oscillator		40		60	%
Internal High Speed Oscillator						
F_{HAO}	Internal high speed oscillator frequency	F_{HAO} = 4.147MHz, F_{HAO} = 4.147MHz, after trim	-10% -2%	4.147	+10% +2%	MHz
		F_{HAO} = 31.795MHz, F_{HAO} = 31.795MHz, after trim	-10% -2%	31.795	+10% +2%	MHz
	Voltage coefficient	VDD5V = 2.0V ~ 5.5 V		1		%
T_{HAO}	Temperature coefficient	-40~85℃		5		%
I_{HAO}	Internal high speed oscillator current	F_{HAO} = 4.147MHz		50		uA
		F_{HAO} = 31.795MHz (VDD5V>= 3.0V)		180		uA
D_{HAO}	Duty of oscillator		40		60	%
WT_{HAO}	Wake up time	F_{HAO} = 4.147MHz		15		us
Internal Low Speed Oscillator						
F_{LPO}	Internal low speed oscillator frequency		-20%	32	+20%	KHz
	Voltage coefficient	VDD5V = 2.0V ~ 5.5V		1		%
T_{LPO}	Temperature coefficient	-40~85℃		5		%
I_{LPO}	Internal low speed oscillator current			2.5		uA
D_{LPO}	Duty of low speed oscillator		40		60	%

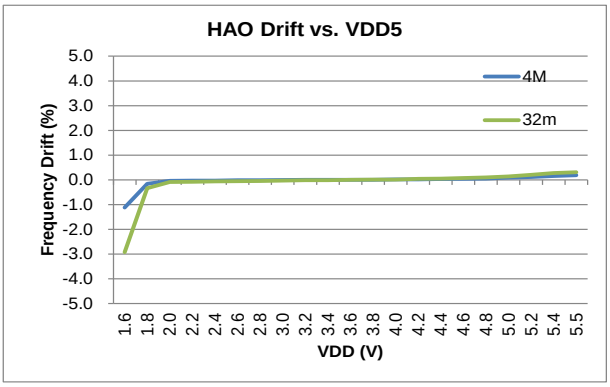


Figure5.2-1 HAO vs. VDD5V

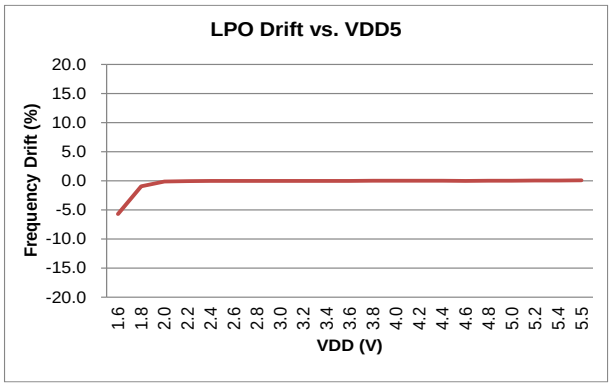


Figure5.2-2 LPO vs. VDD5V

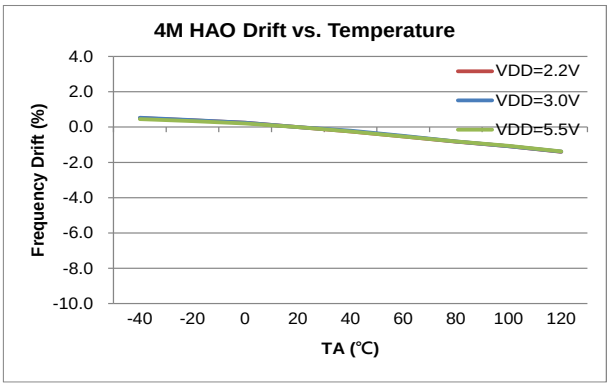


Figure5.2-3 HAO vs. Temperature

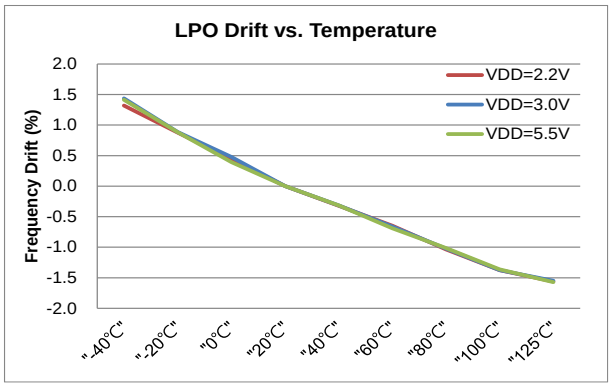


Figure5.2-4 LPO vs. Temperature

5.3. Power Management System

typical values are at T_A=25℃ and VDD= VDD5V= 3.0V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA LDO (Analog power)						
	Output voltage error		-5		5	%
	Capacitor loading		0.1	1	10	uF
	Settling time	Capacitor loading = 0.1Uf, 99% of VDDA		100		us
	Operation current	Bias + Band gap + VDDA LDO		35	50	uA
	Dropout voltage	VDD=2.9V, VDAS[1:0]=10b, I_L=10Ma		0.4		V
	Select VDDA output voltage, VDD=5.5V, I_L=0.1Ma	VDAS[1:0]=00b	-5%	2.4	+5%	V
		VDAS[1:0]=01b		2.6		
		VDAS[1:0]=10b		2.9		
		VDAS[1:0]=11b		3.2		
	Select VDDA output voltage, VDD=2.6V, I_L=10Ma	VDAS[1:0]=00b	-6%	2.4	+5%	V
	Voltage coefficient	VDD5V = 2.5 ~ 3.6V		0.2		%/V
		VDD5V = 3.6 ~ 5.5V		0.2		%/V
	Temperature coefficient			100		ppm/°C
VDD15 LDO (Digital Core power)						
	Output voltage		1.35	1.5	1.65	V
	Capacitor loading		0.1	0.47	1	uF
	Dropout voltage	Load = 10mA		0.2		V
	Voltage coefficient	VDD5V= 2.0 ~ 3.6V		0.5		%/V
		VDD5V= 3.6 ~ 5.5V		1		%/V
	Temperature coefficient			200		ppm/°C
REFO Buffer (Bnadgap reference Buffer)						
	Output voltage		1.1	1.2	1.3	V
	Capacitor loading		0.022	0.1	1	uF
	Operation current			20		uA
	Output current		-1		1	mA
	Temperature coefficient	VDDA=2.9 V		80		ppm/°C
	Voltage coefficient	VDDA= 2.4V ~ 3.6V		0.2		%/V

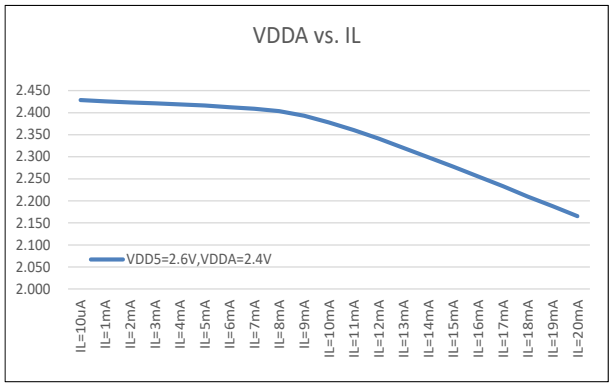


Figure5.3-1 VDDA vs. IL

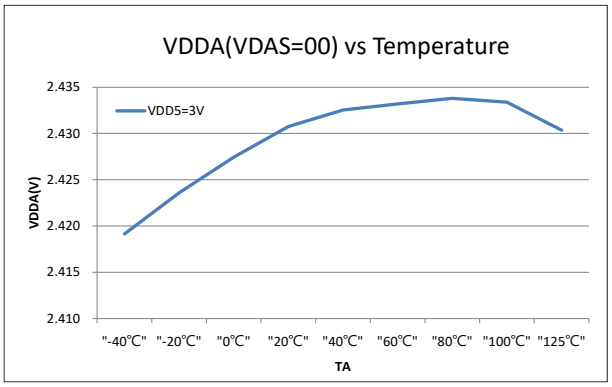


Figure5.3-2 VDDA vs. Temperature

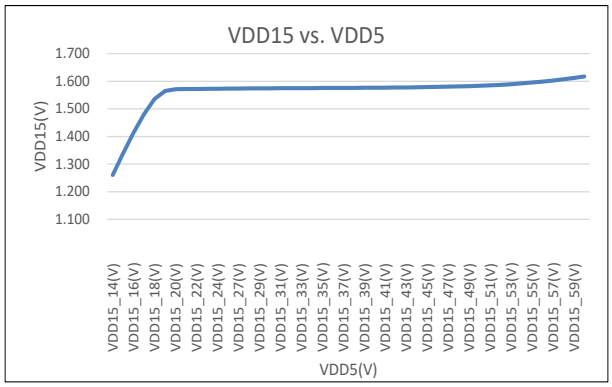


Figure5.3-3 VDD15 vs. VDD5

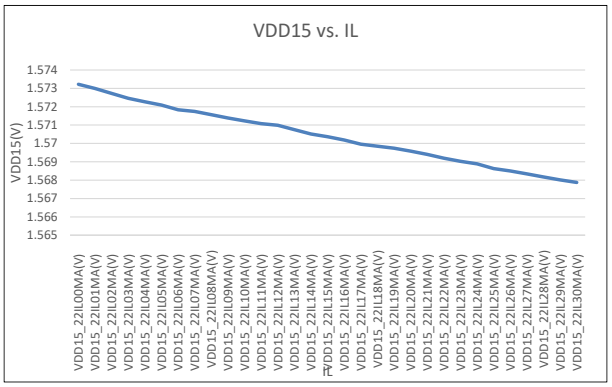


Figure5.3-4 VDD15 vs. IL

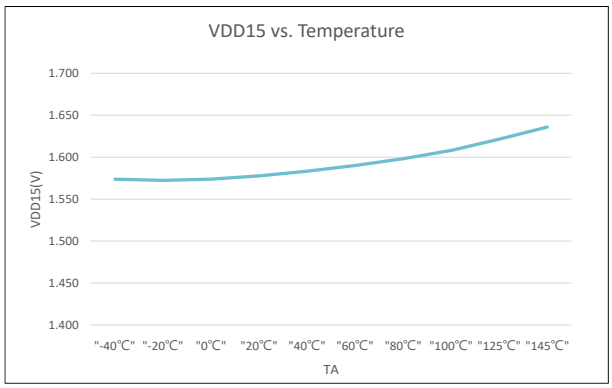


Figure5.3-5 VDD15 vs. Temperature

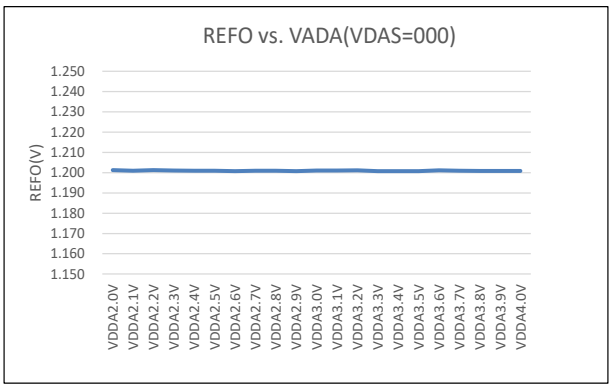


Figure5.3-6 REFO vs. VDDA

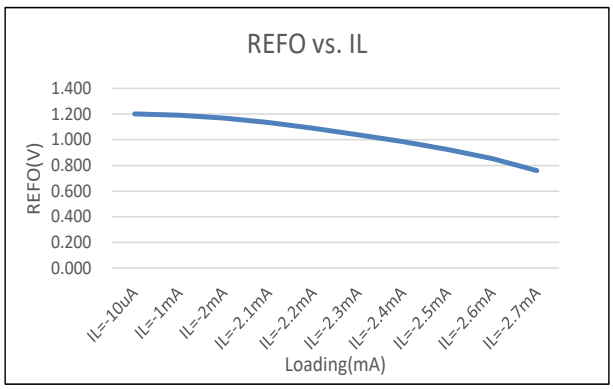


Figure5.3-7 REFO vs. IL

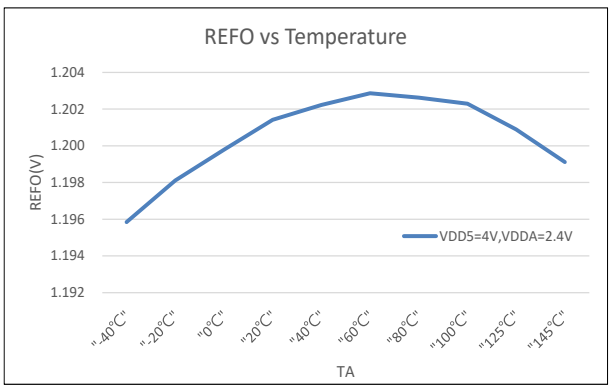


Figure5.3-8 REFO vs. Temperature

5.4. Reset Management System

typical values are at T_A=25℃ and VDD= VDD5V= 3.0V, Unless otherwise noted.

Sym.	Parameter		Min.	Typ.	Max.	Unit
BOR1	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$		2			us
	V_{DD5V} Start Voltage to accepted reset internally (H➔L),V_{LVR1}		1.2	1.4	1.6	V
	temperature drift, T_A=-40℃~85℃			30		%
	BOR1 current, I_{BOR1}, (include BOR1 and VDD15 LDO)			2.5	5	uA
BOR2	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR2}$		2			uS
	V_{DD5V} Start Voltage to accepted reset internally (L➔H),V_{HYS2}, and BORTH[2:0]:	000b		1.7		V
		001b		2.0		
		010b		2.2		
		011b		2.5		
		100b		2.7		
		101b		3.0		
		110b		3.6		
		111b		4.0		
	V_{DD} Start Voltage to accepted reset internally (H➔L),V_{LVR2}, and BORTH[2:0]:	000b~ 111b	13%	V_{HYS2}-0.06V	13%	V
	hysteresis, $V_{HYS2\text{-}LVR2}$			60		mV
	BOR2 current, I_{BOR2}			10	15	uA
	Temperature Drift			5		%
RST	Pulse length needed as RST pin to accepted reset internally, $t_{d\text{-}RST}$		2			us
	Input Voltage to accepted reset voltage			1.1		V
	Reset release voltage			1.6		V
BOR1/BOR2：Brownout Reset 1/2 RST：External Reset pin						

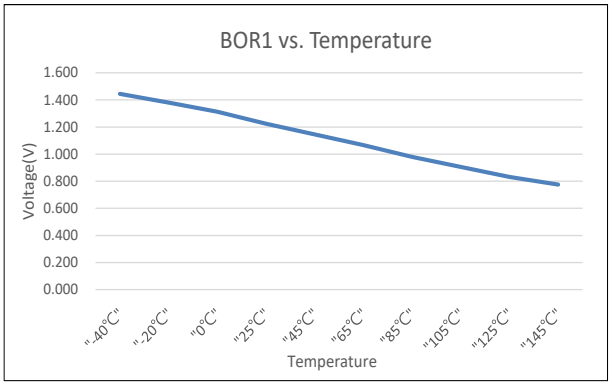


Figure5.4-1 BOR1 vs. Temperature

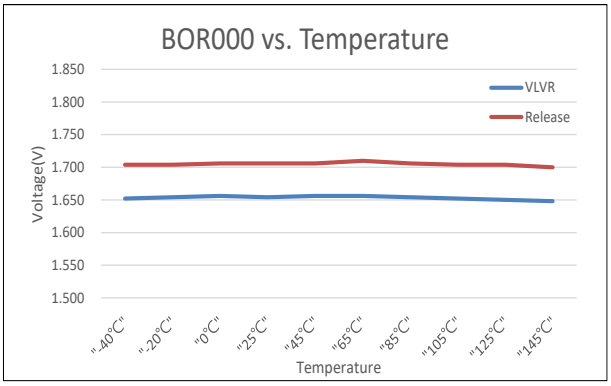


Figure5.4-2 BOR2 vs. Temperature

5.5. GPIO Port System

Typical values are at T_A=25℃ and VDD= VDD5V= 3.3V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PT 1 ~ 3 GPIO Port						
R_{PU}	Internal pull high resistor		65	85	105	Kω
V_{IH}	Input high voltage		0.75*V_{DD5V}			V
V_{IL}	Input low voltage				0.3*V_{DD5V}	V
V_{hys}	Input Voltage hysteresis(V_{IH} — V_{IL})			0.3*V_{DD5V}		V
I_{LKG}	Leakage Current				0.1	Ua
V_{OH}	High-level output voltage	V_{DD5V} =3.3V, I_{OH}=-10Ma,	V_{DD5V} -0.4			
		V_{DD5V} 5V, I_{OH}=-15Ma,	V_{DD5V} -0.4			
V_{OL}	Low-level output voltage	V_{DD5V} =3.3V, I_{OL}=10Ma			V_{SS} +0.4	
		V_{DD5V} =5V, I_{OL}=15Ma			V_{SS} +0.4	
PT 6 ~ 10、13 GPIO Port						
R_{PU}	Internal pull high resistor			NA		
V_{IH}	Input high voltage		0.75*V_{DD5V}			V
V_{IL}	Input low voltage				0.3*V_{DD5V}	V
V_{hys}	Input Voltage hysteresis(V_{IH} — V_{IL})			0.3*V_{DD5V}		V
I_{LKG}	Leakage Current				0.1	Ua
V_{OH}	High-level output voltage	V_{DD5V} =3.3V, I_{OH}=10Ma,	V_{DD5V} -0.5			
		V_{DD5V} =5V, I_{OH}=15Ma,	V_{DD5V} -0.5			
V_{OL}	Low-level output voltage	V_{DD5V} =3.3V, I_{OL}=-10Ma			V_{SS} +0.4	
		V_{DD5V} =5V, I_{OL}=-15Ma			V_{SS} +0.4	

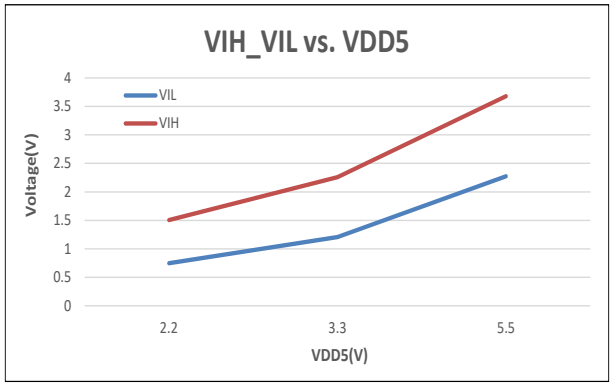


Figure5.5-1 VIH/VIL vs. VDD5V

5.6. ADC Management System

all specifications at T_A=-40℃ to +85℃, VDDA=REFP=2.4V, REFN=VSS, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Analog Inputs						
	Full-scale input voltage —(VINP — AINN)	Considering ADC performance matches ADC ENOB table. REFP=VDDA, REFN=VSS VREF be set to 1/2 only	±0.5*VREF/Gain			V
		Considering ADC performance matches ADC ENOB table. REFP=REFO_I REFN=VSS VREF be set to 1 only	±VREF/Gain			
	Common-mode input range	Gain = 1, @25℃	VSS-0.2V		VDDA	V
System Performance						
	Resolution	No missing codes		24		Bits
	Data rate			ADC Clock /OSR		SPS
	Digital filter settling time	Full setting		3		Data
	Integral nonlinearity (INL)	Differential input End-point fit, OSR=65536		30		PPM
	ADC Gain drift			5	10	ppm/℃
	Normal-mode rejection	f_{IN}=60Hz ±1Hz, Output rate = 15 SPS		70		dB
	Common-mode rejection	ΔVDDA = 0.1V @ DC		80		dB
	Input-referred noise	Output rate= 31 SPS, ADC Gain=1		2.04		uV, rms
	Power-supply rejection	ΔVDDA = 0.1V @ DC		80		dB
Voltage Reference Input						
	Voltage reference input	—VREF = REFP — REFN			VDDA	V
	Positive Reference Input	REFP, @25℃	VDDA/2		VDDA	V
	Negative Reference Input	REFN, @25℃	VSS		VDDA/2	V
ADC Modulator Current						
ADC	ADC Modulator	VDD5V=3.3V,VDDA=2.4V, ADC Clock=1Mhz		300		uA
PGA	ADC PGA	VDD5V=3.3V,VDDA=2.4V		700		uA

ADC ENOB and RMS Noise

Typical values are at TA=25℃and VDD5V(VDD)= 3.3V, VDDA=2.4V and A/D Clock=4M/4=1MHz, unless otherwise noted. HY16F3910 provides important input noise specification that aims at ΣΔADC. Below twoTables lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short with 1K load cell, voltage reference: 1.2V and 1024 records were sampled.

NOTE : Because the settable over-sampling rate(OSR) range is 64~32768, the output rate range that HY16F3910 can support is**15625Hz~31Hz**.Below two tables do not show the ADC ENOB and RMS Noise performance of each stage of OSR.

ENOB(RMS) with OSR/GAIN at CPUCK=4MHz, A/D Clock=4M/4=1MHz, VDDA=2.4V, VREF=AI2-AI3=VDDA-VSS,VRGN=0.5, Vin=AI0-AI1,ext short with 1K load cell									
OSR					**128**	**512**	**2048**	**8196**	**32768**
Output rate(Hz)					**7813**	**1953**	**488**	**122**	**31**
Gain	**=**	**PGAGN**	**x**	**ADGN**					
1	**=**	**off**	**x**	**1**	16.48	17.5	18.47	19.15	20.18
2	**=**	**off**	**x**	**2**	16.38	17.61	18.19	19	20.25
3	**=**	**off**	**x**	**3**	16.22	17.22	18.17	19.06	20.19
4	**=**	**off**	**x**	**4**	15.84	16.92	17.97	19	20.34
8	**=**	**8**	**x**	**1**	16.5	17.52	18.43	19.07	19.7
16	**=**	**16**	**x**	**1**	16.13	17.11	18.18	19.09	19.7
32	**=**	**32**	**x**	**1**	16.15	16.81	17.63	18.83	19.71
32	**=**	**8**	**x**	**4**	15.3	15.94	17.23	18	19.05
64	**=**	**16**	**x**	**4**	14.55	15.77	16.67	17.53	18.44
128	**=**	**32**	**x**	**4**	14.18	15.14	16.2	17.37	18.15

Table 5.6-1ΣΔADC ENOB Table

RMS Noise(uV) with OSR/GAIN at CPUCK=4MHz, A/D Clock=4M/4=1MHz, VDDA=2.4V, VREF=AI2-AI3=VDDA-VSS, VRGN=0.5; Vin=AI0-AI1, ext.short with 1K load cell									
OSR					128	512	2048	8196	32768
Output rate(Hz)					7813	1953	488	122	31
Gain	**=**	**PGAGN**	**x**	**ADGN**					
1	**=**	**off**	**x**	**1**	26.376	13.049	6.672	4.146	2.038
2	**=**	**off**	**x**	**2**	14.145	6.043	4.043	2.311	0.966
3	**=**	**off**	**x**	**3**	10.559	5.275	2.739	1.472	0.674
4	**=**	**off**	**x**	**4**	10.337	4.881	2.356	1.151	0.454
8	**=**	**8**	**x**	**1**	3.257	1.603	0.858	0.547	0.369
16	**=**	**16**	**x**	**1**	2.112	1.065	0.508	0.272	0.184
32	**=**	**32**	**x**	**1**	1.041	0.657	0.371	0.162	0.088
32	**=**	**8**	**x**	**4**	1.874	1.204	0.490	0.288	0.139
64	**=**	**16**	**x**	**4**	1.570	0.676	0.363	0.200	0.139
128	**=**	**32**	**x**	**4**	1.016	0.522	0.252	0.111	0.065

Table 5.6-2 ΣΔADC RMS Table

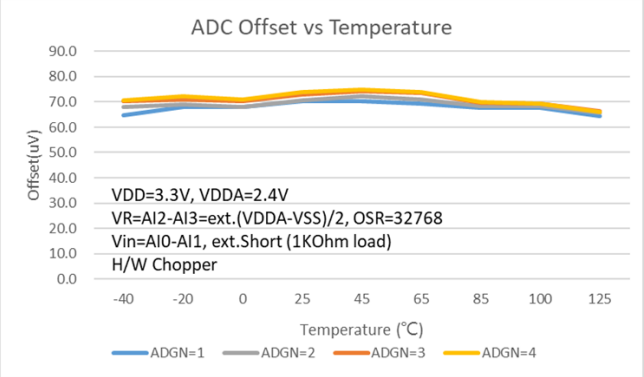


Figure5.6-1 ADC Offset vs Temperature

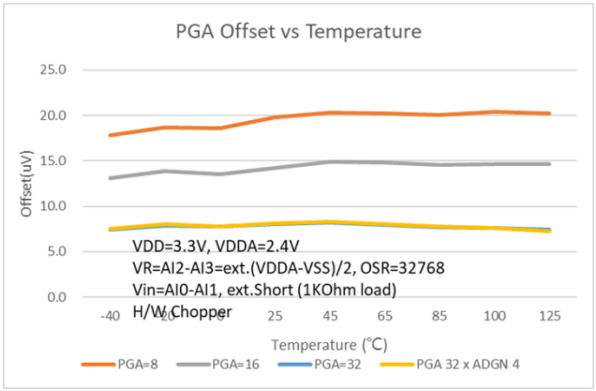


Figure5.6-2 PGA Offset vs Temperature

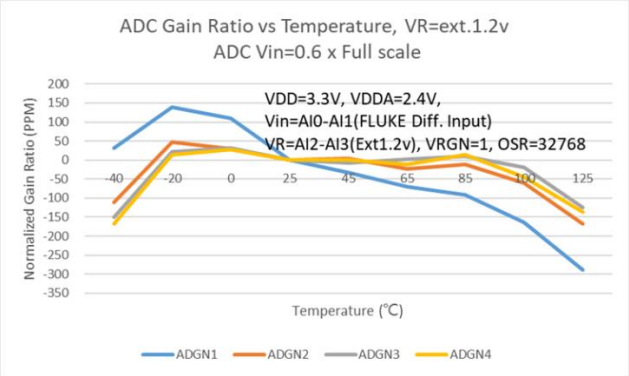


Figure5.6-3 ADC Gain Ratio vs Temperature

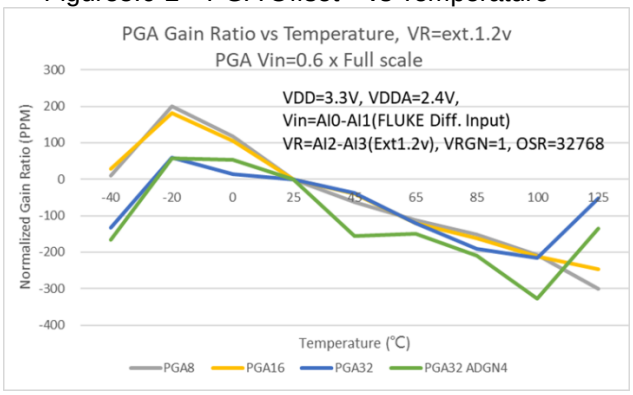


Figure5.6-4 PGA Gain Ratio vs Temperature

5.7. Internal Temperature Sensor

typical values are at T_A=25℃, VDD= VDD5Vp= 3.0V, and VDDA=2.4V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			172		Uv/℃
KT	absolute temperature scale 0K			-286		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

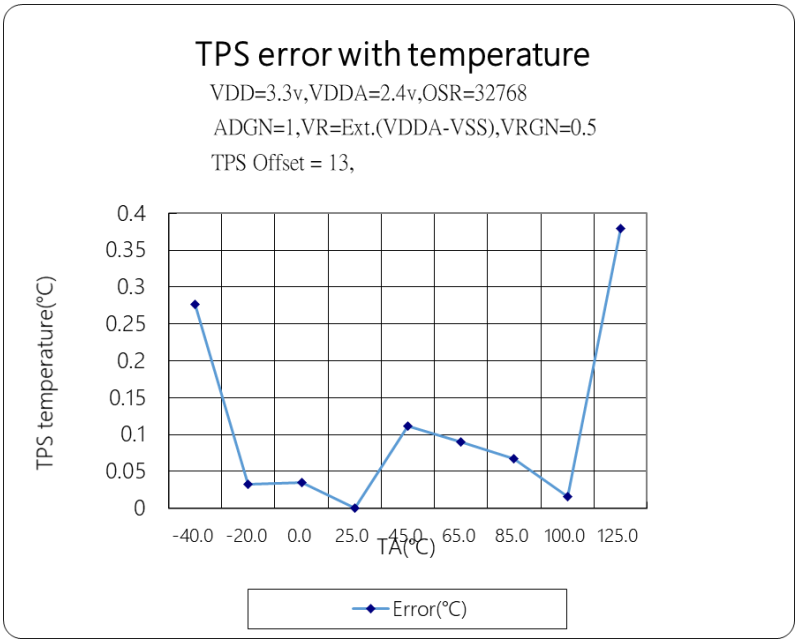


Figure5.7-1 ADC Temperature Sensor Error

5.8. LVD Comparator Management System

Typical values are at TA=25℃ and VDD= VDD5V= 3.0V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LVD	operation current, I_{V12_BOR}			2.5		uA
	Operation current, I_{V12_BGR}			10		uA
	V12_BOR Reference Voltage		1.1	1.2	1.3	V
	V12_BOR Reference Voltage Temperature drift			200		PPM/℃
	V12_BOR Reference Voltage to VDD5V Voltage drift			±2		%/V
	V12_BGR Reference Voltage		1.15	1.2	1.25	V
	V12_BGR Reference Voltage Temperature drift			50		PPM/℃
	V12_BGR Reference Voltage to VDD5V Voltage drift			±2		%/V
	compare reference voltage temperature drift, T_A = -40℃ ~ 85 ℃			50		ppm/℃
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1111b			LVDIN		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1110b		5%	4.0	5%	V
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1101b			3.6		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1100b			3.3		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1011b			3.0		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1010b			2.9		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1001b			2.8		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1000b			2.7		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0111b			2.6		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0110b			2.5		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0101b			2.4		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0100b			2.3		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0011b			2.2		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0010b			2.1		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0001b			2.0		
	detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0000b			Off		
LVD：Low Voltage Detect						

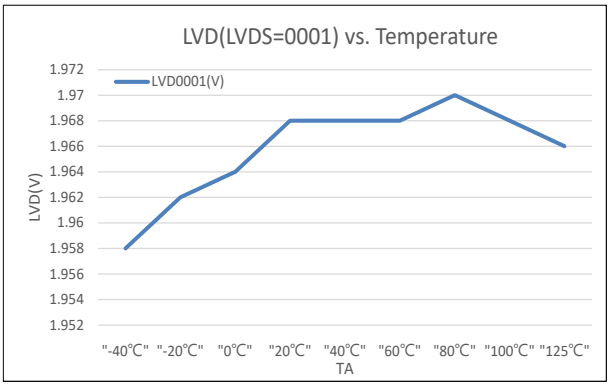


Figure5.8-1 LVD vs. Temperature

5.9. LCD System

Typical values are at T_A=25℃, VDD= VDD5V= 3.3V, and C_{VLCD}=4.7uF, Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LCD}	Operation Current Charge Pump Mode		W/O Panel		20		uA
V_{LCD}	Supply Voltage Range	VLCD	With Buffer, enlcdp[0]=0b	2.5		5.5	V
		enlcdp[0]=1b @VDD5V > 2.0V	VLCD=111b, @VDD5V>=2.75V		5.0		V
			vlcd=110b @VDD5V>=2.5V		4.5		
			vlcd=101b @VDD5V>=2.2V		3.94		
			vlcd=100b @VDD5V>=2V		3.3		
			vlcd=011b		3.0		
			vlcd=010b		2.8		
	VDD Voltage drift	enlcdp[0]=1b			5		%
Z_{LCD}	Output Impedance With LCD Buffer	F_{LCD} = LS_CK/32/9, VLCD = 3 V			10		KΩ

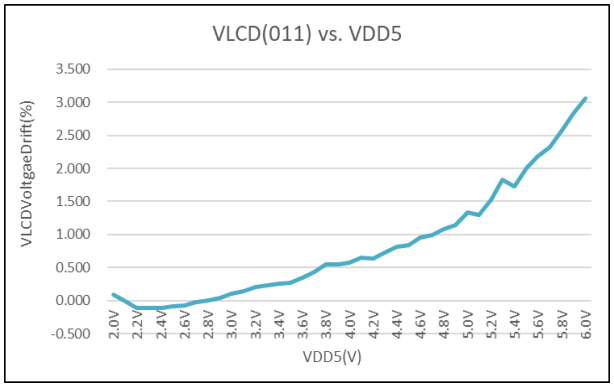


Figure5.9-1 VLCD vs. VDD5V

5.10. Flash Memory

Typical values are at T_A=-40˚C~ 85˚C, VDD= VDD5V= 3.3V, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	V_{DD5V} Supply voltage		2.0		5.5	V
	Program/Erase supply current				4	mA
	Data retention time		10			Years
	Number of program/Erase cycles(Endurance)		100			K Cycles
	Mass Erase time		10			ms
	Sector Erase time		2			ms
	Word Write time		20			us

6. 订货信息

下单品名 [1]	封装型式	引脚数	封装型式描述方式		程序代码编号 [2]	出货包装形式	个装数量	材料组成	MSL[3]
HY16F3910—N088	QFN	88	N	088	-	Tray	168	Green[4]	MSL-3
HY16F3910—L080	LQFP	80	L	080	-	Tray	160	Green[4]	MSL-3
HY16F3910—L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3

[1] 产品名称品名封装型式描述方式装型程序代码编号（空白片 / 标准品 / 代客烧录码）:

例如：您的需求是 HY16F3910 不带程序代码的空白片且需要的产品是封装片 QFN88 出货，则下单品名为 HY16F3910—N088，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的 HY16F3910 代客烧录服务申请的程序代码编号为 001，而需求的产品是封装片 QFN88 出货，则下单品名为 HY16F3910—N088-001，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的需求是 HY16F3910 不带程序代码的空白片且需要的产品是封装片 LQFP80 出货，则下单品名为 HY16F3910—L080，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的 HY16F3910 代客烧录服务申请的程序代码编号为 005，而需求的产品是封装片 LQFP80 出货，则下单品名为 HY16F3910—L080-005，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的需求是 HY16F3910 不带程序代码的空白片且需要的产品是封装片 LQFP64 出货，则下单品名为 HY16F3910—L064，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的 HY16F3910 代客烧录服务申请的程序代码编号为 009，而需求的产品是封装片 LQFP64 出货，则下单品名为 HY16F3910—L064-009，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

[2] 程序代码编号:

“式码编号装形式为外，请为标准品或代客烧录申请的程序代码编号，而空白芯片不带此码。

[3] MSL:

湿度敏感性等级系依据 IPC/JEDEC J-STD-020 的规范加以试验分级，并参考 IPC/JEDEC J-STD-033 的标准处理、包装、运输与使用。

[4] Green (RoHS & no Cl/Br):

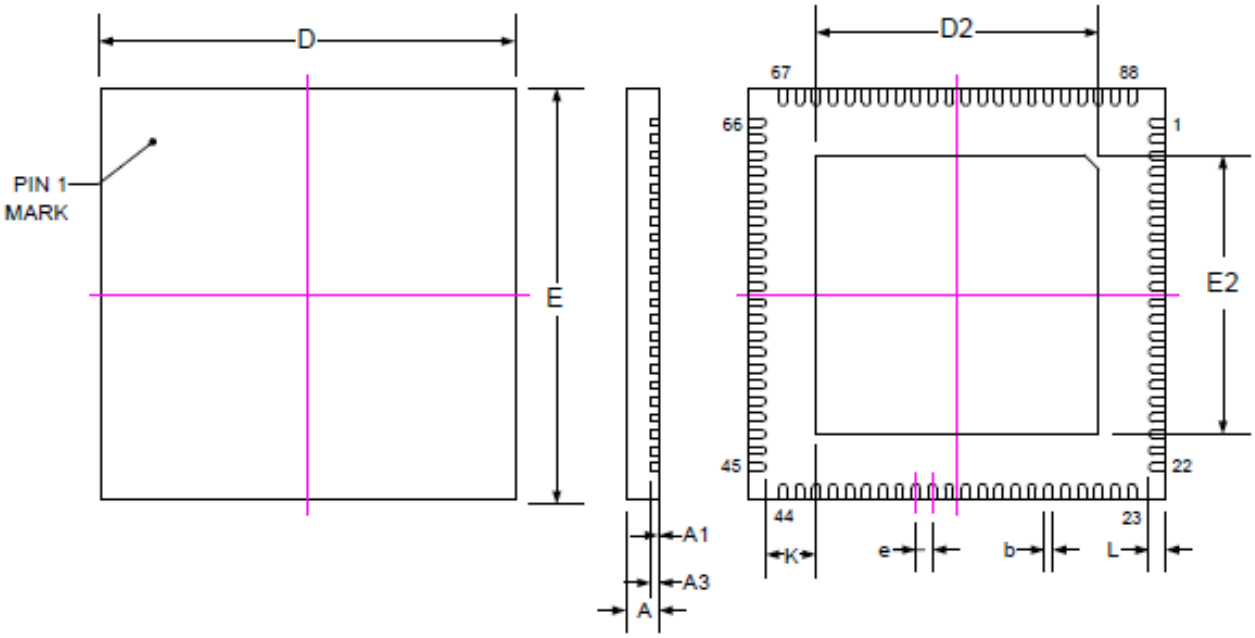
HYCON 产品皆为 Green Product，符合 RoHS 指令，REACH 高关注物质(SVHC)以及无卤素规定 (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

7. 封装尺寸信息

7.1. QFN88(N088) (TYPE 1)

7.1.1. Package Dimensions QFN88(10x10)

Unit: mm



SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		10.00 BSC	
E		10.00 BSC	
e		0.40 BSC	
D2	6.75	6.80	6.85
E2	6.75	6.80	6.85
L	0.30	0.40	0.50
K	1.08	1.20	1.33

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm
4. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

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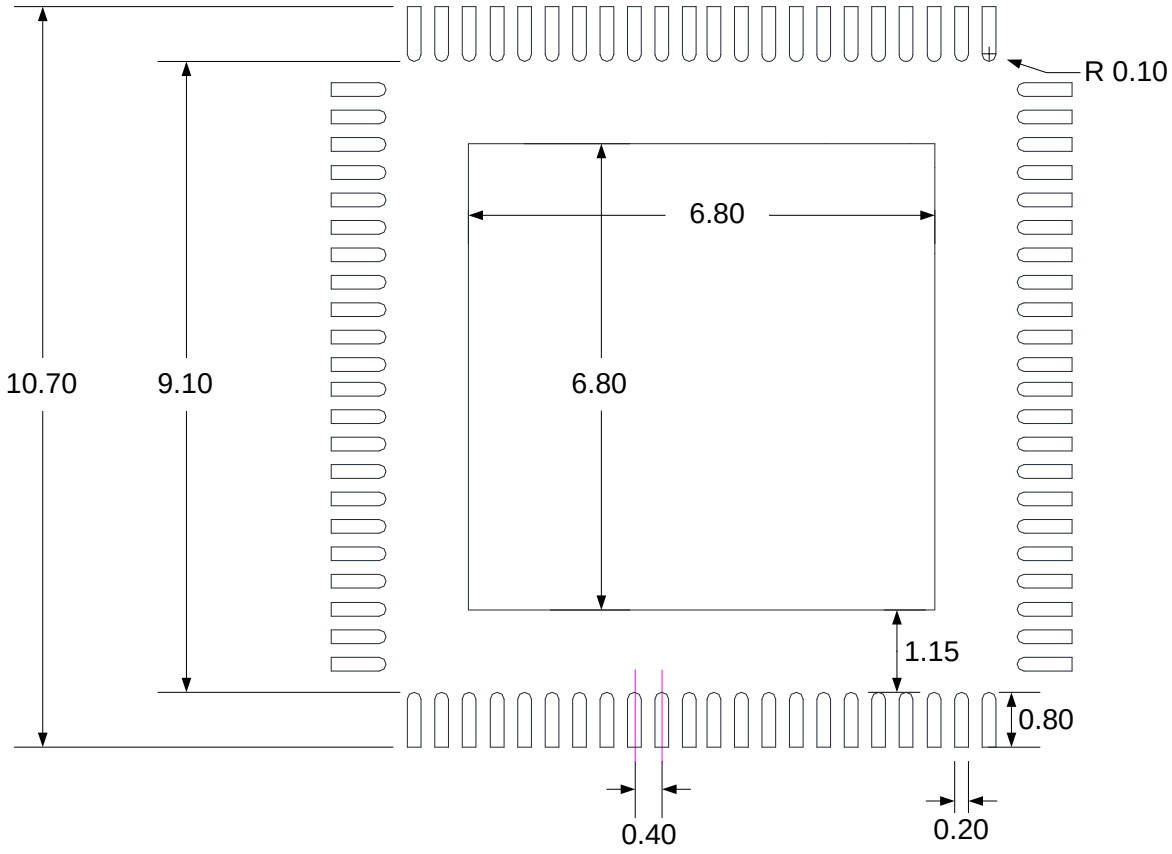
7.1.2. Land Pattern Design Recommendations



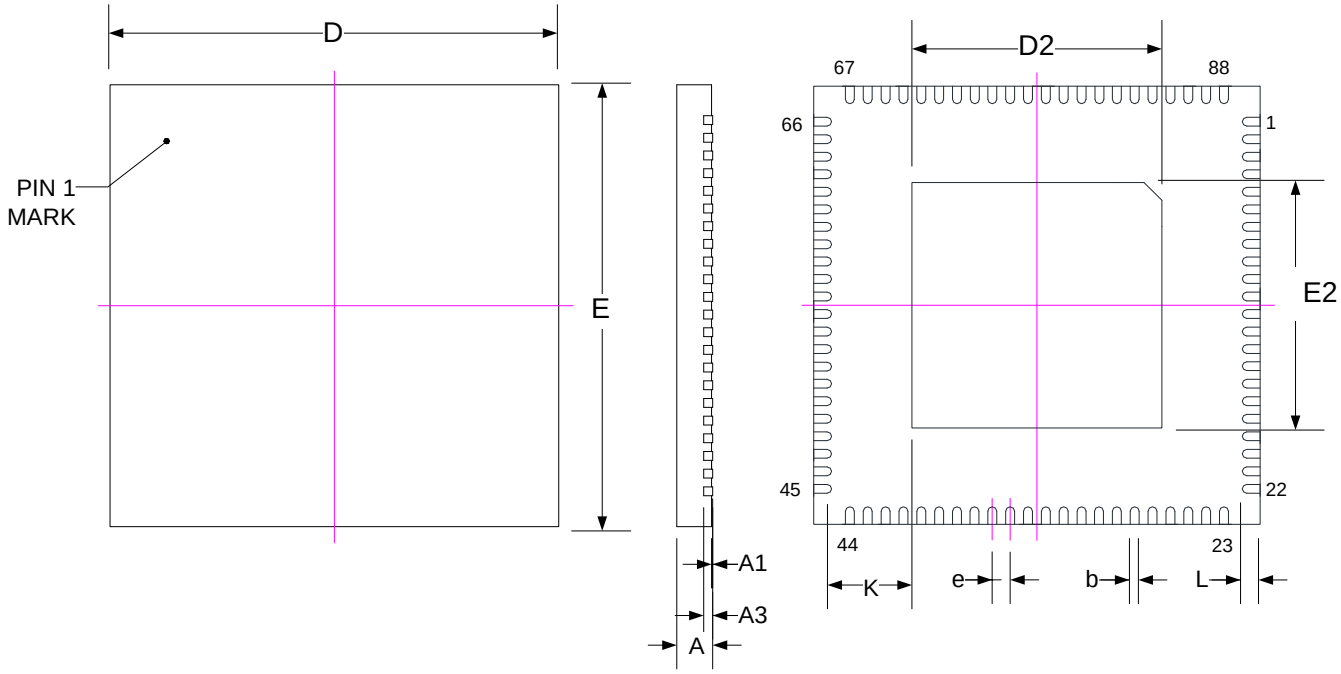
Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm

7.2. QFN88(N088) (TYPE 2)

7.2.1. Package Dimensions QFN88(10x10)

Unit: mm

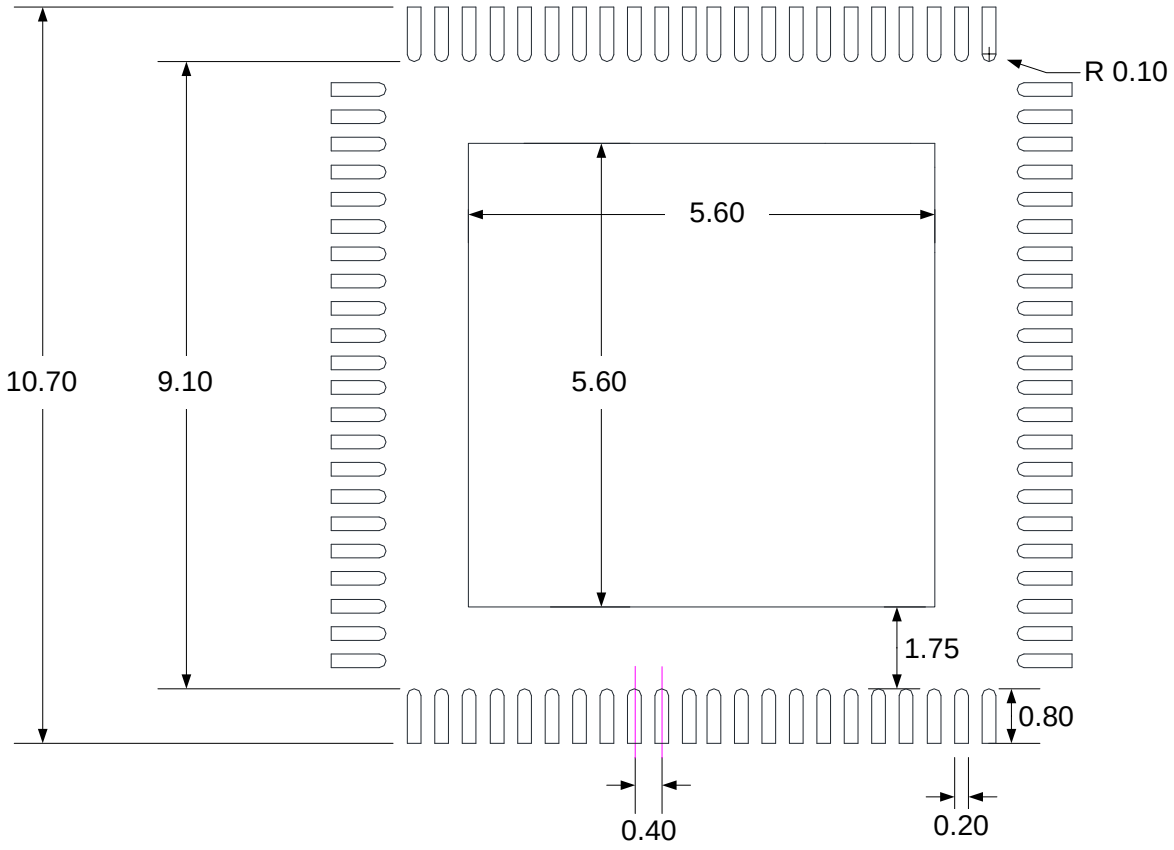


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		10.00 BSC	
E		10.00 BSC	
e		0.40 BSC	
D2	5.45	5.60	5.75
E2	5.45	5.60	5.75
L	0.30	0.40	0.50
K	1.62	1.80	1.98

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

7.2.2. Land Pattern Design Recommendations



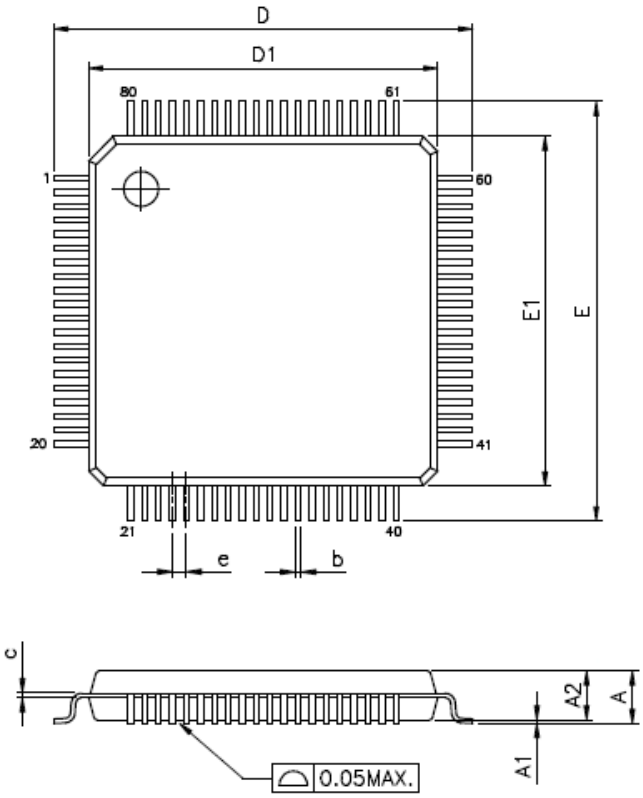
Note:

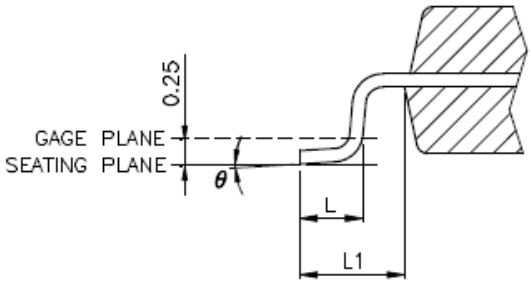
1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm

7.3. LQFP80(L080)

7.3.1. Package Dimensions LQFP80(10x10)

Unit: mm





SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	--	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

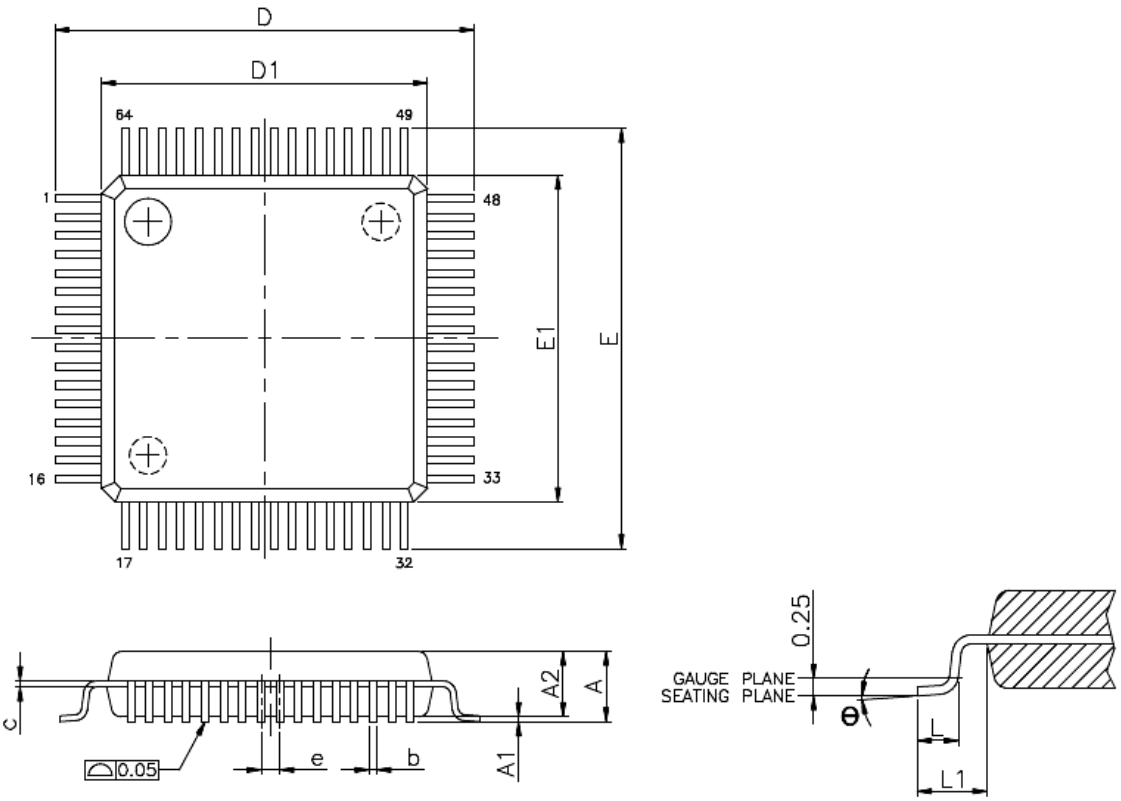
Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

7.4. LQFP64(L064)

7.4.1. Package Dimensions LQFP64(7x7)

Unit: mm



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8. 修订记录

以下描述本文件差异较大的地方，而标点符号与字形的改变不在此描述范围。

文件版次	页次	日期	摘要
V01	ALL	2021/11/24	初版发行
V02	ALL	2022/9/14	1、 修改 Page6:1 章节-修改选型总表的字体型号，及'Pin'改为'Package'。 2、 Page62: 7.1.2 章节 删除链接 'http://www.hycontek.com/attachments/MSP/OJTI-HM-2013-002.pdf' 3、 Page64：7.2.2 章节 删除链接 'http://www.hycontek.com/attachments/MSP/OJTI-HM-2013-002.pdf' 4、 Page54: 5.6 章节–在 ADC ENOB Table 之前添加 'ADC ENOB And RMS Niose'文字描述。 5、 Page11: 2.2.1 章节-SDRV1/SDRV2 pin 的功能说明修改为'Reserved，内部测试，不需连接，保持空接即可'。
V03	ALL	2022/11/01	1、4.4 章节 时钟系统网络：修改 UART/UART2 的频率网络图，增加 HXST 作为频率源使用设置，及使用范例说明。 2、4.8 章节 看门狗网络：修改 WDTO[14:0]除频值。
V04	ALL	2022/11/14	1、4.4 章节 时钟系统网络： 移除 GPIO 时钟网络图 2、2.2.1 章节 引脚定义： 修改 VDD15 引脚说明，外接电容改为 1uF。 3、3.1 章节 桥式传感器应用电路： VDD15 电容改为 1uF；VDD5V 增加 0.1uF 电容。 4、3.2 章节 血压传感器应用电路： VDD15 电容改为 1uF；VDD5V 增加 0.1uF 电容。 应用电路断开 pin3 与 pin1/pin6 的连接。 5、4.5 章节 电源系统网络图：修改 VDD15 电容为：0.1~1uF; 6、5.9 章节 LCD System： '@VDD5V>=2.5V' 取消超链接功能； '@VDD5V>=2.2V' 取消超链接功能；