HYCON TECHNOLOGY

HY16F3981

规格书

高精密混合信号处理控制器

4X32 ~ 6X30 LCD Driver

32-bit 低功耗微控制器

21-bit ENOB ΣΔADC

64KB Flash ROM

目录

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1. 特性

数位功能

- 32-bit 1T Andes Core E801 内核
- 支持 C 开发环境指令集
- 数字工作电压 2.2V to 3.6V.
- 工作温度-40 to 85℃
- 低功耗:
  - 运行模式: 0.6mA@CPU_CK:2MHz/2
  - 待机模式:5uA@LSRC=35KHz
  - 休眠模式:Typ.2.5uA
- 64KB Flash ROM、8KB SRAM
  - Write/Erase 的周期次数为 ：20,000 次
  - Write/Read/Erase 的操作电压为 ：2.7V~3.6V
- 16-bit Timer A, Timer B(x2), Timer C
- 16-bit PWM 控制器及信号捕捉功能
- 硬件实现 32-bit SPI/UART(x2)/I2C 通信接口
- 硬件实现时钟 RTC 万年历功能
- 4x32 ~ 6x30 LCD 液晶驱动器：
  1/3、1/4、1/5、1/6 Duty 及 1/3 Bias 选择
  支持 R Type 驱动方式
  内建升压稳压线路，提供 4 段 VLCD 偏压 3.3V, 3.0V, 2.8V, or 2.6V 可透过校正函数提供 5 段 VLCD 偏压
- 多个可编程复用型 I/O：
  数个通用型数字输出入端口
  数个可选择 LCD 端口或数字输出入端口

模拟功能

- 模拟工作电压为 2.4V to 3.6V
- 内建低噪声 24-bit Σ ADC：
  ADC 支持 x1~ x8 信号放大，内建仪表放大器 IA, x4~ x32 信号放大,最大输入放大倍率高达 256
  输入参考信号可解析至 0.1uVrms(Gain=256)
  最高转换率可达 15Ksps
- 外部高速振荡器频率达 16MHz
- 外部低速振荡器 32768Hz
- 内建 RC 高速振荡器频率高达 16MHz
- 内建 RC 低速振荡器频率低至 35KHz
- 电源模块：
  内建四段可调整稳压电源(VDDA)
  1.2V 带隙参考电压(REFO)
- 轨对轨运算放大器 OPAMP：
  CMOS 输入, 1MHz 增益带宽
  可设计为比较器
- 12-BIT 可编程数位电阻器：
  可编程电阻分压计
  电阻保证单调性
  搭配 OPAMP 可设计为 12-BIT DAC
- 低电压比较器：
  低电压检测电路
  支持外部电压输入比较

Part No.	24-b ΣΔADC	Flash (byte)	SRAM (byte)	R2R OPAMP	DAC	Temp. Sensor	RTC	I/O	PWM	Serial Interface	LCD	ISP Mode	Pin
HY16F3981-L064	(7+2)-CH	64K	8K	1	12bits	Y	1	16+36	4-CH	2*UART 32bits SPI I2C	4x32 6x30	Y	LQFP64
HY16F3981-E028	(7+2)-CH	64K	8K	1	12bits	Y	1	17	4-CH	2*UART 32bits SPI I2C	-	Y	SSOP28

2. 管脚名称定义

2.1 HY16F3981 系列管脚图

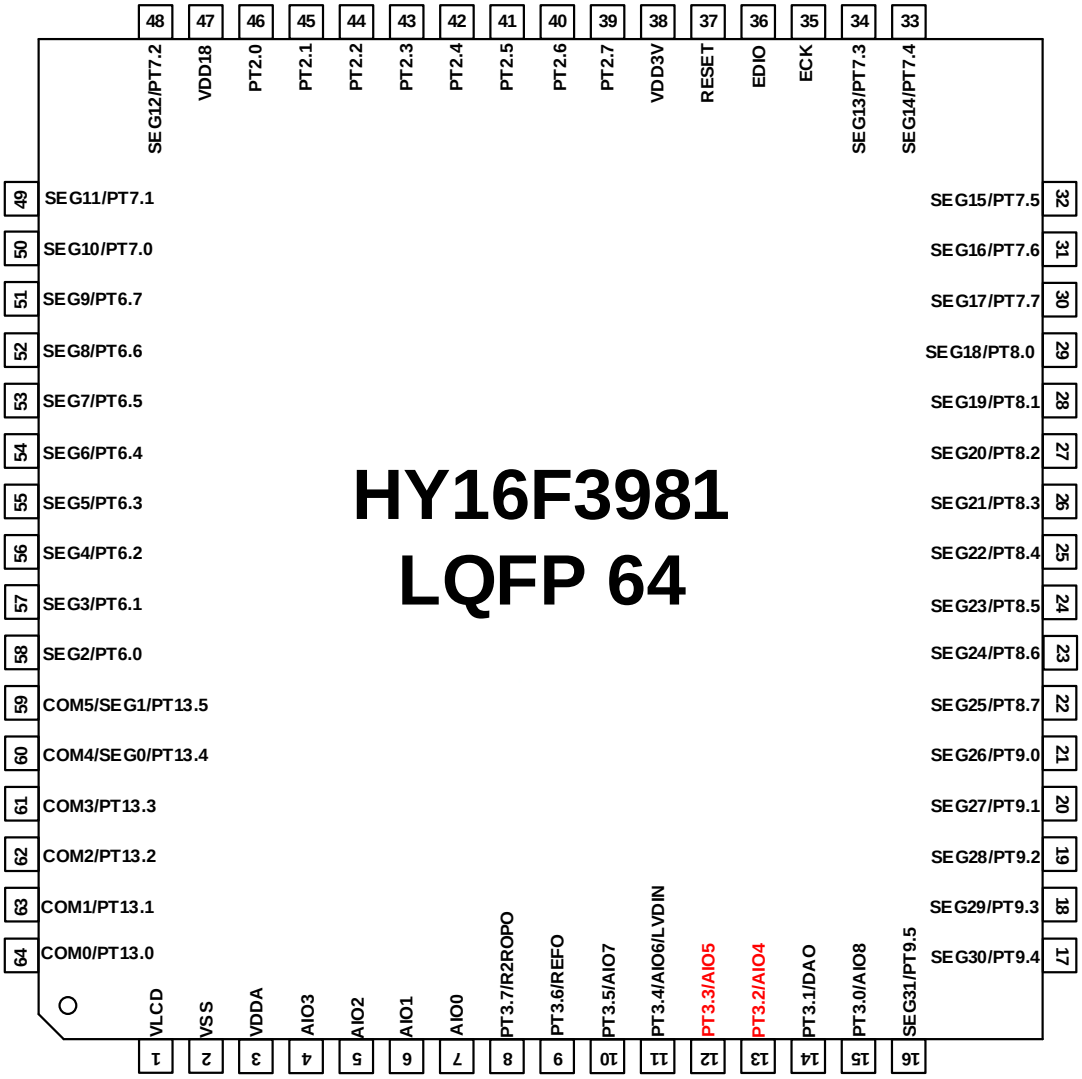


图 2-1-1 HY16F3981 LQFP64 管脚图

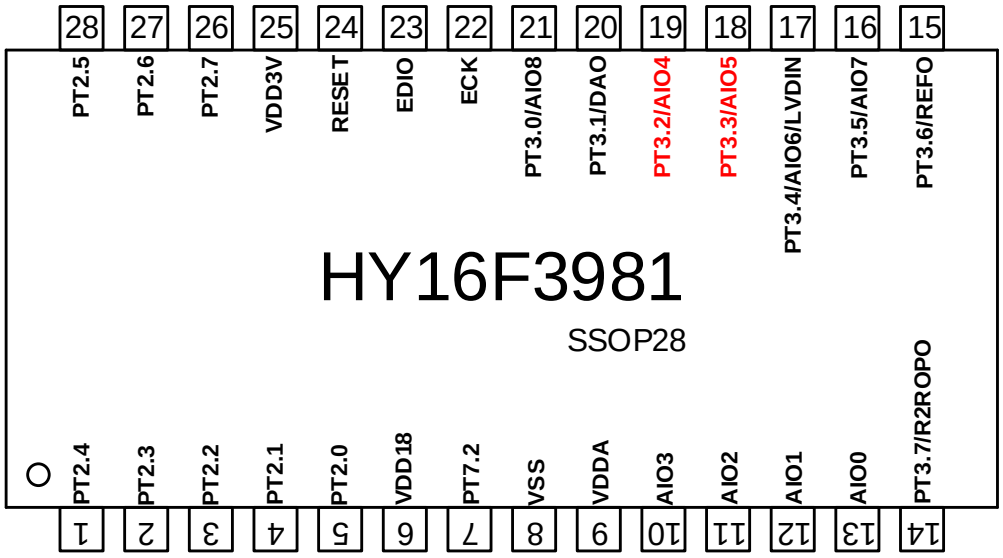


图 2-1-2 HY16F3981 SSOP28 管脚图

2.2 引脚功能描述

2.2.1 HY16F3981 引脚定义

类型定义：I = 数字输入;O = 数字输出;OD = 开漏输出;AI = 模拟输入;AO = 模拟输出;P = 电源连接端.

引脚	HY16F3981-L064	HY16F3981-E028	类型	名称	描述
VLCD	1	-	PIO	VLCD	LCD 稳压电源输出/LCD 电源输入, 10uF Cap to VSS.
VSS	2	8	PI	VSS	接地端引脚
VDDA	3	9	PIO	VDDA	模拟电源电压/LDO 稳压输出端/模拟电源电压输入端 1uF~10uF Cap to VSS.
AIO3	4	10	AI	AIO3	ADC 模拟输入引脚 AIO3
AIO2	5	11	AI	AIO2	ADC 模拟输入引脚 AIO2
AIO1	6	12	AI	AIO1	ADC 模拟输入引脚 AIO1
AIO0	7	13	AI	AIO0	ADC 模拟输入引脚 AIO0
PT3.7	8	14	IO AO I	PT3.7 R2ROPO INT3.7	通用数字输入/输出引脚 Rail-to-rail 运算放大器模拟输出引脚 R2ROPO 外部中断源 INT3.7 输入引脚
PT3.6	9	15	IO PIO I	PT3.6 REFO INT3.6	通用数字输入/输出引脚 模拟参考电压 1.2V 输出引脚, 0.1uF Cap to VSS. 外部中断源 INT3.6 输入引脚
PT3.5	10	16	IO AI I	PT3.5 AIO7 INT3.5	通用数字输入/输出引脚 ADC 模拟输入引脚 AIO7 外部中断源 INT3.5 输入引脚
PT3.4	11	17	IO AI I AI	PT3.4 AIO6 INT3.4 LVDIN	通用数字输入/输出引脚 ADC 模拟输入引脚 AIO6 外部中断源 INT3.4 输入引脚 低电压比较器外部输入引脚 LVDIN
PT3.3	12	18	IO AI I	PT3.3 AIO5 INT3.3	通用数字输入/输出引脚 ADC 模拟输入引脚 AIO5 外部中断源 INT3.3 输入引脚
PT3.2	13	19	IO AI I	PT3.2 AIO4 INT3.2	通用数字输入/输出引脚 ADC 模拟输入引脚 AIO4 外部中断源 INT3.2 输入引脚
PT3.1	14	20	IO DO AO I	PT3.1 OPO2 DAO INT3.1	通用数字输入/输出引脚 运算放大器数字输出引脚 OPO2 12-BIT Resistance Ladders 输出引脚 外部中断源 INT3.1 输入引脚

引脚	HY16F3981-L064	HY16F3981-E028	类型	名称	描述
PT3.0	15	21	IO	PT3.0	通用数字输入/输出引脚
			DO	OPO1	运算放大器数字输出引脚 OPO1
			AI	AIO8	模拟输入引脚 AIO8
			I	INT3.0	外部中断源 INT3.0 输入引脚
SEG31	16	-	IO	PT9.5	通用数字输入/输出引脚
			AO	SEG31	LCD Segment 输出
			O	PWM1_8	TimerB, PWM1_8 输出引脚
			I	RX_8	EUART 通信接收引脚 RX_8
SEG30	17	-	IO	PT9.4	通用数字输入/输出引脚
			AO	SEG30	LCD Segment 输出
			O	PWM0_8	TimerB, PWM0_8 输出引脚
			O	TX_8	EUART 通信发送引脚 TX_8
SEG29	18	-	IO	PT9.3	通用数字输入/输出引脚
			AO	SEG29	LCD Segment 输出
			O	PWM3_7	TimerB2, PWM3_7 输出引脚
			O	MOSI_7	SPI 通信数据引脚 MOSI_7(主机输出，从机输入)
			I	RX2_7	EUART2 通信接收引脚 RX2_7
SEG28	19	-	IO	PT9.2	通用数字输入/输出引脚
			AO	SEG28	LCD Segment 输出
			O	PWM2_7	TimerB2, PWM2_7 输出引脚
			O	MISO_7	SPI 通信数据引脚 MISO_7(主机输入，从机输出)
			O	TX2_7	EUART2 通信发送引脚 TX2_7
SEG27	20	-	IO	PT9.1	通用数字输入/输出引脚
			AO	SEG27	LCD Segment 输出
			O	PWM1_7	TimerB, PWM1_7 输出引脚
			O	CK_7	SPI 通信时钟引脚 CK_7
			I	RX_7	EUART 通信接收引脚 RX_7
SEG26	21	-	IO	PT9.0	通用数字输入/输出引脚
			AO	SEG26	LCD Segment 输出
			O	PWM0_7	TimerB, PWM0_7 输出引脚
			O	CS_7	SPI 通信使能引脚 CS_7
			O	TX_7	EUART 通信发送引脚 TX_7

引脚	HY16F3981-L064	HY16F3981-E028	类型	名称	描述
SEG25	22	-	IO	PT8.7	通用数字输入/输出引脚
			AO	SEG25	LCD Segment 输出
			O	PWM3_6	TimerB2, PWM3_6 输出引脚
			O	MOSI_6	SPI 通信数据引脚 MOSI_6(主机输出，从机输入)
			I	RX2_6	EUART2 通信接收引脚 RX2_6
			I	TCI3_8	TimerB2 输入源引脚 TCI3_8
SEG24	23	-	IO	PT8.6	通用数字输入/输出引脚
			AO	SEG24	LCD Segment 输出
			O	PWM2_6	TimerB2, PWM2_6 输出引脚
			O	MISO_6	SPI 通信数据引脚 MISO_6(主机输入，从机输出)
			O	TX2_6	EUART2 通信发送引脚 TX2_6
SEG23	24	-	IO	PT8.5	通用数字输入/输出引脚
			AO	SEG23	LCD Segment 输出
			O	PWM1_6	TimerB, PWM1_6 输出引脚
			O	CK_6	SPI 通信时钟引脚 CK_6
			I	RX_6	EUART 通信接收引脚 RX_6
			I	TCI3_7	TimerB2 输入源引脚 TCI3_7
SEG22	25	-	IO	PT8.4	通用数字输入/输出引脚
			AO	SEG22	LCD Segment 输出
			O	PWM0_6	TimerB, PWM0_6 输出引脚
			O	CS_6	SPI 通信使能引脚 CS_6
			O	TX_6	EUART 通信发送引脚 TX_6
SEG21	26	-	IO	PT8.3	通用数字输入/输出引脚
			AO	SEG21	LCD Segment 输出
			O	PWM3_5	TimerB2, PWM3_5 输出引脚
			O	MOSI_5	SPI 通信数据引脚 MOSI_5(主机输出，从机输入)
			I	RX2_5	EUART2 通信接收引脚 RX2_5
			I	TCI3_6	TimerB2 输入源引脚 TCI3_6
SEG20	27	-	IO	PT8.2	通用数字输入/输出引脚
			AO	SEG20	LCD Segment 输出
			O	PWM2_5	TimerB2, PWM2_5 输出引脚
			O	MISO_5	SPI 通信数据引脚 MISO_5(主机输入，从机输出)
			O	TX2_5	EUART2 通信发送引脚 TX2_5

引脚	HY16F3981-L064	HY16F3981-E028	类型	名称	描述
SEG19	28		IO	PT8.1	通用数字输入/输出引脚
			AO	SEG19	LCD Segment 输出
			O	PWM1_5	TimerB, PWM1_5 输出引脚
			O	CK_5	SPI 通信时钟引脚 CK_5
			I	RX_5	EUART 通信接收引脚 RX_5
			I	TCI3_5	TimerB2 输入源引脚 TCI3_5
SEG18	29		IO	PT8.0	通用数字输入/输出引脚
			AO	SEG18	LCD Segment 输出
			O	PWM0_5	TimerB, PWM0_5 输出引脚
			O	CS_5	SPI 通信使能引脚 CS_5
			O	TX_5	EUART 通信发送引脚 TX_5
SEG17	30		IO	PT7.7	通用数字输入/输出引脚
			AO	SEG17	LCD Segment 输出
			I	TCI3_4	TimerB2 输入源引脚 TCI3_4
SEG16	31		IO	PT7.6	通用数字输入/输出引脚
			AO	SEG16	LCD Segment 输出
SEG15	32		IO	PT7.5	通用数字输入/输出引脚
			AO	SEG15	LCD Segment 输出
			I	TCI3_3	TimerB2 输入源引脚 TCI3_3
SEG14	33		IO	PT7.4	通用数字输入/输出引脚
			AO	SEG14	LCD Segment 输出
SEG13	34		IO	PT7.3	通用数字输入/输出引脚
			AO	SEG13	LCD Segment 输出
			I	TCI3_2	TimerB2 输入源引脚 TCI3_2
ECK	35	22	DIO	ECK	开发调试通信口(EDM)时钟引脚, 100K Resistance to VSS.
EDIO	36	23	DIO	EDIO	开发调试通信口(EDM)数据输入/输出引脚, 100K Resistance to VSS.
RESET	37	24	DI	RESET	复位引脚(低电位有效), 100K Resistance to VDD3V, 100nF Cap to VSS.
VDD3V	38	25	PI	VDD3V	芯片工作电源电压输入引脚, 10uF Cap to VSS.

引脚	HY16F3981-L064	HY16F3981-E028	类型	名称	描述
PT2.7	39	26	IO	PT2.7	通用数字输入/输出引脚
			XO	HS_XOUT	外部高速晶振 2~16MHZ 输出引脚
			I	INT2.7	外部中断源 INT2.7 输入引脚
			O	PWM3_4	TimerB2, PWM3_4 输出引脚
			O	MOSI_4	SPI 通信数据引脚 MOSI_4(主机输出，从机输入)
			I	RX2_4	EUART2 通信接收引脚 RX2_4
			I	TCI2_8	捕捉比较器输入源引脚 TCI2_8
			IO	SDA_8	I2C 通信数据引脚 SDA_8
PT2.6	40	27	IO	PT2.6	通用数字输入/输出引脚
			XI	HS_XIN	外部高速晶振 2~16MHZ 输入引脚
			I	INT2.6	外部中断源 INT2.6 输入引脚
			O	PWM2_4	TimerB2, PWM2_4 输出引脚
			I	MISO_4	SPI 通信数据引脚 MISO_4(主机输入，从机输出)
			O	TX2_4	EUART2 通信发送引脚 TX2_4
			I	TCI1_8	捕捉比较器输入源引脚 TCI1_8
			IO	SCL_8	I2C 通信时钟引脚 SCL_8
PT2.5	41	28	IO	PT2.5	通用数字输入/输出引脚
			XI	LS_XIN	外部低速晶振 32768HZ 输入引脚
			I	INT2.5	外部中断源 INT2.5 输入引脚
			O	PWM1_4	TimerB, PWM1_4 输出引脚
			I	CK_4	SPI 通信时钟引脚 CK_4
			I	RX_4	EUART 通信接收引脚 RX_4
			I	TCI2_7	捕捉比较器输入源引脚 TCI2_7
			IO	SDA_7	I2C 通信数据引脚 SDA_7
PT2.4	42	1	IO	PT2.4	通用数字输入/输出引脚
			XO	LS_XOUT	外部低速晶振 32768HZ 输出引脚
			I	INT2.4	外部中断源 INT2.4 输入引脚
			O	PWM0_4	TimerB, PWM0_4 输出引脚
			I	CS_4	SPI 通信使能引脚 CS_4
			O	TX_4	EUART 通信发送引脚 TX_4
			I	TCI1_7	捕捉比较器输入源引脚 TCI1_7
			IO	SCL_7	I2C 通信时钟引脚 SCL_7

引脚	HY16F3981-L064	HY16F3981-E028	类型	名称	描述
PT2.3	43	2	IO	PT2.3	通用数字输入/输出引脚
			I	INT2.3	外部中断源 INT2.3 输入引脚
			O	PWM3_3	TimerB2, PWM3_3 输出引脚
			O	MOSI_3	SPI 通信数据引脚 MOSI_3(主机输出，从机输入)
			I	RX2_3	EUART2 通信接收引脚 RX2_3
			I	TCI2_6	捕捉比较器输入源引脚 TCI2_6
			IO	SDA_6	I2C 通信数据引脚 SDA_6
PT2.2	44	3	IO	PT2.2	通用数字输入/输出引脚
			I	INT2.2	外部中断源 INT2.2 输入引脚
			O	PWM2_3	TimerB2, PWM2_3 输出引脚
			I	MISO_3	SPI 通信数据引脚 MISO_3(主机输入，从机输出)
			O	TX2_3	EUART2 通信发送引脚 TX2_3
			I	TCI1_6	捕捉比较器输入源引脚 TCI1_6
			IO	SCL_6	I2C 通信时钟引脚 SCL_6
PT2.1	45	4	IO	PT2.1	通用数字输入/输出引脚
			I	INT2.1	外部中断源 INT2.1 输入引脚
			O	PWM1_3	TimerB, PWM1_3 输出引脚
			I	CK_3	SPI 通信时钟引脚 CK_3
			I	RX_3	EUART 通信接收引脚 RX_3
			I	TCI2_5	捕捉比较器输入源引脚 TCI2_5
			IO	SDA_5	I2C 通信数据引脚 SDA_5
PT2.0	46	5	IO	PT2.0	通用数字输入/输出引脚
			I	INT2.0	外部中断源 INT2.0 输入引脚
			O	PWM0_3	TimerB, PWM0_3 输出引脚
			I	CS_3	SPI 通信使能引脚 CS_3
			O	TX_3	EUART 通信发送引脚 TX_3
			I	TCI1_5	捕捉比较器输入源引脚 TCI1_5
			IO	SCL_5	I2C 通信时钟引脚 SCL_5
VDD18	47	6	PI	VDD18	数字电源电压引脚，输出 1.8V, 1uF Cap to VSS
SEG12	48	7	IO	PT7.2	通用数字输入/输出引脚
			AO	SEG12	LCD Segment 输出
SEG11	49	-	IO	PT7.1	通用数字输入/输出引脚
			AO	SEG11	LCD Segment 输出
			I	TCI3_1	TimerB2 输入源引脚 TCI3_1
SEG10	50	-	IO	PT7.0	通用数字输入/输出引脚
			AO	SEG10	LCD Segment 输出

引脚	HY16F3981-L064	HY16F3981-E028	类型	名称	描述
SEG9	51	-	IO AO	PT6.7 SEG9	通用数字输入/输出引脚 LCD Segment 输出
SEG8	52	-	IO AO	PT6.6 SEG8	通用数字输入/输出引脚 LCD Segment 输出
SEG7	53	-	IO AO	PT6.5 SEG7	通用数字输入/输出引脚 LCD Segment 输出
SEG6	54	-	IO AO	PT6.4 SEG6	通用数字输入/输出引脚 LCD Segment 输出
SEG5	55	-	IO AO	PT6.3 SEG5	通用数字输入/输出引脚 LCD Segment 输出
SEG4	56	-	IO AO	PT6.2 SEG4	通用数字输入/输出引脚 LCD Segment 输出
SEG3	57	-	IO AO	PT6.1 SEG3	通用数字输入/输出引脚 LCD Segment 输出
SEG2	58	-	IO AO	PT6.0 SEG2	通用数字输入/输出引脚 LCD Segment 输出
SEG1	59		IO AO AO	PT13.5 SEG1 COM5	通用数字输入/输出引脚 LCD Segment 输出 LCD Common 输出
SEG0	60		IO AO AO	PT13.4 SEG0 COM4	通用数字输入/输出引脚 LCD Segment 输出 LCD Common 输出
COM3	61		IO AO	PT13.3 COM3	通用数字输入/输出引脚 LCD Common 输出
COM2	62		IO AO	PT13.2 COM2	通用数字输入/输出引脚 LCD Common 输出
COM1	63		IO AO	PT13.1 COM1	通用数字输入/输出引脚 LCD Common 输出
COM0	64		IO AO	PT13.0 COM0	通用数字输入/输出引脚 LCD Common 输出

表2-1 HY16F3981 管脚定义及管脚功能描述

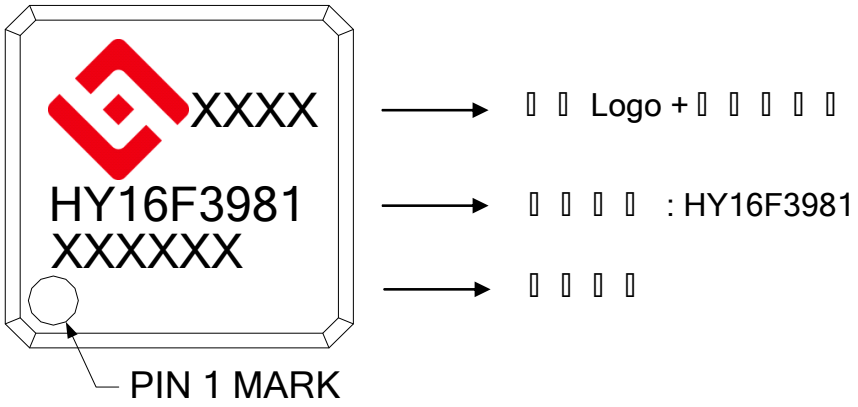
2.2.2 管脚复用功能及复用功能优先级别

Function	INT	Timer C Capture	Special Function	SPI	I2C	UART 1/2	AIP	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	0	1	2	3	4	5	6
PT2.0	INT2.0	TCI1_5		CS_3	SCL_5	Tx_3			PWM0_3
PT2.1	INT2.1	TCI2_5		CK_3	SDA_5	Rx_3			PWM1_3
PT2.2	INT2.2	TCI1_6		MISO_3	SCL_6	Tx2_3			PWM2_3
PT2.3	INT2.3	TCI2_6		MOSI_3	SDA_6	Rx2_3			PWM3_3
PT2.4	INT2.4	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4			PWM0_4
PT2.5	INT2.5	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4			PWM1_4
PT2.6	INT2.6	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4			PWM2_4
PT2.7	INT2.7	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4			PWM3_4
PT3.0	INT3.0						OPO1	AIO8	
PT3.1	INT3.1						OPO2	DAO	
PT3.2	INT3.2							AIO4	
PT3.3	INT3.3							AIO5	
PT3.4	INT3.4							AIO6/LVDIN	
PT3.5	INT3.5							AIO7	
PT3.6	INT3.6							REFO	
PT3.7	INT3.7							R2ROPO	
RESET	RESET								
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	
PT13.0			COM 0						
PT13.1			COM 1						
PT13.2			COM 2						
PT13.3			COM 3						
PT13.4			COM 4/SEG 0						
PT13.5			COM 5/SEG 1						
PT6.0			SEG 2						
PT6.1			SEG 3						

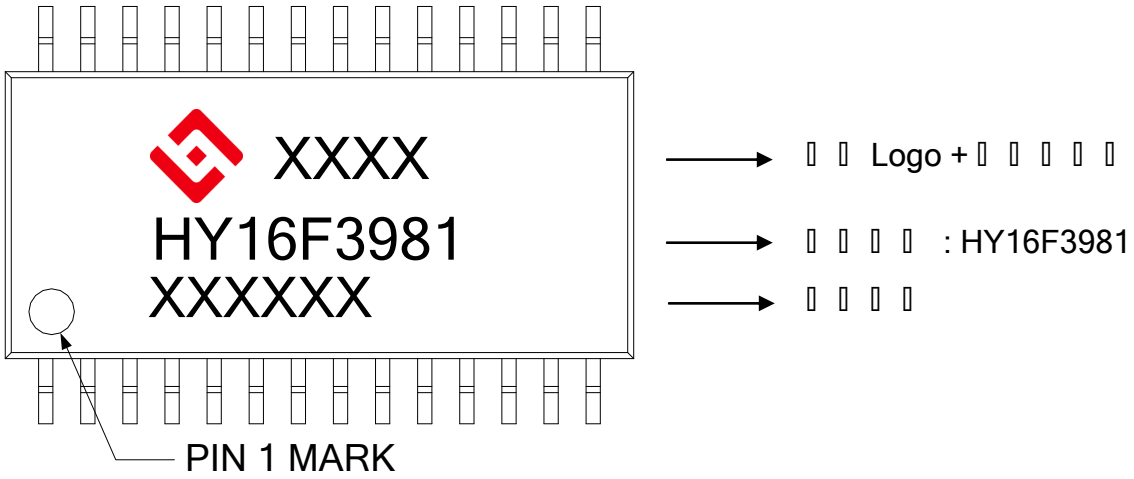
PT6.2			SEG 4						
PT6.3			SEG 5						
PT6.4			SEG 6						
PT6.5			SEG 7						
PT6.6			SEG 8						
PT6.7			SEG 9						
PT7.0			SEG 10						
PT7.1		TCI3_1	SEG 11						
PT7.2			SEG 12						
PT7.3		TCI3_2	SEG 13						
PT7.4			SEG 14						
PT7.5		TCI3_3	SEG 15						
PT7.6			SEG 16						
PT7.7		TCI3_4	SEG 17						
PT8.0			SEG 18	CS_5		Tx_5			PWM0_5
PT8.1		TCI3_5	SEG 19	CK_5		Rx_5			PWM1_5
PT8.2			SEG 20	MISO_5		Tx2_5			PWM2_5
PT8.3		TCI3_6	SEG 21	MOSI_5		Rx2_5			PWM3_5
PT8.4			SEG 22	CS_6		Tx_6			PWM0_6
PT8.5		TCI3_7	SEG 23	CK_6		Rx_6			PWM1_6
PT8.6			SEG 24	MISO_6		Tx2_6			PWM2_6
PT8.7		TCI3_8	SEG 25	MOSI_6		Rx2_6			PWM3_6
PT9.0			SEG 26	CS_7		Tx_7			PWM0_7
PT9.1			SEG 27	CK_7		Rx_7			PWM1_7
PT9.2			SEG 28	MISO_7		Tx2_7			PWM2_7
PT9.3			SEG 29	MOSI_7		Rx2_7			PWM3_7
PT9.4			SEG 30			Tx_8			PWM0_8
PT9.5			SEG 31			Rx_8			PWM1_8

2.3 封装片丝印信息

2.3.1 LQFP 封装片丝印信息



2.3.2 SSOP28 封装片丝印信息



3. 应用电路

3.1 红外线感测应用电路(LQFP64 支持 LCD)

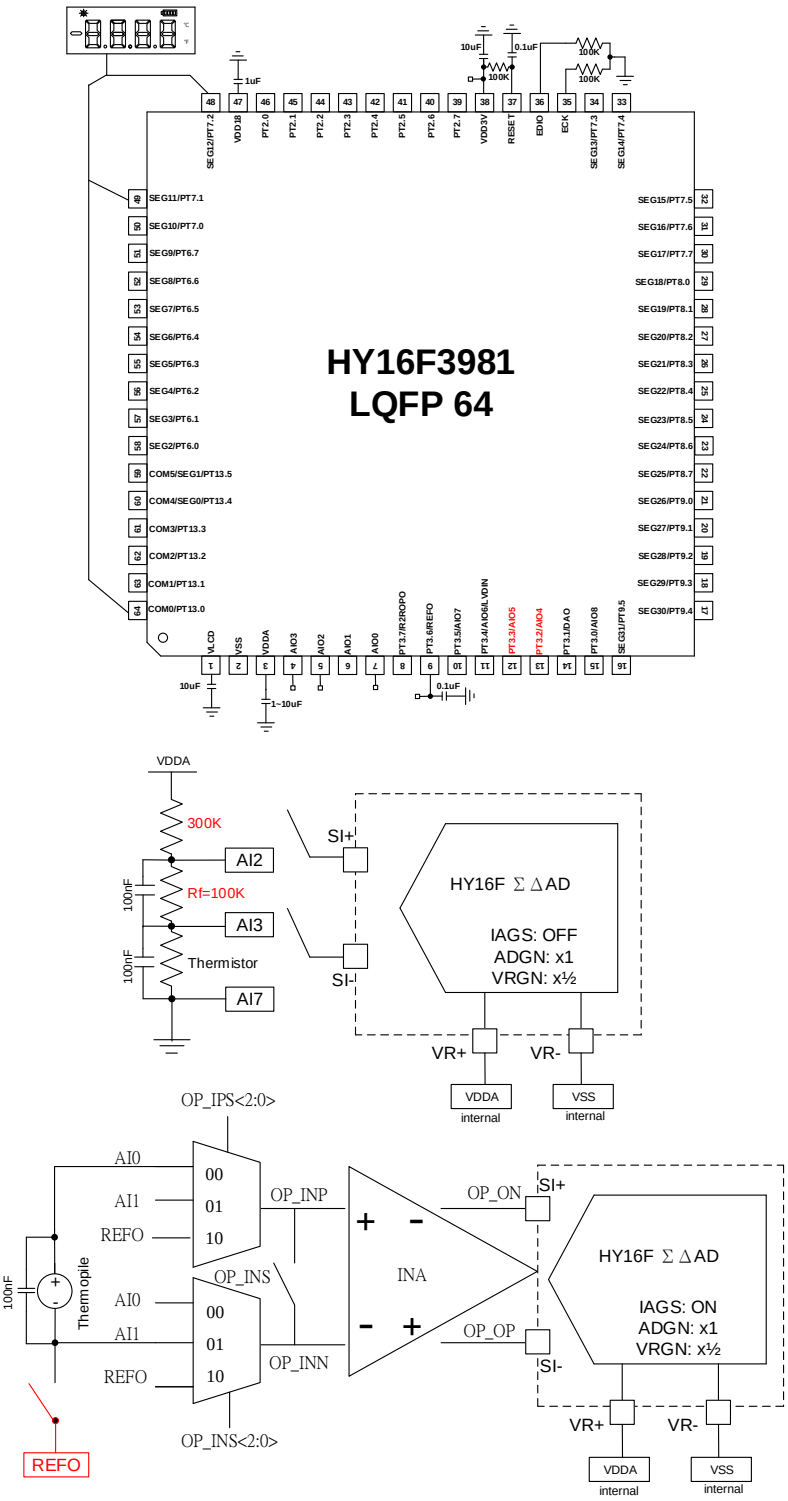


图3-1 红外线感测应用电路(LQFP64支持LCD)

3.2 红外线感测应用电路(SSOP28 无支持 LCD)

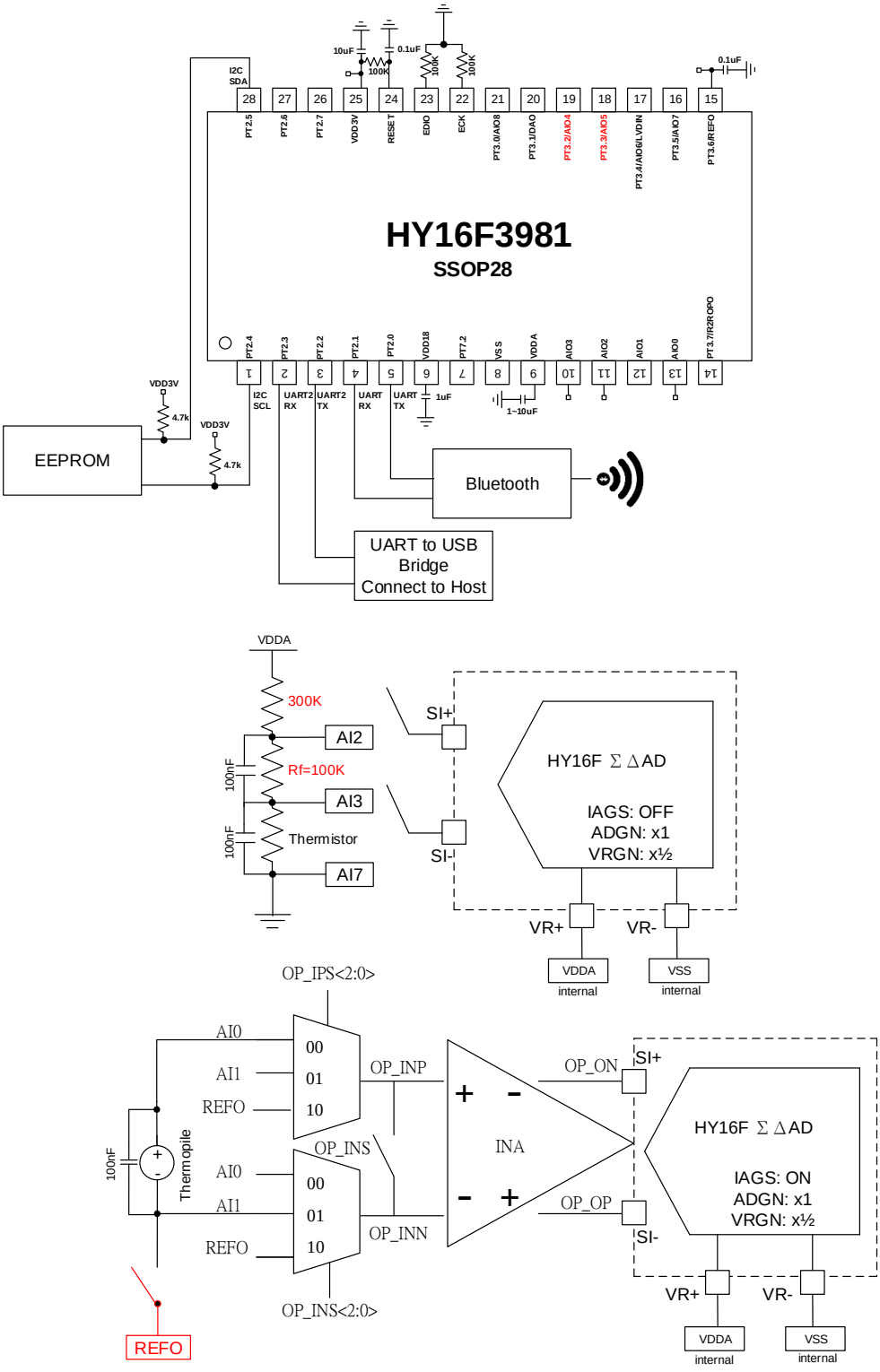


图3-2 红外线感测应用电路(SSOP28无支持LCD)

3.3 血压计传感器应用电路(LQFP64 支持 LCD)

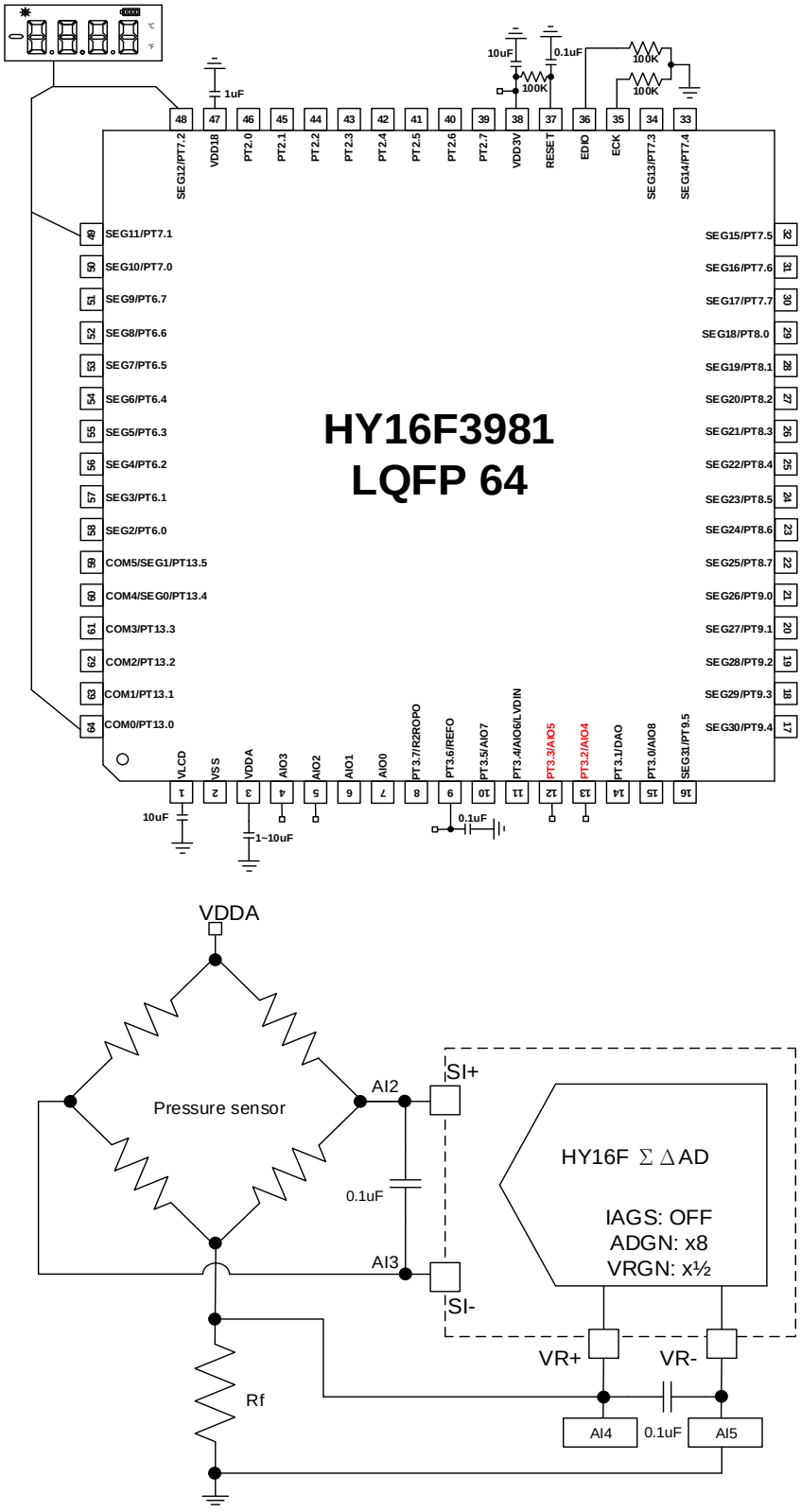


图 3-3 血压计传感器应用电路(LQFP64支持LCD)

3.4 血压计传感器应用电路(SSOP28 无支持 LCD)

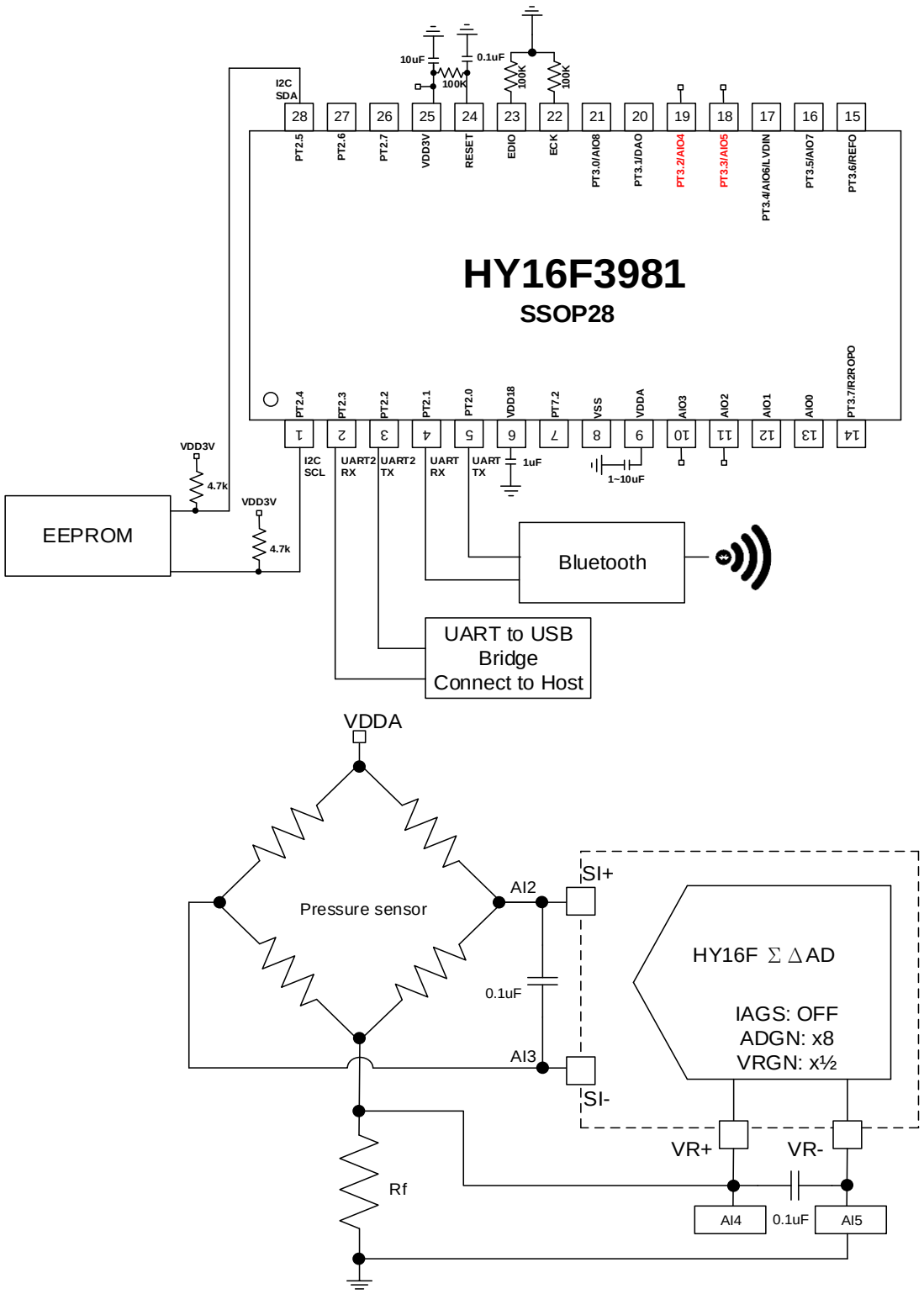


图 3-4 血压计传感器应用电路(SSOP28无支持LCD)

4. 功能概述

4.1 内部框图

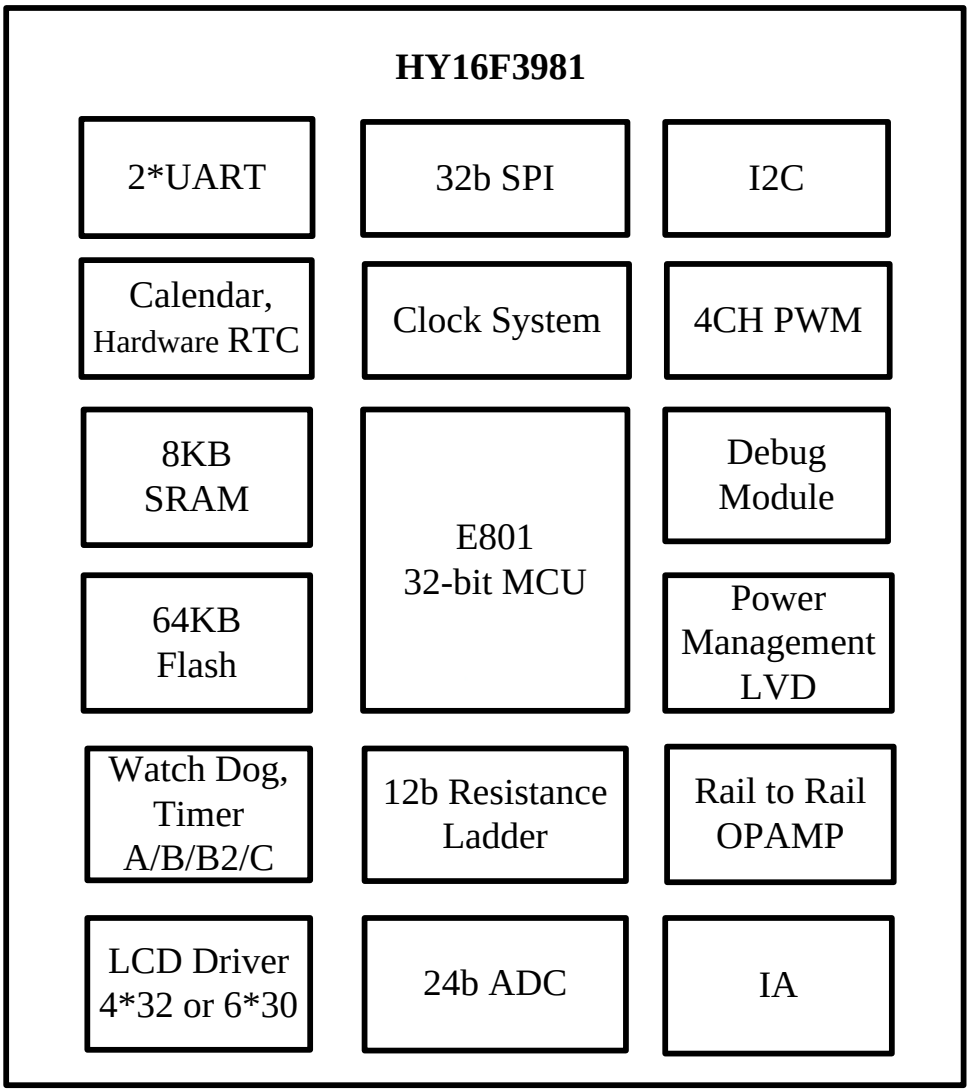


图 4-1 HY16F3981 内部框图

4.2 中央处理器核心方框图

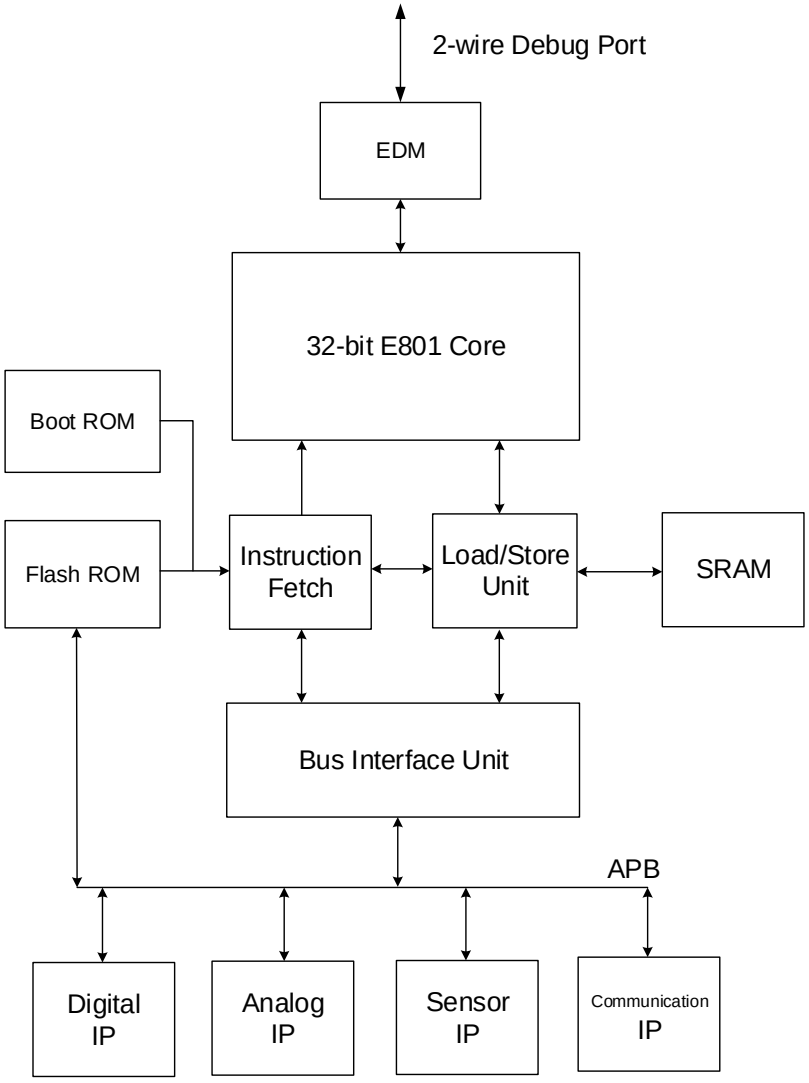
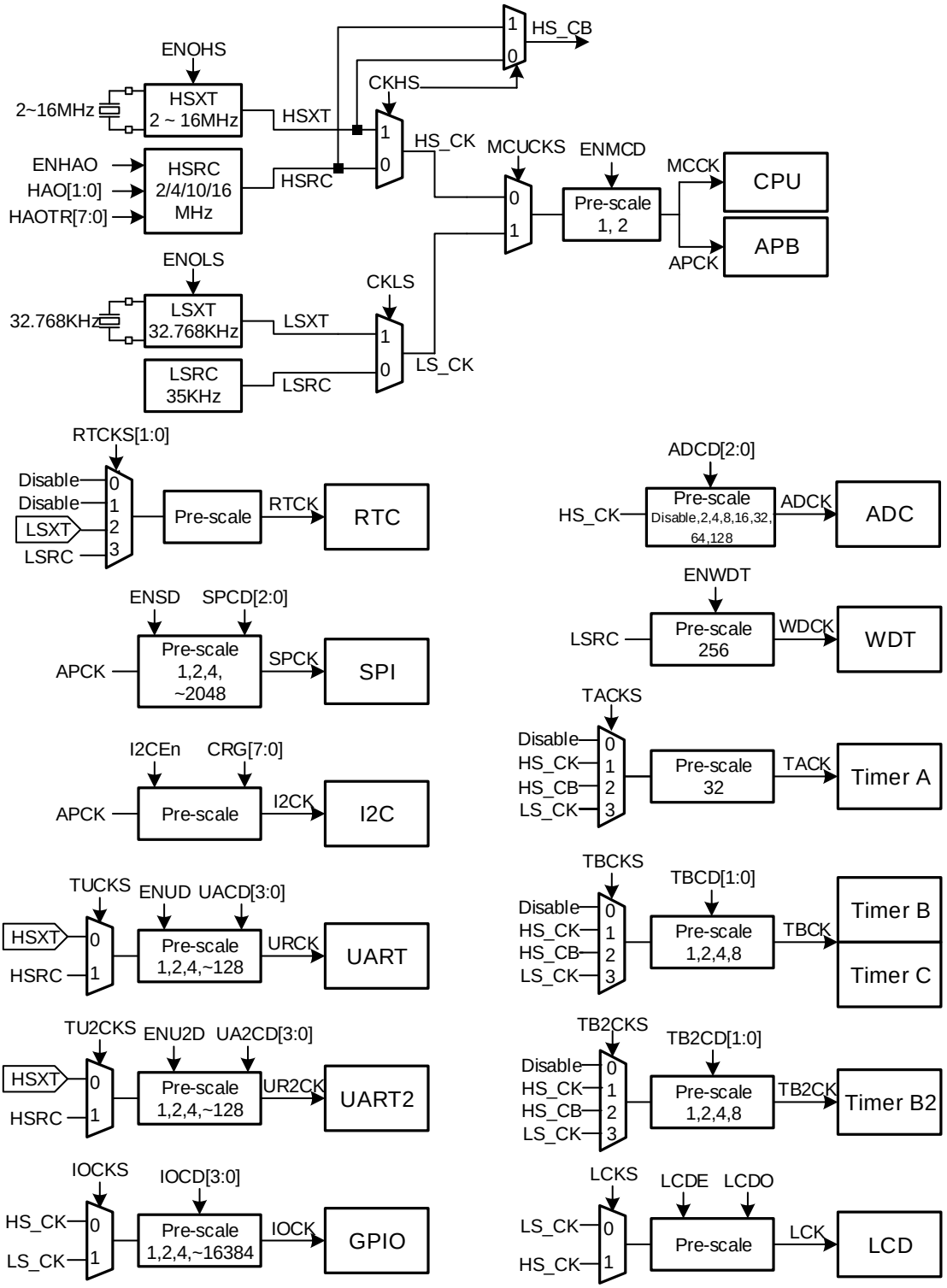


Figure 4-2 中央处理器核心方框图

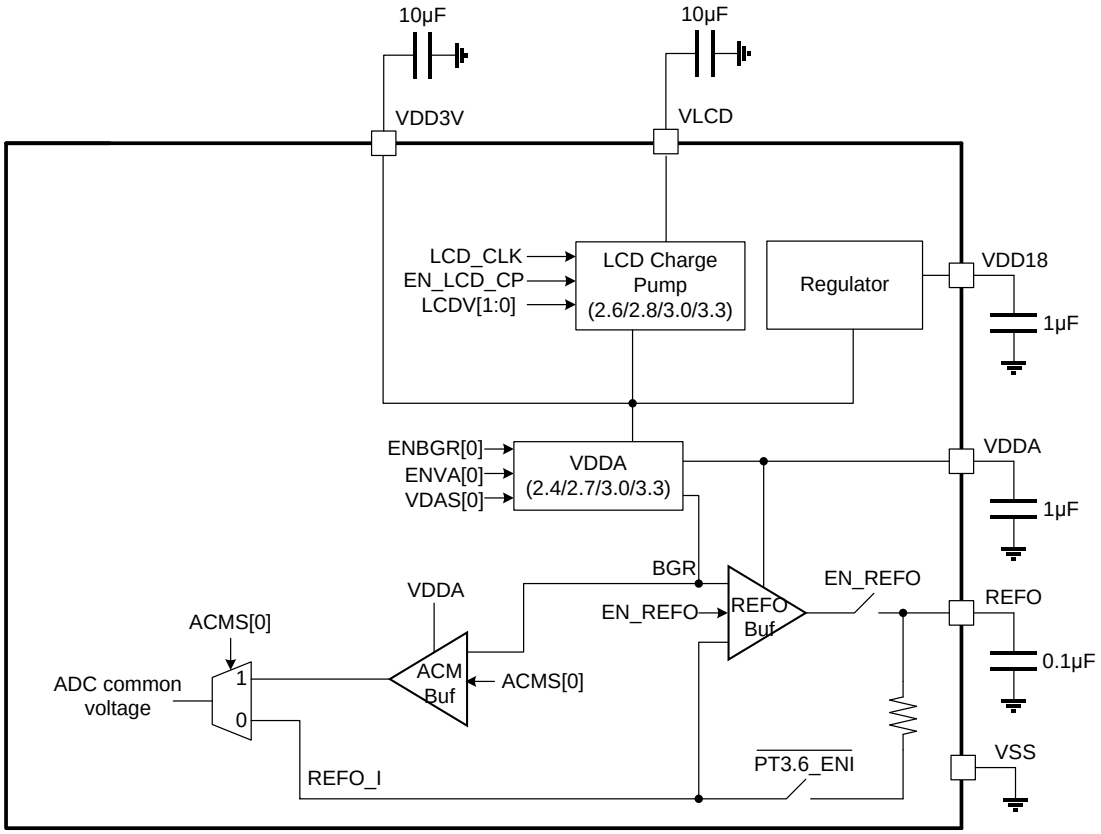
4.3 相关的支持文档

文件名	描述
UG-HY16F3981	HY16F3981 系列用户手册
APD-HY16IDE022	HY16F3981 C 函数库手册
APD-HY16IDE023	HY16F3981 各 IP 使用说明书
APD-HY16IDE001	HY16F 系列 IDE 软件使用说明书/ HY16F Series Device 安装程序
APD-HY16IDE009	HY16F 系列 ICE 硬件使用说明书
APD-HY16IDE006	HY16F 系列烧录器使用说明书

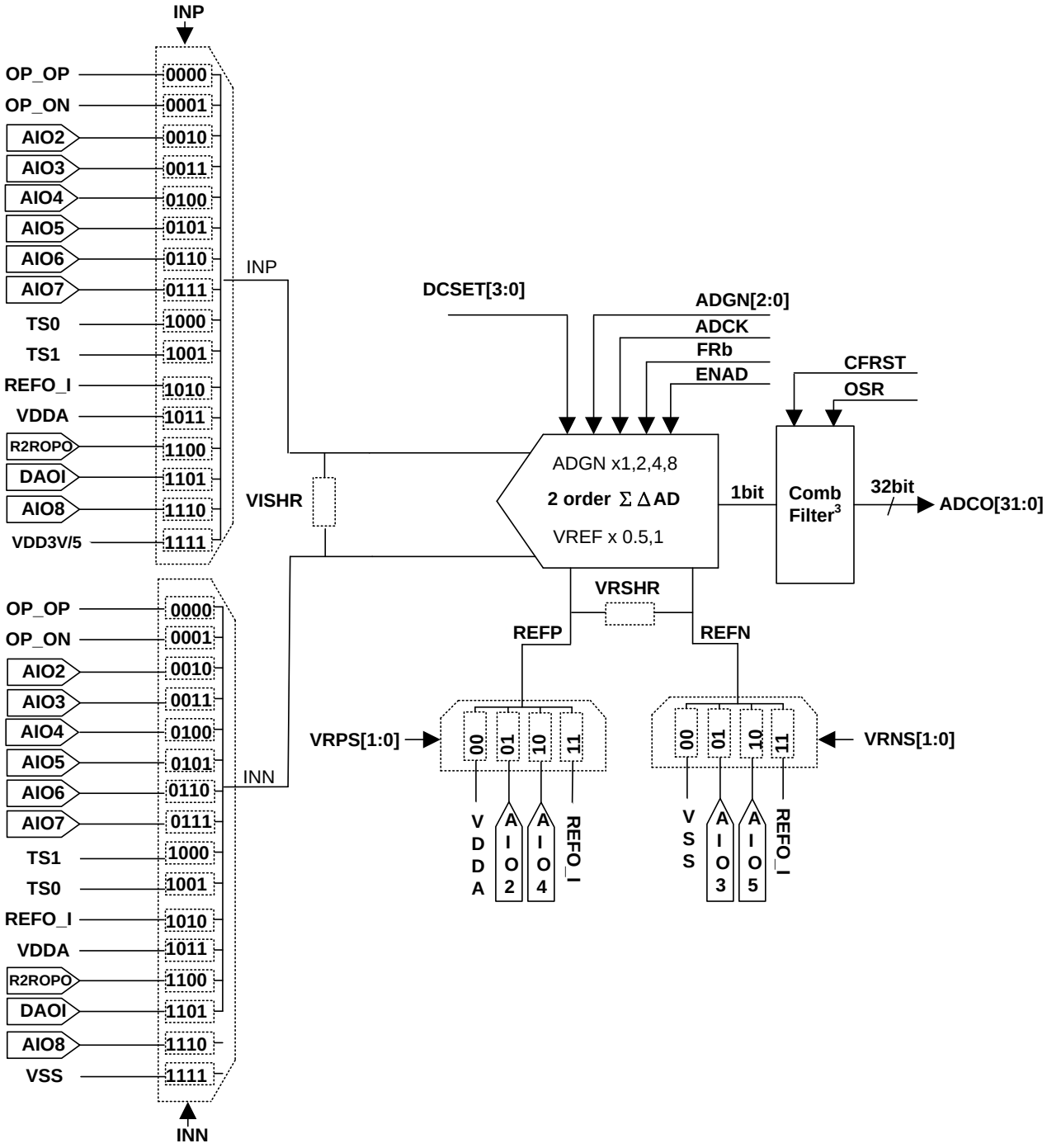
4.4 时钟系统网络


HS_CB
ENOHS
CKHS
2~16MHz
HSXT
2 ~ 16MHz
HSXT
HS_CK
MCUCKS
ENMCD
MCCK
CPU
ENHAO
HAO[1:0]
HAOTR[7:0]
HSRC
2/4/10/16
MHz
HSRC
Pre-scale
1, 2
APB
APCK
ENOLS
CKLS
32.768KHz
LSXT
32.768KHz
LSXT
LS_CK
LSRC
35KHz
LSRC
RTCKS[1:0]
Disable
Disable
LSXT
LSRC
Pre-scale
RTCK
RTC
ADCD[2:0]
HS_CK
Pre-scale
Disable,2,4,8,16,32,
64,128
ADCK
ADC
ENWDT
LSRC
Pre-scale
256
WDCK
WDT
ENSD
SPCD[2:0]
APCK
Pre-scale
1,2,4,
~2048
SPCK
SPI
TACKS
Disable
HS_CK
HS_CB
LS_CK
Pre-scale
32
TACK
Timer A
I2CEn
CRG[7:0]
APCK
Pre-scale
I2CK
I2C
TBCKS
TBCD[1:0]
Disable
HS_CK
HS_CB
LS_CK
Pre-scale
1,2,4,8
TBCK
Timer B
Timer C
TUCKS
ENUD
UACD[3:0]
HSXT
HSRC
Pre-scale
1,2,4,~128
URCK
UART
TB2CKS
TB2CD[1:0]
Disable
HS_CK
HS_CB
LS_CK
Pre-scale
1,2,4,8
TB2CK
Timer B2
TU2CKS
ENU2D
UA2CD[3:0]
HSXT
HSRC
Pre-scale
1,2,4,~128
UR2CK
UART2
IOCKS
IOCD[3:0]
HS_CK
LS_CK
Pre-scale
1,2,4,~16384
IOCK
GPIO
LCKS
LCDE
LCDO
LS_CK
HS_CK
Pre-scale
LCK
LCD

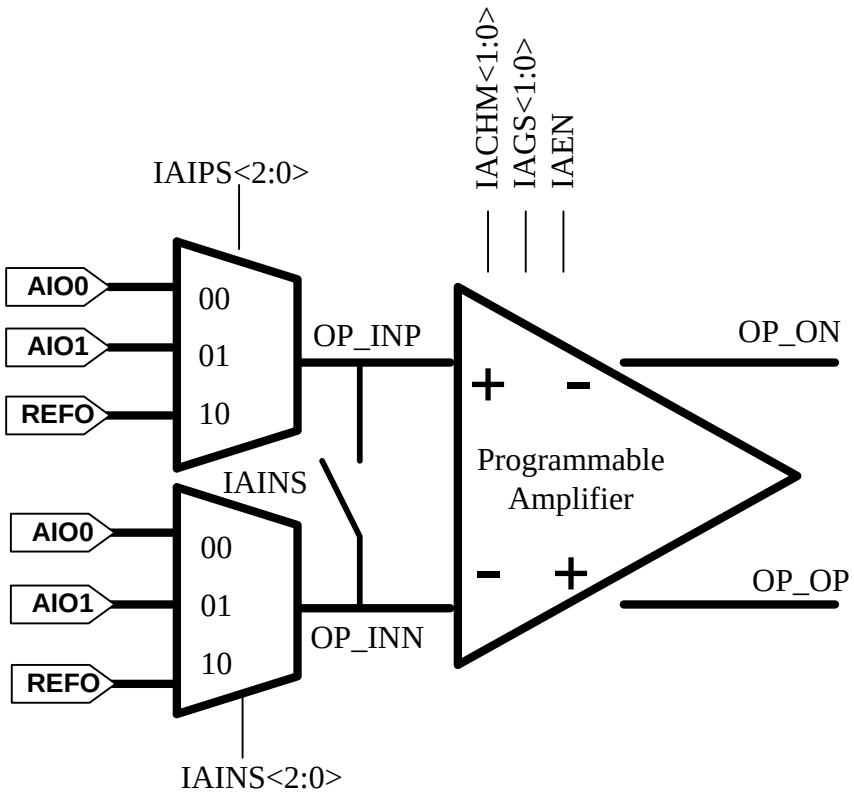
4.5 电源系统网络


10μF
10μF
VDD3V
VLCD
LCD_CLK
EN_LCD_CP
LCDV[1:0]
LCD Charge Pump (2.6/2.8/3.0/3.3)
Regulator
VDD18
1μF
ENBGR[0]
ENVA[0]
VDAS[0]
VDDA (2.4/2.7/3.0/3.3)
VDDA
1μF
BGR
EN_REFO
REFO Buf
REFO
0.1μF
VDDA
ACMS[0]
ADC common voltage
1
0
ACM Buf
ACMS[0]
PT3.6_ENI
VSS
REFO_I

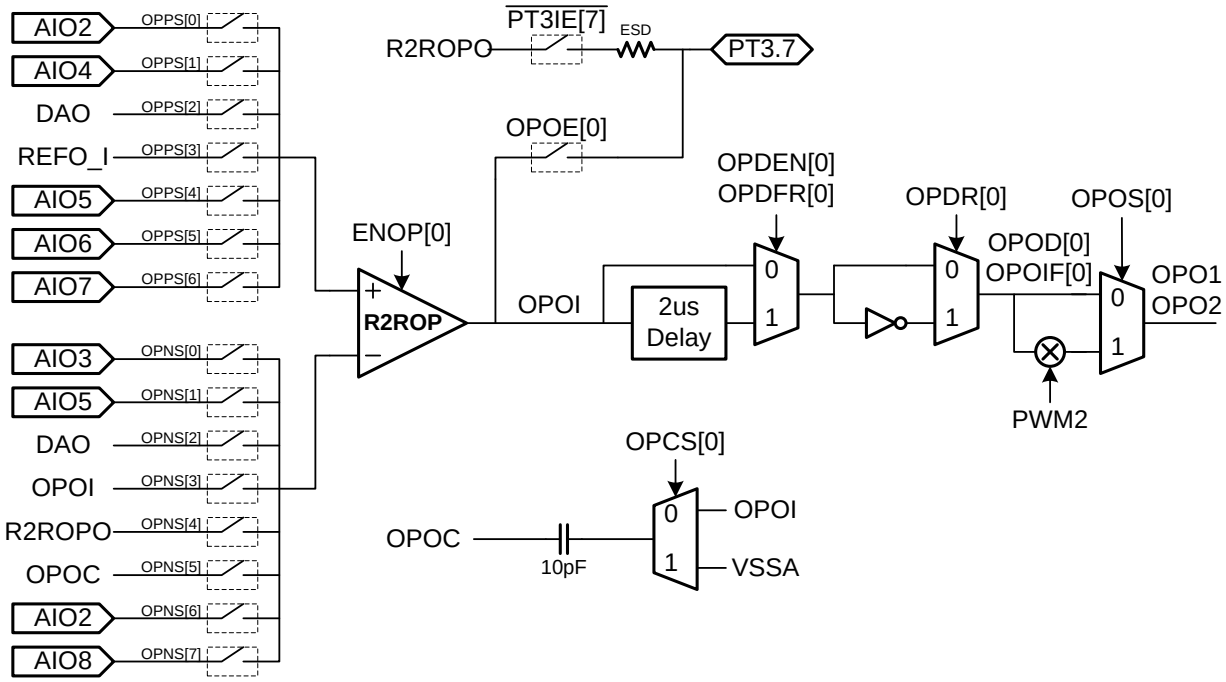
4.6 24-bit ΣΔADC 网络



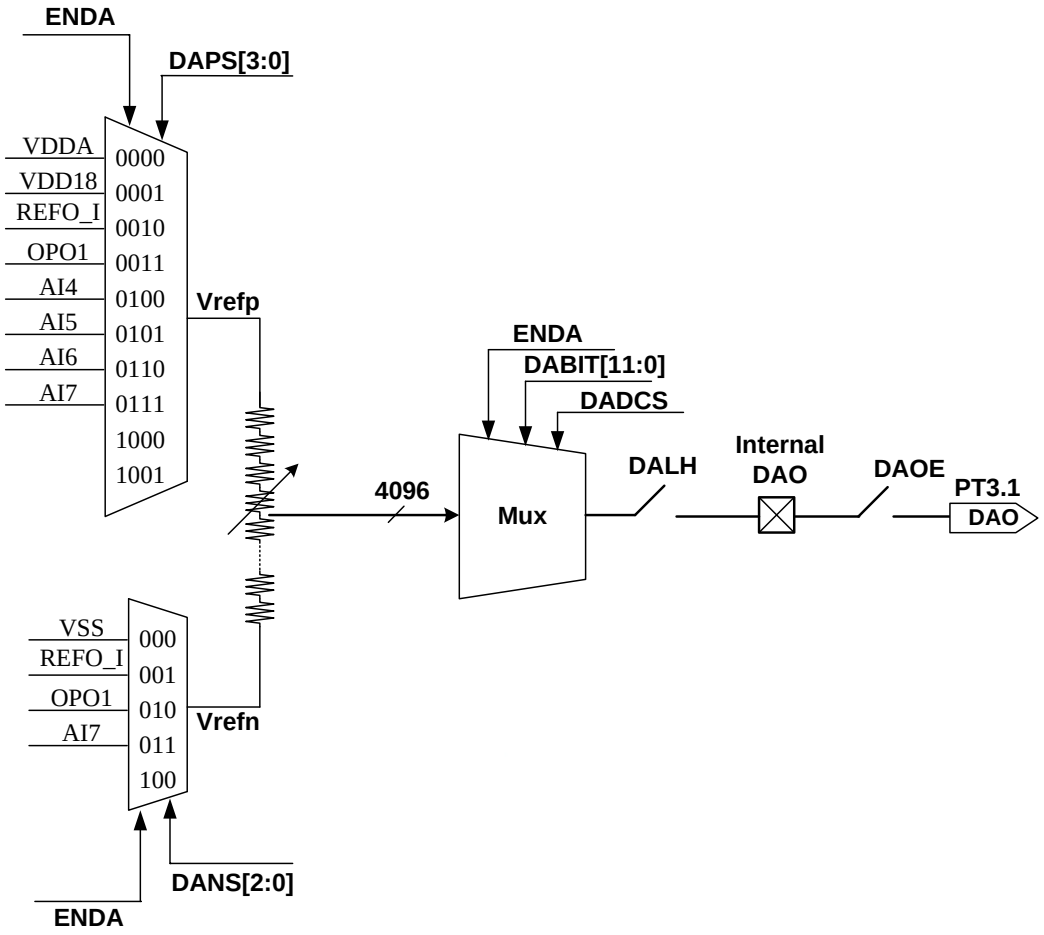
4.7 仪表放大器 IA 网络



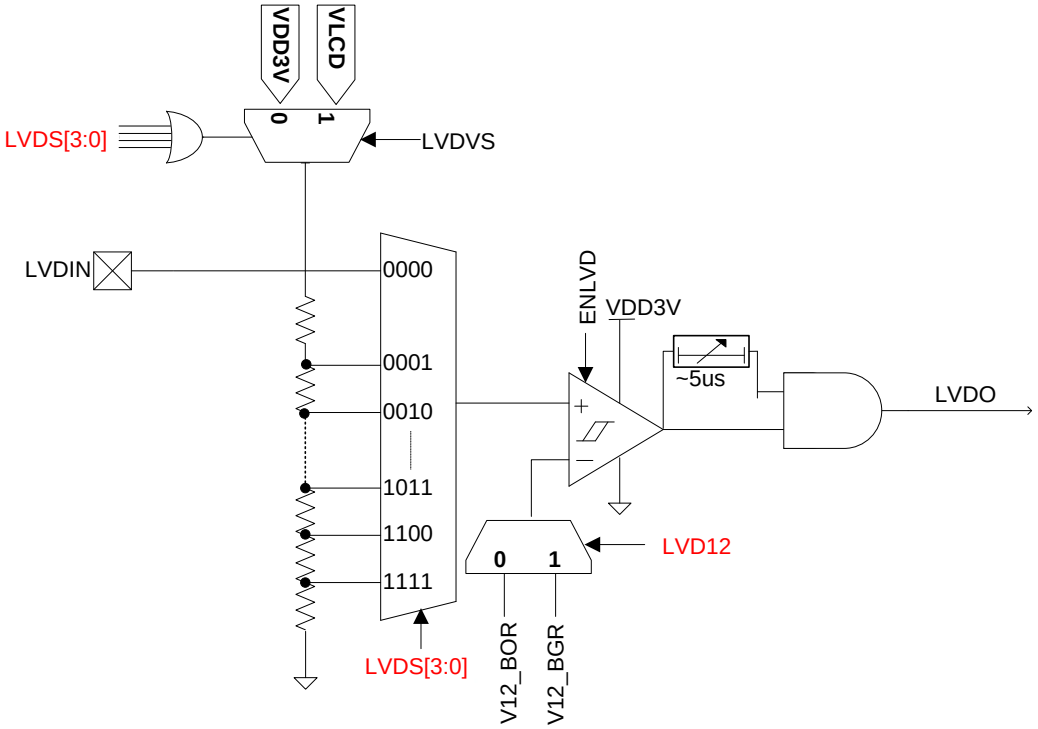
4.8 轨对轨运算放大器 OPAMP 网络



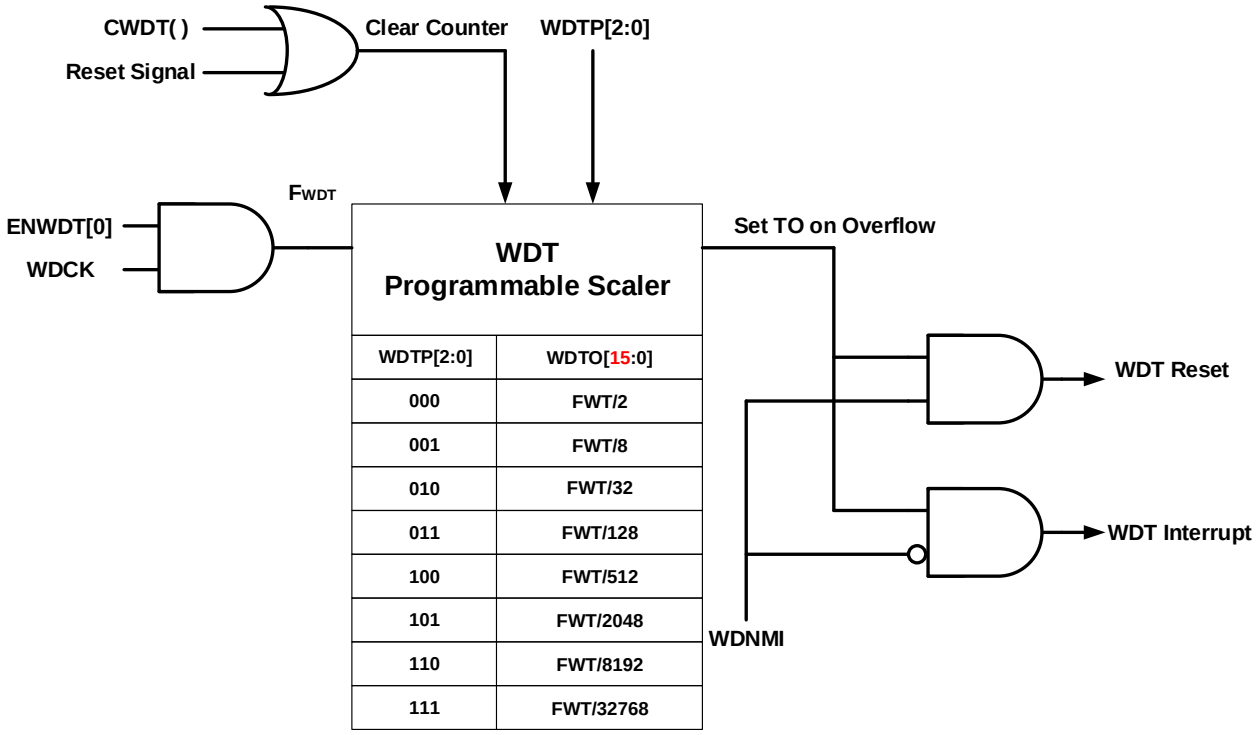
4.9 12-bit Resistance Ladder 网络



4.10 低电压比较器网络

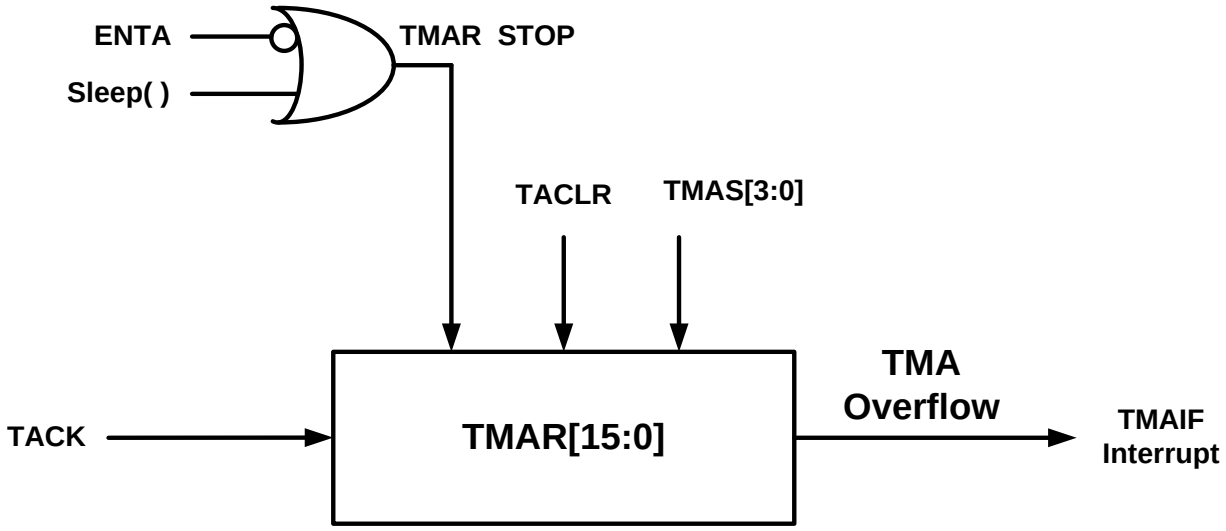


4.11 看门狗(WDT)网络



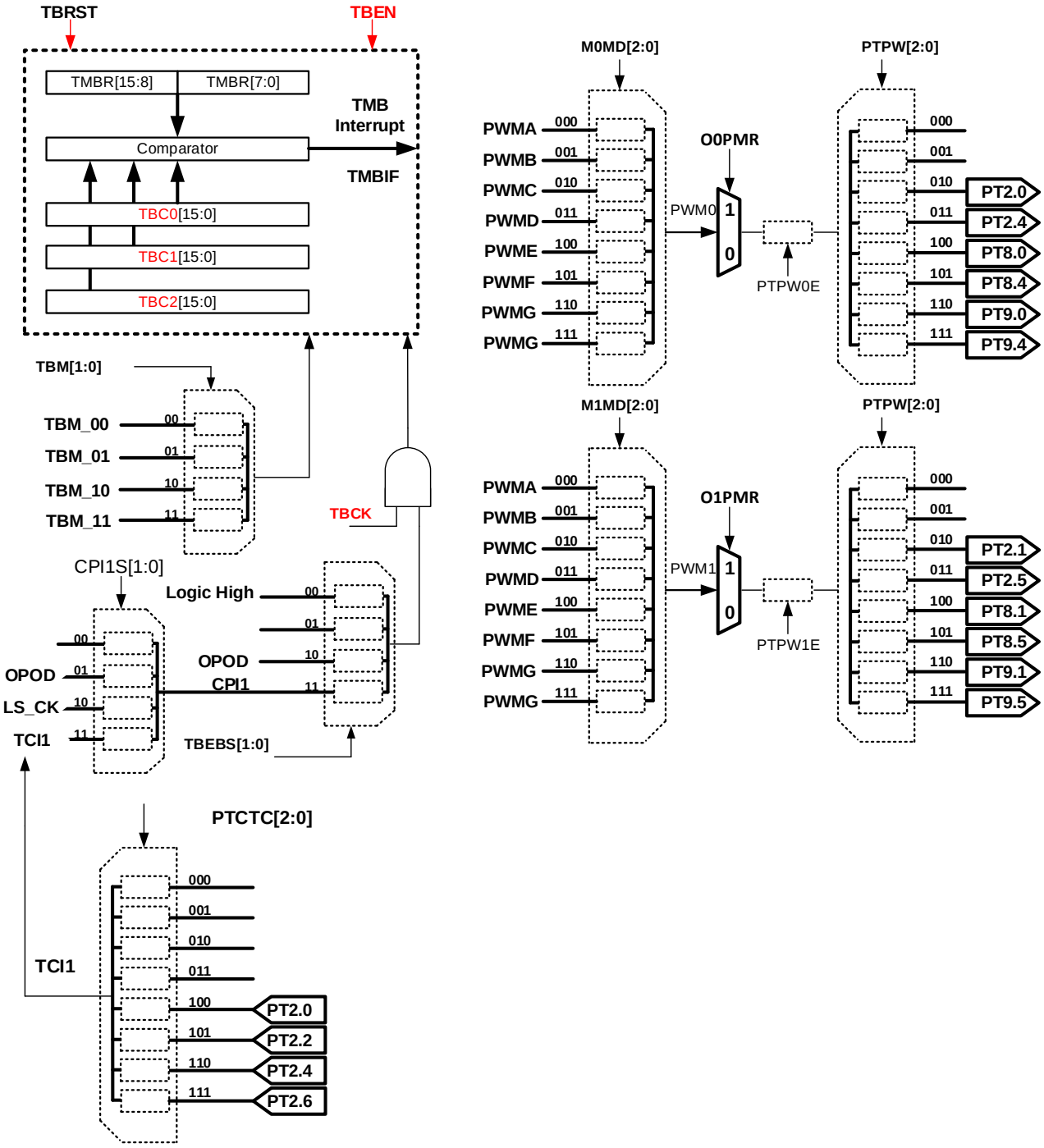
WDTP[2:0]	WDTO[15:0]
000	FWT/2
001	FWT/8
010	FWT/32
011	FWT/128
100	FWT/512
101	FWT/2048
110	FWT/8192
111	FWT/32768

4.12 定时计数器 A 网络

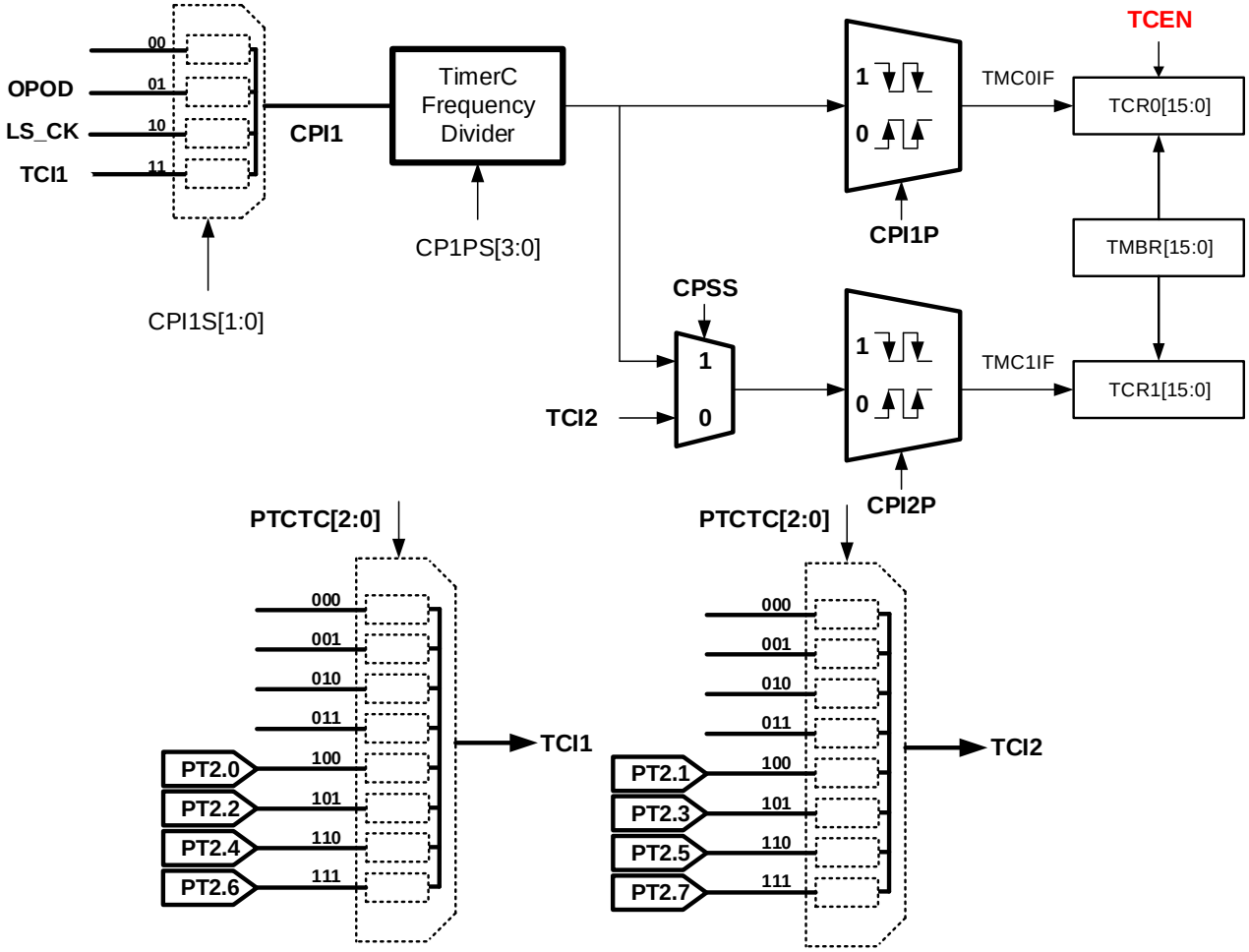


TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

4.13 定时计数器 B 网络

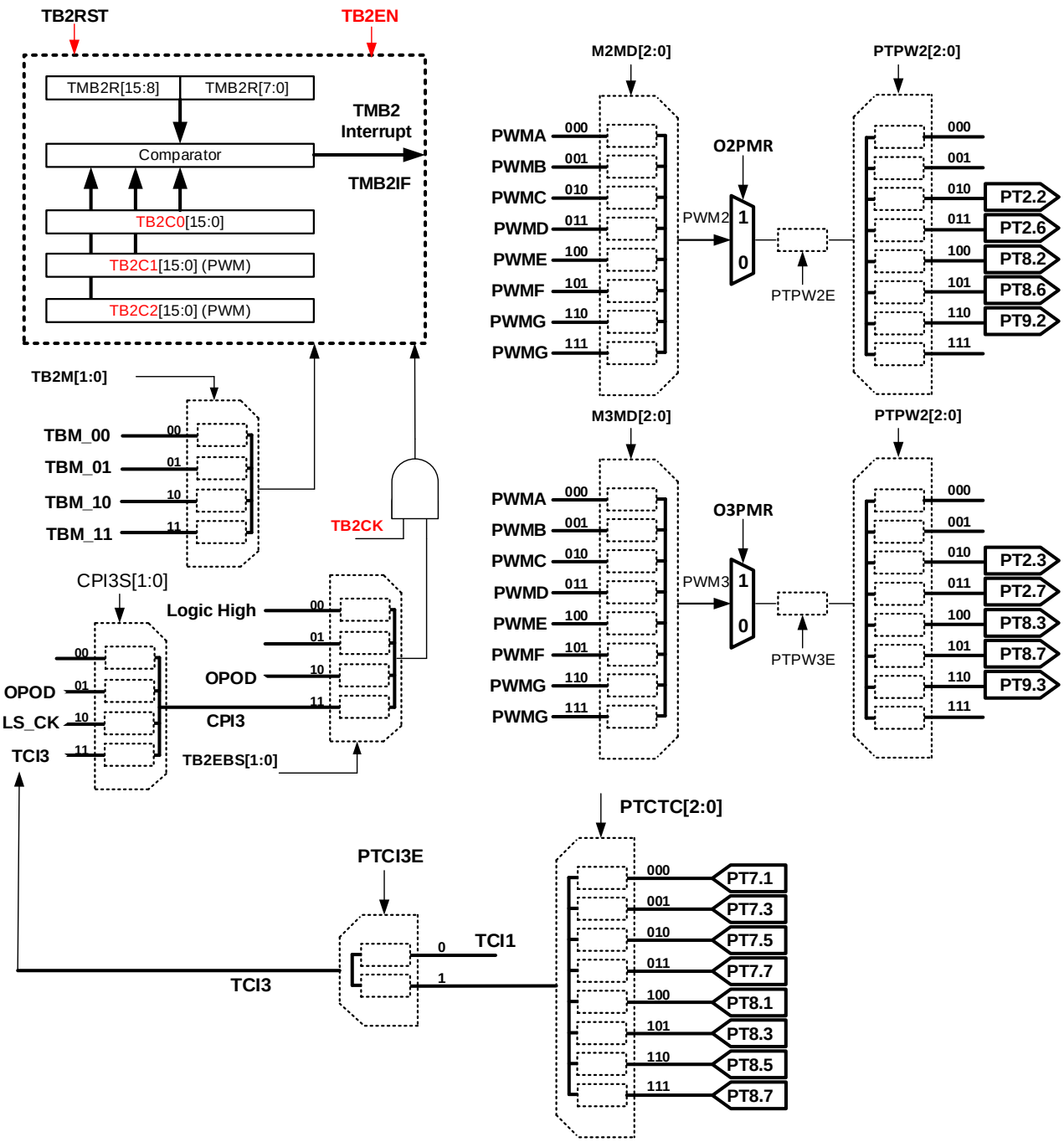


4.14 定时计数器 C 网络

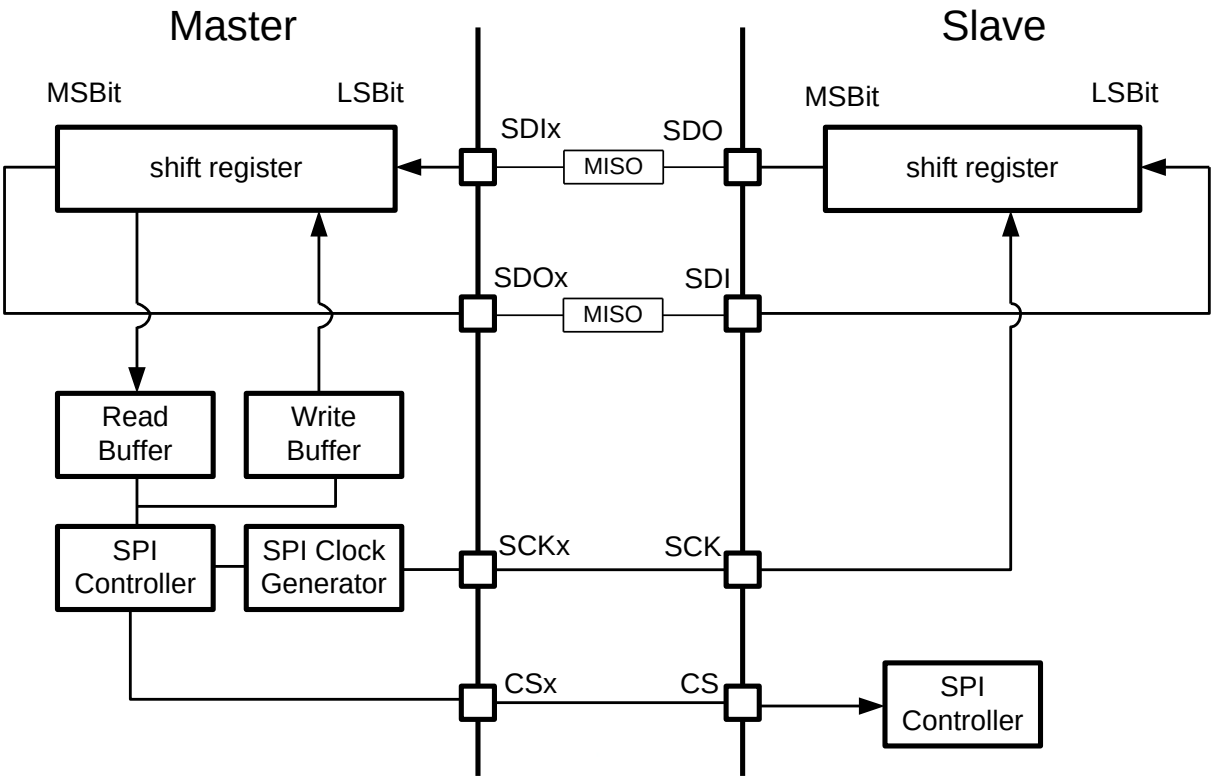


CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

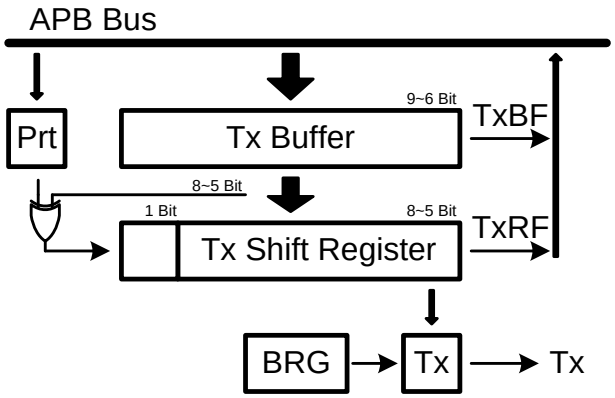
4.15 定时计数器 B2 网络



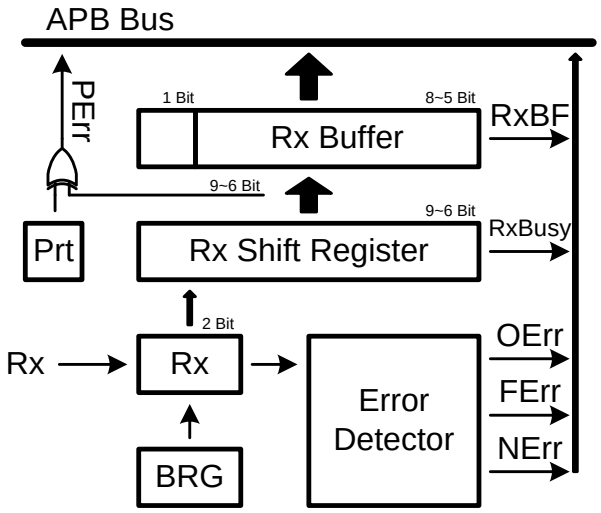
4.16 32-bit SPI 网络



4.17 UART 网络

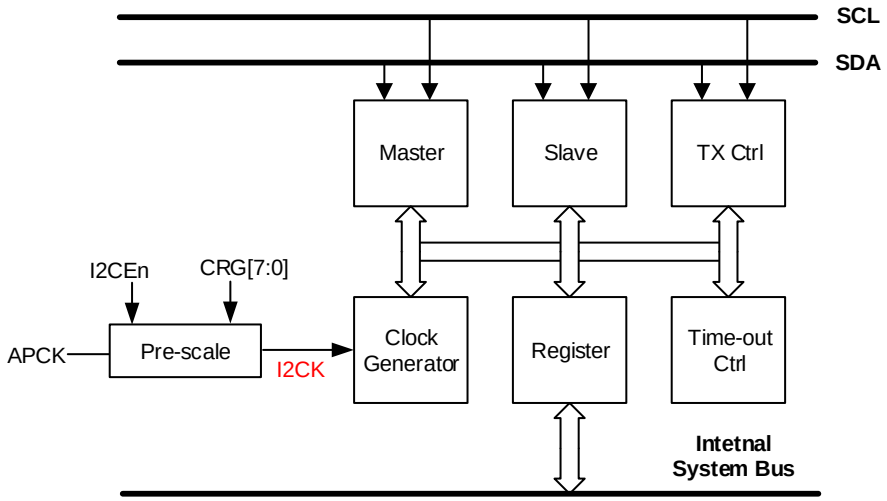


UART Transmit Block Diagram

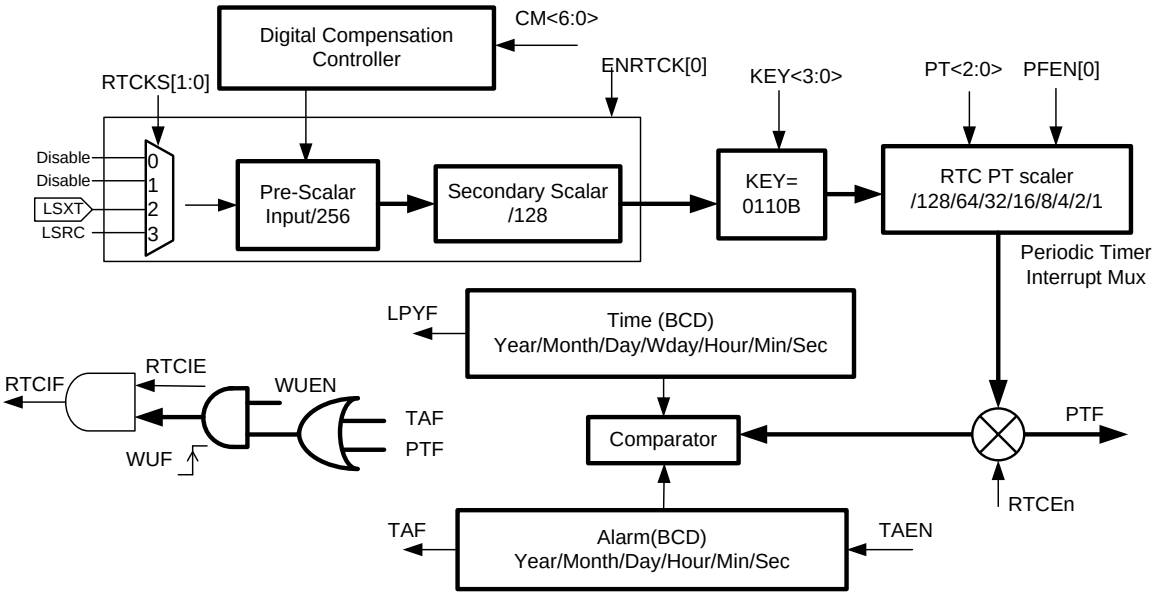


UART Receive Block Diagram

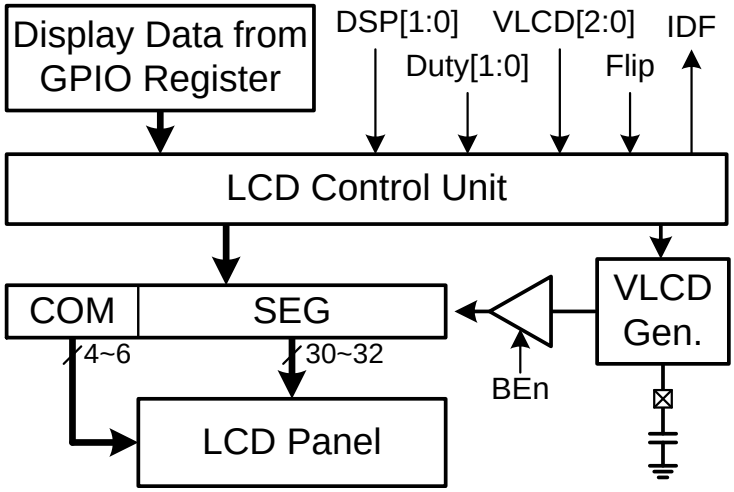
4.17 I2C 网络



4.18 硬件万年历 RTC 网络



4.19 LCD 网络


Display Data from GPIO Register
DSP[1:0]
Duty[1:0]
VLCD[2:0]
Flip
IDF
LCD Control Unit
COM
SEG
4~6
30~32
BEn
VLCD Gen.
LCD Panel

5. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)
Voltage applied at VDD3V to VSS ……−0.2 V to 4.0 V
Voltage applied to any pin …….... −0.2 V to VDD3V + 0.3 V
Diode current at any device terminal…… ±2mA
Storage temperature, Tstg: (UN programmed device) ..... −55℃ to 150℃
(Programmed device) …….... −40℃ to 85℃
Soldering Temperature (10 Sec) . . . . . ….. . . . . +260°C
Maximum output current sink by any PORT2 to PORT13 I/O PIN ……10mA

5.1 Recommended Operating Conditions

VDD3V=3.0V.TA=25℃,Unless Otherwise Noted

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD3V	Digital power	2.2	3.0	3.6	V
Supply Current	I_Sleep	Sleep Mode		2.5	5	uA
	I_Idle01	LSRC=35KHz LPO IDLE Mode		5	10	uA
	I_Idle02	LSXT=32768Hz IDLE Mode		6.5	12	uA
	I_Idle03	HSRC=2MHz+IDLE Mode		50	70	uA
	I_Idle04	HSRC=4MHz+IDLE Mode		100	130	uA
	I_Idle05	HSRC=10MHz+IDLE Mode		200	260	uA
	I_Idle06	HSRC=16MHz+IDLE Mode (VDD>= 2.6V)		350	460	uA
	Free Run_01MHz	HSRC=2MHz@CPU_CK:2MHz/2		0.6	0.8	mA
	Free Run_02MHz	HSRC=2MHz@CPU_CK:2MHz		1.0	1.2	mA
	Free Run_04MHz	HSRC=4MHz@CPU_CK:4MHz		2.0	2.4	mA
	Free Run_10MHz	HSRC=10MHz@CPU_CK:10MHz		3.0	3.6	mA
	Free Run_16MHz	HSRC=16MHz@CPU_CK:16MHz (VDD>= 2.6V)		4.0	4.8	mA
	Free Run_35KHz	LSRC=35KHz @CPU_CK: LSRC (Low power mode)		20	30	uA
Power Up Delay	$t_{PU,DLY}$	Power on or wake up from sleep mode		64	80	ms

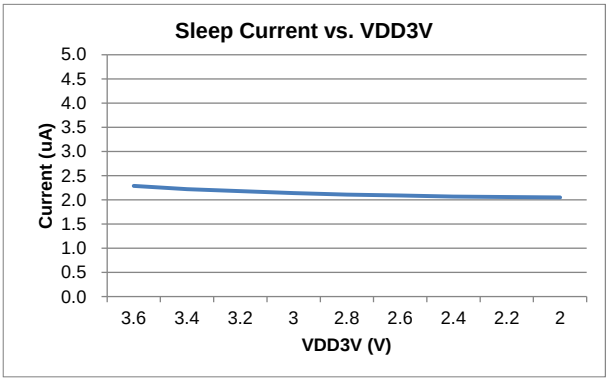


Figure5.1-1 Sleep Current vs. VDD3V

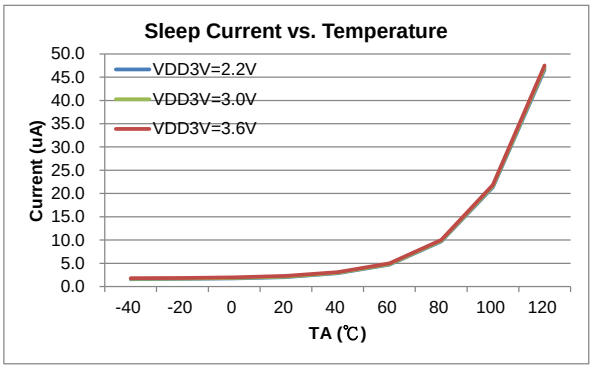


Figure5.1-2 Sleep Current vs. Temperature

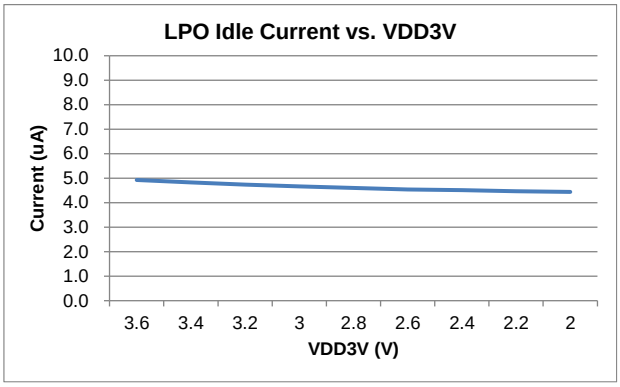


Figure5.1-3 LPO Idle Current vs. VDD3V

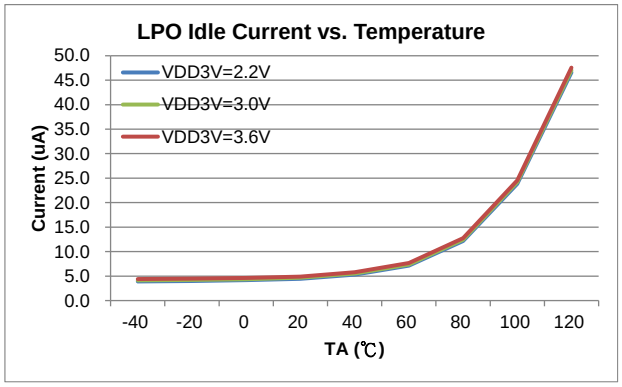


Figure5.1-4 LPO Idle Current vs. Temperature

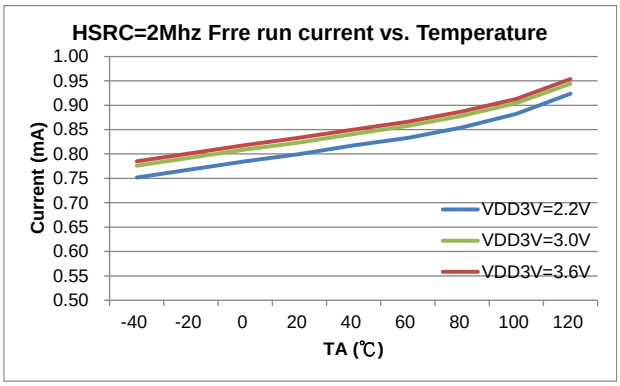


Figure5.1-5 2MHz Free run current vs. Temperature

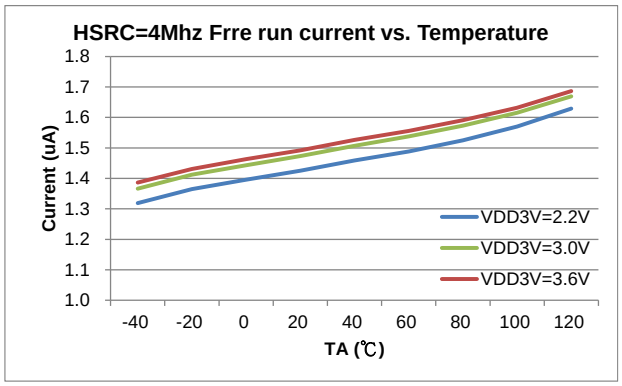


Figure5.1-6 4MHz Free run current vs. Temperature

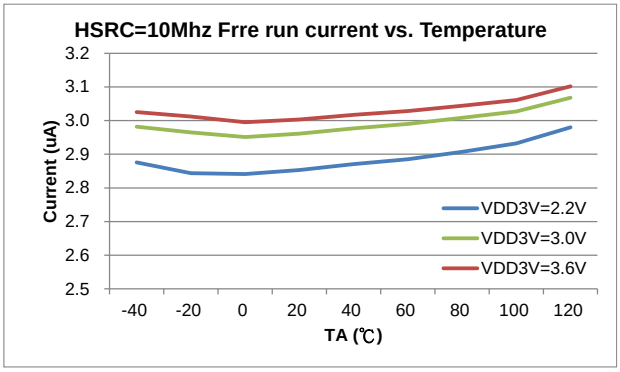


Figure5.1-7 10MHz Free run current vs. Temperature

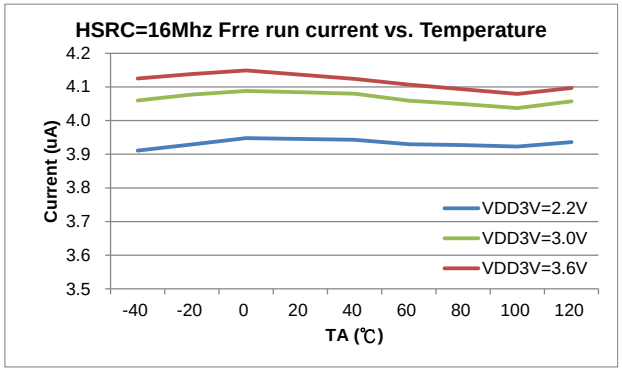


Figure5.1-8 16MHz Free run current vs. Temperature

5.2 Clock System

Typical values are at T_A=25℃ and VDD3V = 3.0V.Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
External High Speed Oscillator						
VDD3V	Operation voltage		2.2		3.6	V
F_{XHS}	High speed oscillator frequency	VDD3V = 2.2V ~ 3.6V OHS_HS = 1b			10	MHz
		VDD3V = 2.6V ~ 3.6V OHS_HS = 1b			16	MHz
		VDD3V = 2.2V ~ 3.6V OHS_HS = 0b			4	MHz
I_{XHS}	High speed oscillator current	F_{XHS} = 16MHz, OHS_HS = 1b, (VDD>= 2.6V)		125		uA
D_{XHS}	Duty of high oscillator		40		60	%
External Low Speed Oscillator						
F_{XLS}	Low speed oscillator frequency	VDD3V = 2.2V ~ 3.6V		32.768		KHz
I_{XLS}	Low speed oscillator current			4		uA
D_{XLS}	Duty of low speed oscillator		40		60	%
RTC	Normal Mode	VDD3V=3.0V @Flash Run		22		uA
Internal High Speed Oscillator						
F_{HAO}	Internal high speed oscillator frequency	F_{HAO} = 2MHz, F_{HAO} = 2MHz, after trim Note1	-10% -2%	2 1.843	+10% +2%	MHz
		F_{HAO} = 4MHz, F_{HAO} = 4MHz, after trim Note1	-10% -2%	4 4.147	+10% +2%	MHz
		F_{HAO} = 10MHz, F_{HAO} = 10MHz, after trim Note1	-10% -2%	10 9.216	+10% +2%	MHz
		F_{HAO} = 16MHz, F_{HAO} = 16MHz, after trim Note1	-10% -2%	16 15.667	+10% +2%	MHz
	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-1.5		+1.5	%
T_{HAO}	Temperature coefficient	-40~85℃	-2.5		+2.5	%
I_{HAO}	Internal high speed oscillator current	F_{HAO} = 2MHz		20		uA
		F_{HAO} = 16MHz (VDD>= 2.6V)		105		uA
D_{HAO}	Duty of oscillator		40		60	%
WT_{HAO}	Wake up time	F_{HAO} = 2MHz		30		us
Internal Low Speed Oscillator						
F_{LPO}	Internal low speed oscillator frequency	VDD3V = 3.0V	-20%	35	+20%	KHz
	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-1.5		+1.5	%
T_{LPO}	Temperature coefficient	-40~85℃	-5		5	%
I_{LPO}	Internal low speed oscillator current			2.5		uA
D_{LPO}	Duty of low speed oscillator		40		60	%

Note1 :

After Trim: According to the factory calibration parameters of HAO to calibrate HAO, and need to corresponding to the selected HAO frequency. Configure the register 0x40304[7:0]. Please refer to the chapter 6.1.2 of “UG-HY16F3981_TC” to know how to use that in detail.

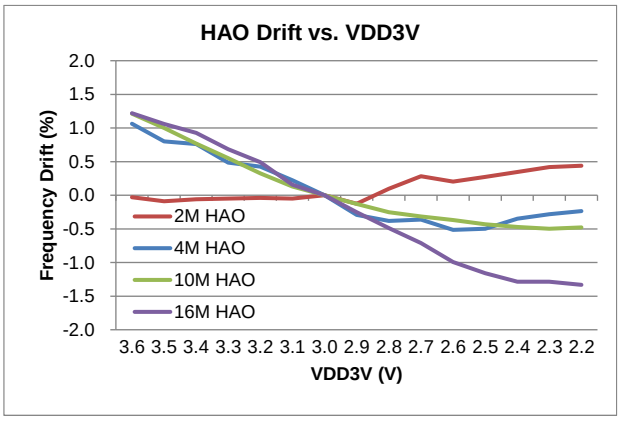


Figure5.2-1 HAO Drift vs. VDD3V

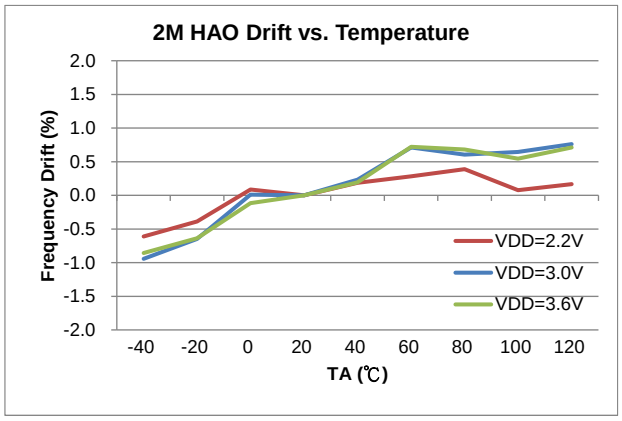


Figure5.2-2 2MHz HAO Drift vs. Temperature

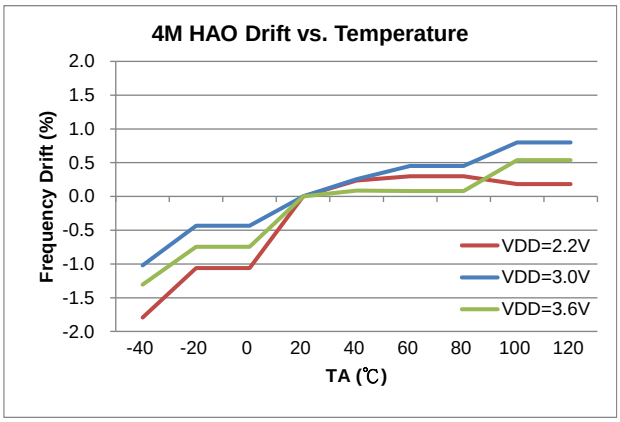


Figure5.2-3 4MHz HAO Drift vs. Temperature

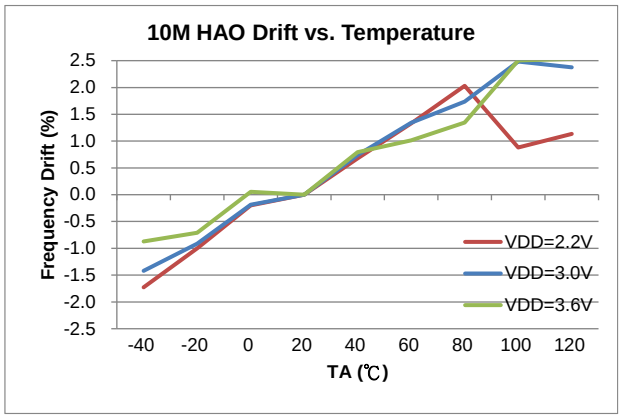


Figure5.2-4 10MHz HAO Drift vs. Temperature

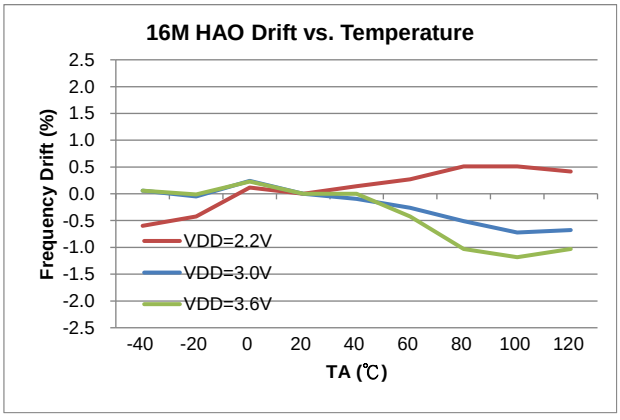


Figure5.2-5 16MHz HAO Drift vs. Temperature

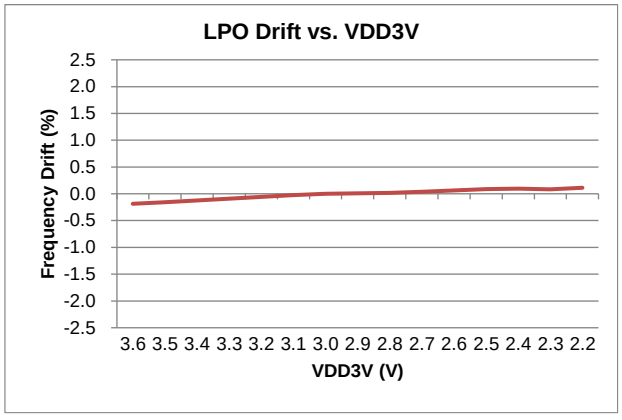


Figure5.2-5 LPO Drift vs. VDD3V

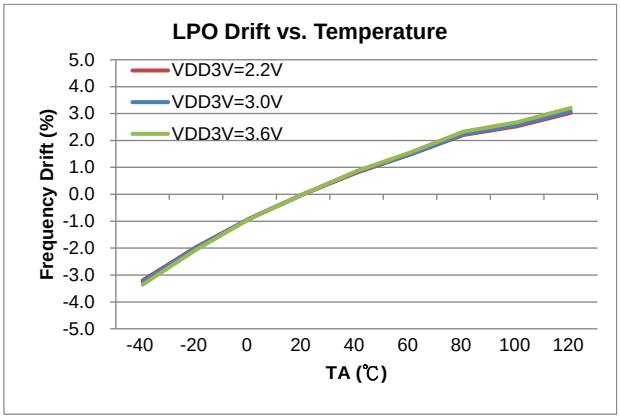


Figure5.2-5 LPO Drift vs. Temperature

5.3 Power Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA LDO						
	Output voltage error		-5		5	%
	Capacitor loading		0.1	1	10	uF
	Settling time	Capacitor loading = 0.1uF, 99% of VDDA		100		us
	Operation current	Bias + Band gap + VDDA LDO		35	50	uA
	Dropout voltage	I_L=10mA		0.2		V
	Voltage coefficient	VDD3V = 2.5 ~ 3.6V		0.1		%/V
	VDDA voltage 1 0x40400[19:18]=00b	I_L = 0.1mA	2.3	2.4		V
	VDDA voltage 2 0x40400[19:18]=01b	I_L = 0.1mA		2.6		V
	VDDA voltage 3 0x40400[19:18]=10b	I_L = 0.1mA		2.9		V
	VDDA voltage 4 0x40400[19:18]=11b	I_L = 0.1mA		3.2		V
	Temperature coefficient	By using BRG VDDA=3.0V		100		ppm/°C
VDD18 LDO						
	Output voltage		1.7	1.8	1.9	V
	Capacitor loading		100	1000	2200	nF
	Voltage coefficient	VDD3V= 2.2 ~ 3.6V		1		%/V
	Temperature coefficient			50		ppm/°C
	Load regulation	Load = 0.1~1mA		0.1		V/A
	Dropout voltage	Load = 1mA		0.2		V
REFO Buffer						
	Output voltage		1.1	1.2	1.3	V
	Capacitor loading		22	100	1000	nF
	Operation current			20		uA
	Output current	1% change voltage	-1		1	mA
	Temperature coefficient	VDDA=2.9V		80		ppm/°C
	Voltage coefficient	VDDA= 2.4V ~ 3.6V		0.1		%/V

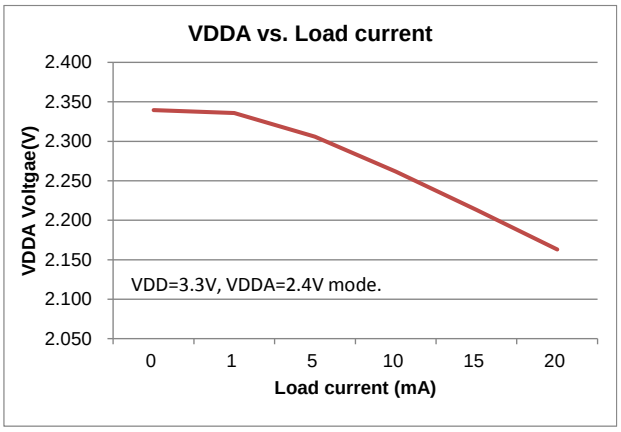


Figure5.3-1 VDDA=2.4V vs. IL

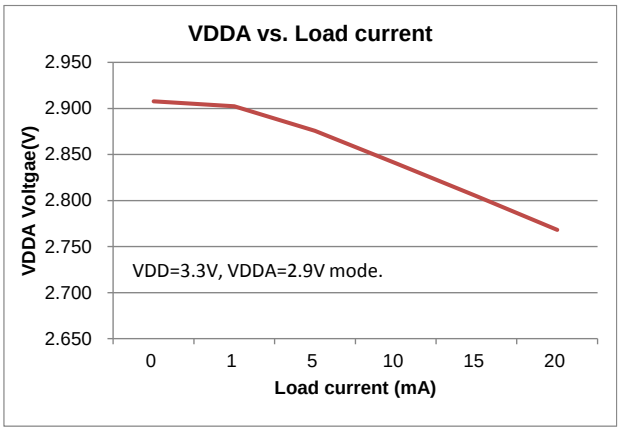


Figure5.3-2 VDDA=2.9V vs. IL

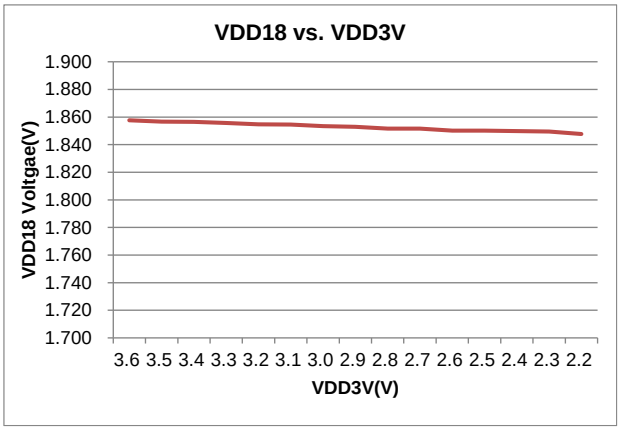


Figure5.3-3 VDD18 vs. VDD3V

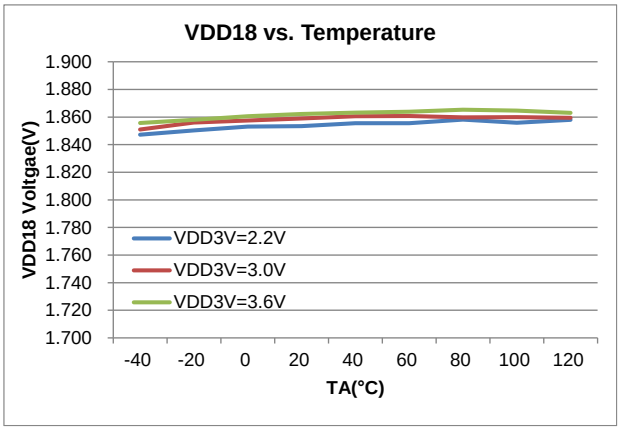


Figure5.3-4 VDD18 vs. Temperature

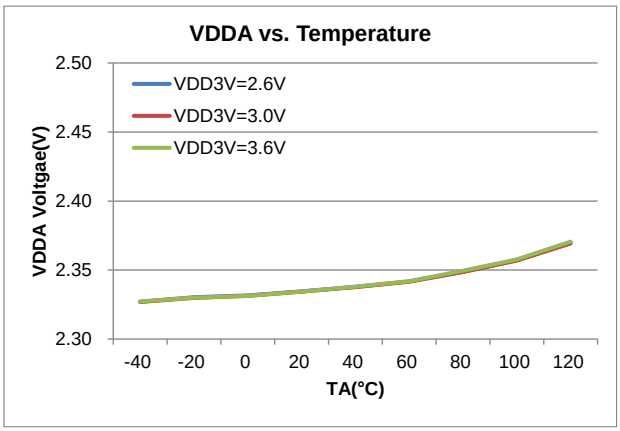


Figure5.3-5 VDDA=2.4V vs. Temperature

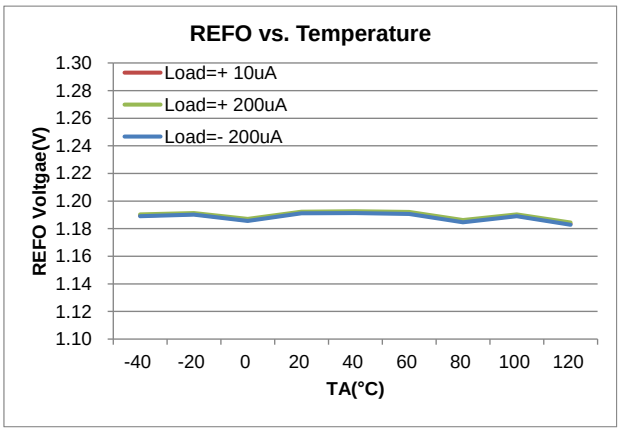


Figure5.3-6 REFO vs. Temperature

5.4 Reset Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Min.	Typ.	Max.	Unit
BOR	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$	2			us
	VDD Start Voltage to accepted reset internally (L→H),V_{LVR}	1.8	1.95	2.1	V
	VDD Start Voltage to accepted reset internally (H→L),V_{HYS}	1.7	1.87	2.05	V
	Temperature drift, T_A=-40℃~85℃	-50		+50	mV
	Hysteresis, $V_{HYS\text{-}LVR}$		80		mV
POR	Operation Slew Rate			0.1	V/us
	Start Voltage to accepted reset	0.6			V

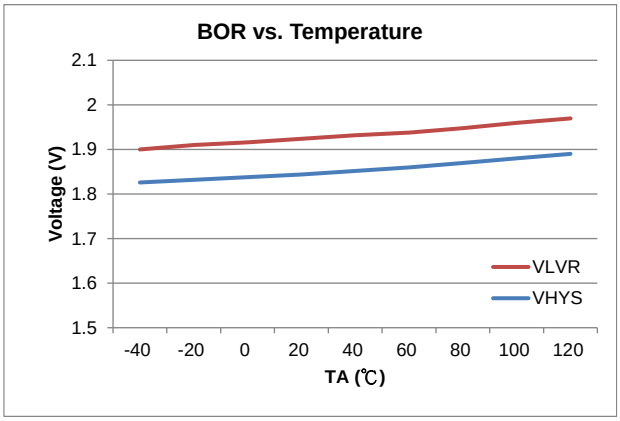


Figure5.4 VLVR and VHYS vs. Temperature

5.5 GPIO Port System

Typical values are at T_A=25℃ and VDD3V = 3.3V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PT 1.0 ~ 4.0 GPIO Port						
R_{PU}	Internal pull high resistor		65	85	105	kΩ
V_{IH}	Input high voltage		0.7*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current			10		mA
I_{OL}	Sink current			10		mA
PT 6.0 ~ 9.5 GPIO Port						
V_{IH}	Input high voltage		0.6*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current	VDD3V-0.3V		10		mA
I_{OL}	Sink current	VSS+0.3V		10		mA

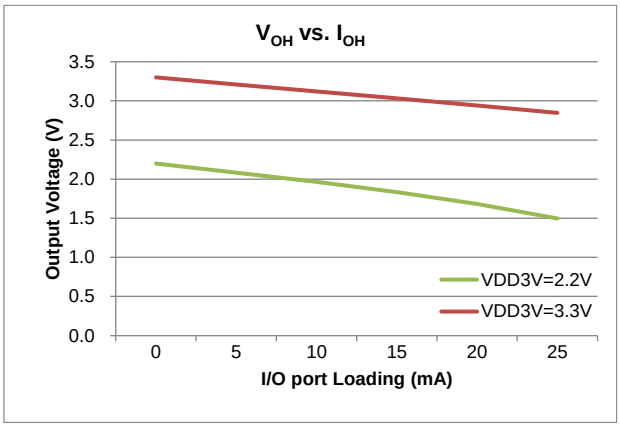


Figure5.5-1 VOH vs. IOH

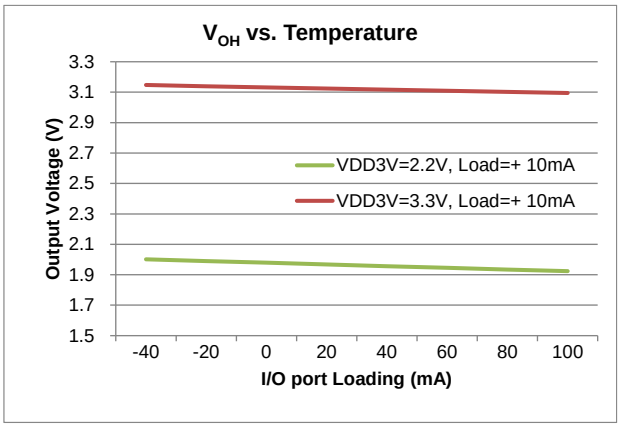


Figure5.5-2 VOH vs. Temperature

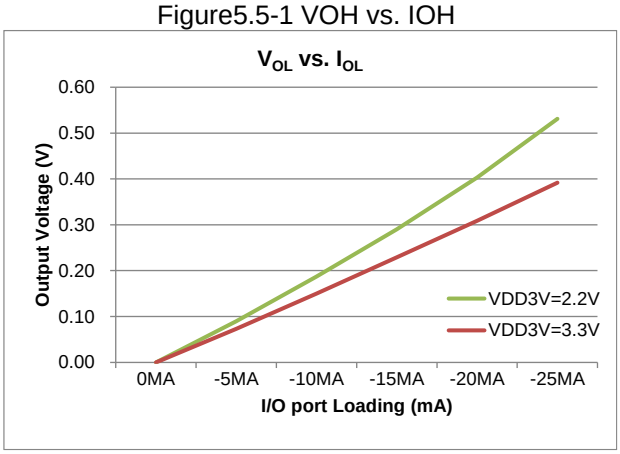


Figure5.5-3 VOL vs. IOL

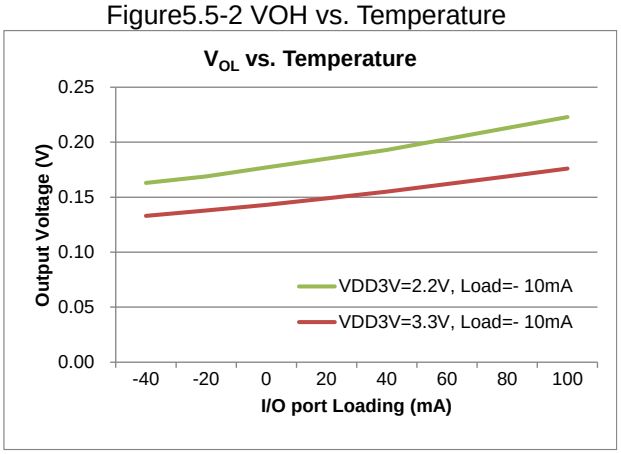


Figure5.5-4 VOL vs. Temperature

5.6 ΣΔADC ENOB and RMS Noise

Typical values are at TA=25℃ and VDD3V = 3.3V, VDDA=2.4V and HS_CK=4MHz, unless otherwise noted.HY16F3981 provides important input noise specification that aims at ΣΔADC. Table 5.6-1 and Table 5.6-2 lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled. IA Chopper On means register IACHM=11b.

ENOB(RMS) with OSR/GAIN at A/D Clock=1Mhz, VDDA=2.4V, VREF=1.2V, IA Chopper On															
Max. Vin(mV) =0.9*VREF (1)	**OSR**					**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**15625**	**7813**	**3906**	**1953**	**977**	**488**	**244**	**122**	**61**	**31**
	Gain	**=**	**IA**	**×**	**ADGN**										
±1080	**1**	**=**	**off**	**×**	**1**	15.3	16.9	17.5	18.0	18.3	18.7	19.5	20.2	20.6	21.0
±540	**2**	**=**	**off**	**×**	**2**	15.2	16.7	17.3	17.8	18.2	18.8	19.3	19.8	20.2	20.5
±270	**4**	**=**	**off**	**×**	**4**	15.2	16.4	17.1	17.5	18.0	18.6	19.0	19.5	19.8	20.2
±135	**8**	**=**	**off**	**×**	**8**	14.9	16.1	16.6	17.2	17.6	18.2	18.5	18.9	19.3	19.6
±270	**4**	**=**	**4**	**×**	**1**	15.2	16.6	17.1	17.6	17.9	18.4	18.8	19.6	20.2	20.5
±135	**8**	**=**	**4**	**×**	**2**	14.8	15.9	16.5	17.0	17.4	17.9	18.4	19.0	19.4	20.0
±67.5	**16**	**=**	**4**	**×**	**4**	14.5	15.1	15.7	16.2	16.6	17.1	17.7	18.2	18.6	19.1
±33.75	**32**	**=**	**4**	**×**	**8**	13.7	14.2	14.7	15.2	15.7	16.3	16.8	17.2	17.7	18.1
±135	**8**	**=**	**8**	**×**	**1**	15.2	16.5	17.0	17.5	18.0	18.4	19.1	19.6	20.0	20.5
±67.5	**16**	**=**	**8**	**×**	**2**	14.8	15.9	16.3	16.8	17.3	17.9	18.3	18.9	19.3	19.7
±33.75	**32**	**=**	**8**	**×**	**4**	14.3	15.0	15.4	16.0	16.5	17.0	17.5	18.0	18.4	19.0
±16.875	**64**	**=**	**8**	**×**	**8**	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	17.9
±67.5	**16**	**=**	**16**	**×**	**1**	15.0	16.1	16.7	17.1	17.5	18.1	18.7	19.1	19.6	20.1
±33.75	**32**	**=**	**16**	**×**	**2**	14.5	15.3	15.8	16.3	16.7	17.3	17.8	18.2	18.7	19.3
±16.875	**64**	**=**	**16**	**×**	**4**	13.8	14.3	14.9	15.3	15.8	16.4	16.8	17.4	17.8	18.4
±8.4375	**128**	**=**	**16**	**×**	**8**	12.8	13.4	13.9	14.4	14.8	15.4	15.9	16.3	16.9	17.4
±33.75	**32**	**=**	**32**	**×**	**1**	14.6	15.3	15.9	16.4	16.9	17.4	17.9	18.4	18.9	19.4
±16.875	**64**	**=**	**32**	**×**	**2**	13.8	14.4	14.9	15.4	15.9	16.4	16.9	17.5	17.9	18.4
±8.4375	**128**	**=**	**32**	**×**	**4**	12.9	13.4	14.0	14.5	14.9	15.5	16.0	16.4	17.0	17.4
±4.21875	**256**	**=**	**32**	**×**	**8**	12.0	12.5	12.9	13.5	13.9	14.5	15.0	15.5	16.0	16.4
(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).															

Table 5.6-1 ΣΔADC ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=1Mhz, VDDA=2.4V, VREF=1.2V, IA Chopper On														
Max. Vin(mV) =0.9*VREF	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					15625	7813	3906	1953	977	488	244	122	61	31
	Gain	=	IA	×	ADGN										
±1080	1	=	off	×	1	58.85	19.18	12.49	8.86	7.08	5.33	3.24	1.98	1.46	1.11
±540	2	=	off	×	2	31.64	11.13	7.10	5.13	3.92	2.52	1.75	1.28	1.00	0.79
±270	4	=	off	×	4	15.79	6.77	4.29	3.19	2.19	1.52	1.11	0.79	0.64	0.48
±135	8	=	off	×	8	9.30	4.20	2.91	1.98	1.42	1.00	0.79	0.61	0.45	0.38
±270	4	=	4	×	1	15.10	5.99	4.04	3.01	2.31	1.68	1.32	0.75	0.48	0.39
±135	8	=	4	×	2	9.94	4.69	3.25	2.25	1.73	1.21	0.83	0.57	0.42	0.28
±67.5	16	=	4	×	4	6.38	4.09	2.84	1.90	1.48	1.01	0.70	0.49	0.36	0.25
±33.75	32	=	4	×	8	5.56	3.99	2.74	1.93	1.35	0.91	0.65	0.49	0.33	0.26
±135	8	=	8	×	1	7.99	3.15	2.25	1.54	1.14	0.84	0.52	0.36	0.28	0.19
±67.5	16	=	8	×	2	5.05	2.44	1.81	1.26	0.88	0.60	0.45	0.31	0.22	0.17
±33.75	32	=	8	×	4	3.56	2.28	1.66	1.14	0.79	0.55	0.40	0.29	0.20	0.14
±16.875	64	=	8	×	8	3.21	2.23	1.56	1.13	0.78	0.56	0.38	0.28	0.19	0.15
±67.5	16	=	16	×	1	4.57	2.04	1.38	1.03	0.76	0.53	0.35	0.25	0.19	0.13
±33.75	32	=	16	×	2	3.12	1.83	1.29	0.94	0.70	0.46	0.32	0.25	0.17	0.11
±16.875	64	=	16	×	4	2.57	1.79	1.23	0.89	0.62	0.43	0.32	0.22	0.16	0.11
±8.4375	128	=	16	×	8	2.58	1.74	1.21	0.86	0.62	0.43	0.31	0.23	0.15	0.11
±33.75	32	=	32	×	1	3.02	1.76	1.20	0.85	0.61	0.43	0.29	0.21	0.15	0.10
±16.875	64	=	32	×	2	2.54	1.69	1.16	0.82	0.59	0.41	0.30	0.20	0.15	0.10
±8.4375	128	=	32	×	4	2.35	1.65	1.14	0.79	0.58	0.40	0.28	0.21	0.14	0.10
±4.21875	256	=	32	×	8	2.22	1.56	1.16	0.79	0.59	0.39	0.29	0.20	0.14	0.10

Table 5.6-2 ΣΔADC RMS Table

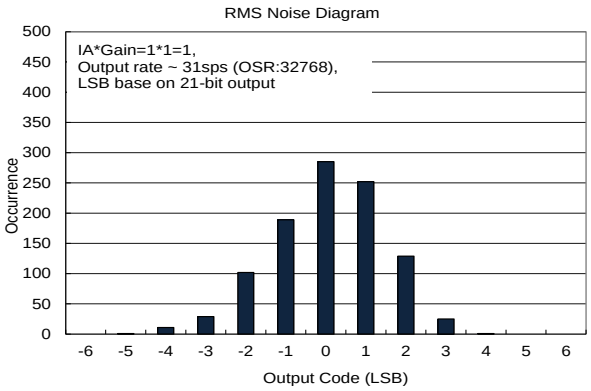


Figure5.6-1(a) RMS Noise Diagram

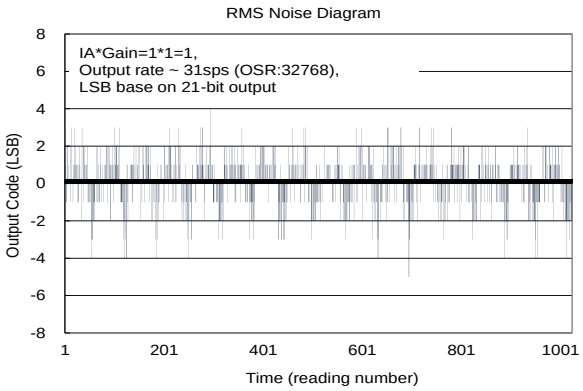


Figure5.6-1(b) Output Code Diagram

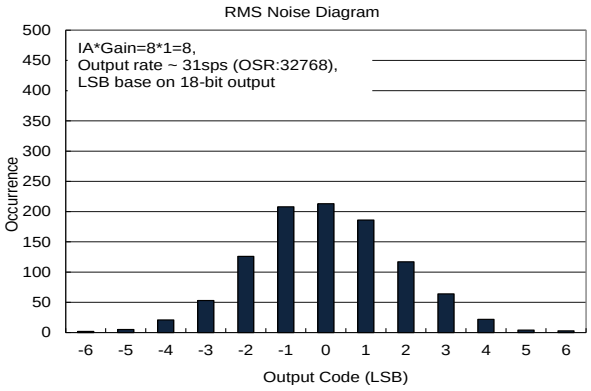


Figure5.6-2(a) RMS Noise Diagram

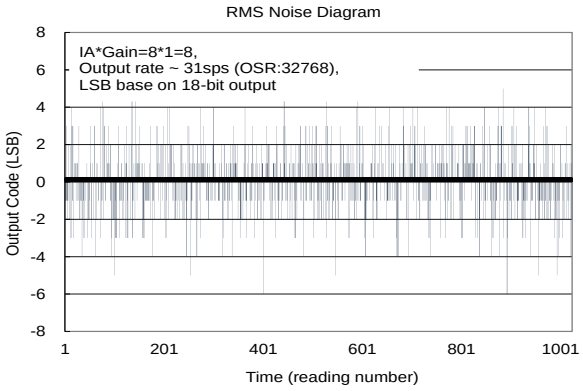


Figure5.6-2(b) Output Code Diagram

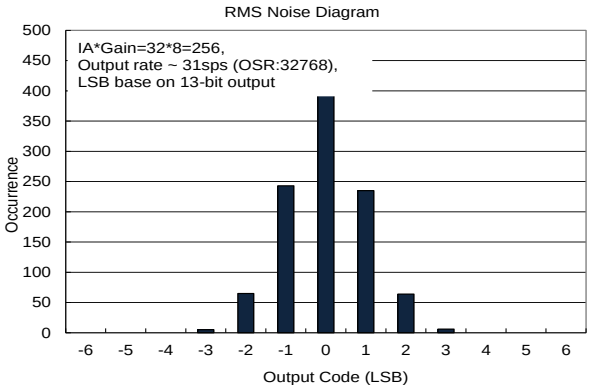


Figure5.6-3(a) RMS Noise Diagram

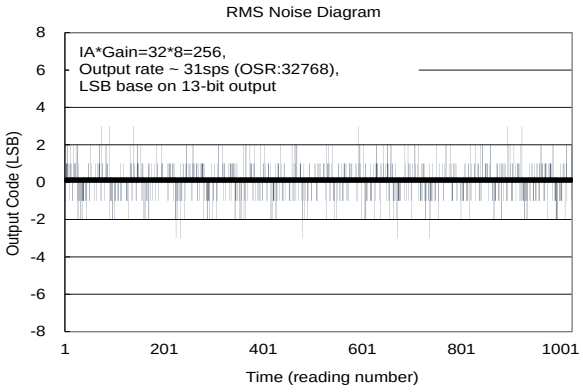


Figure5.6-3(b) Output Code Diagram

5.7 ADC Management System

All specifications at T_A=-40℃ to +85℃,

VDDA=REFP=3.0V, REFN=VSS, Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Analog Inputs							
	Full-scale input voltage (VINP - AINN) Note1	Considering ADC performance matches ADC ENOB table. REFP=VDDA, REFN=VSS VREF be set to 1/2 only		±0.5*VREF/Gain			V
		Considering ADC performance matches ADC ENOB table. REFP=REFO_I REFN=VSS VREF be set to 1 only		±VREF/Gain			
	Common-mode input range	Gain = 1, @25℃		VSS-0.2V		VDDA	V
System Performance							
	Resolution	No missing codes			24		Bits
	Data rate				ADC Clock /OSR		SPS
	Digital filter settling time	Full setting			3		Data
	Integral nonlinearity (INL)	Differential input End-point fit, OSR=32768			15		PPM
	ADC Gain drift				2		ppm/℃
	Normal-mode rejection	f_{IN}=60Hz ±1Hz, Output rate = 31 SPS	Internal OSC		70		dB
			External OSC		80		dB
	Common-mode rejection	ΔVDDA = 0.1V @ DC			80		dB
	Input-referred noise	Output rate= 31 SPS, ADC Gain=1			0.38		uV, rms
	Power-supply rejection	ΔVDDA = 0.1V @ DC			80		dB
Voltage Reference Input							
	Voltage reference input	VREF = REFP - REFN				VDDA	V
	Positive Reference Input	REFP, @25℃		>REFN		VDDA	V
	Negative Reference Input	REFN, @25℃		VSS		<REFP	V
ADC Modulator Current							
ADC	ADC Modulator	VDD3V=3.3V,VDDA=2.4V, ADC Clock=1Mhz			350		uA
IA	ADC IA	VDD3V=3.3V,VDDA=2.4V			300		uA

Note1 :

当 REFP-REFN(VREF) = 1*VDDA 时,

则 VINP-VINN 的差分输入信号不能大于 1/2*VDDA，否则会有线性度问题

当 REFP-REFN(VREF) = 1/2*VDDA 时,

则 VINP-VINN 的差分输入信号不能大于 0.9*VREF，否则会有线性度问题

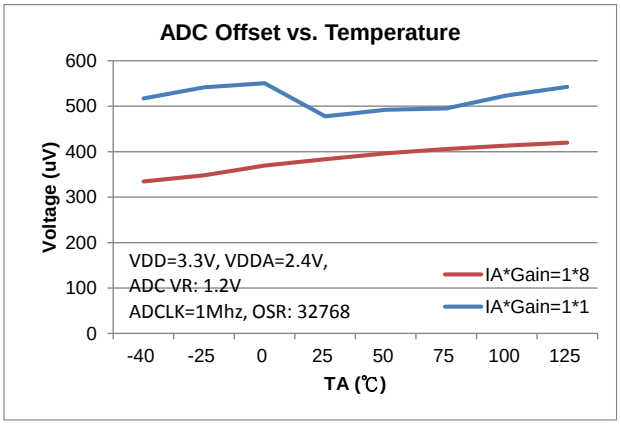


Figure5.7-1 ADC Offset vs. Temperature

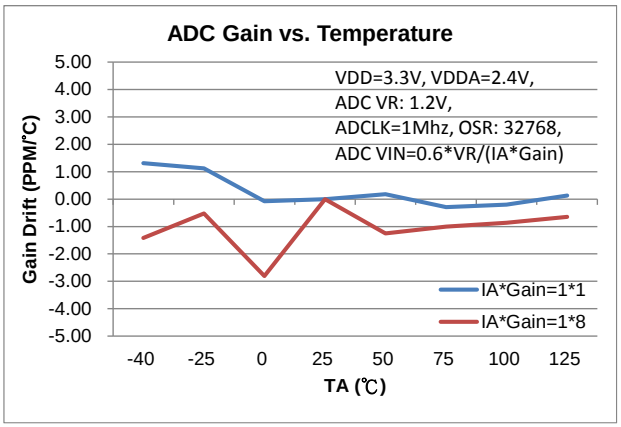


Figure5.7-3 ADC Gain Drift vs. Temperature

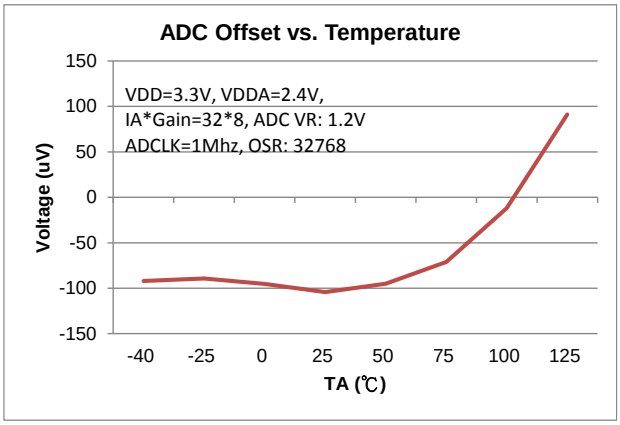


Figure5.7-2 ADC Offset vs. Temperature

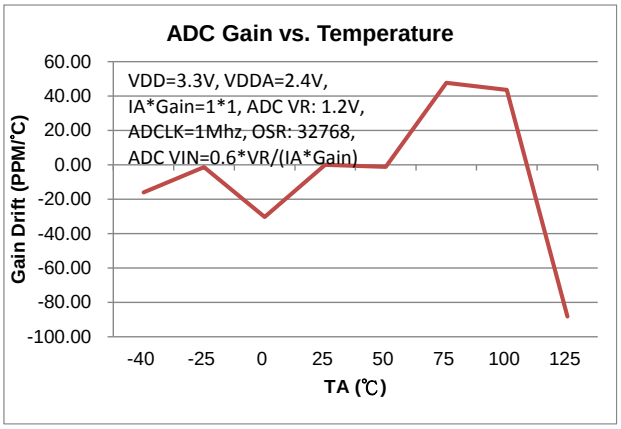


Figure5.7-4 ADC Gain Drift vs. Temperature

5.8 Internal Temperature Sensor

Typical values are at T_A=25℃, VDD3V = 3.0V, and VDDA=2.4V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			172		uV/℃
KT	Absolute temperature scale 0K			-283		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

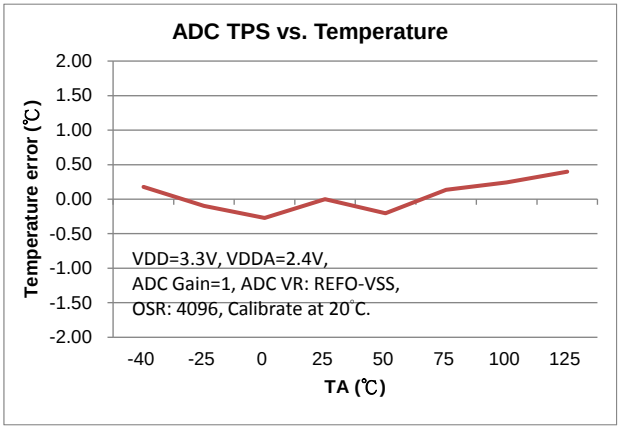


Figure5.8-1 ADC Temperature Sensor Error

5.9 12-Bit Resistance Ladders

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Resolution		Monotonic		12		Bit
	Power Supply		2.4		VDDA	V
	Operation current			50		uA
V_{OUT}	Output range	DA output is between VR- and VR+	0		VDDA	V
V_{REFP}	Positive reference voltage range	$V_{REFP} > V_{REFN}$	0		VDDA	V
V_{REFN}	Negative reference voltage range		0		VDDA	V
R_{ON}	12-Bit Resistance ladders. output switch(DAOE switch resistance)	VDDA=2.4V 0.5V < DAO < VDDA-0.5V			200	Ω
		VDDA=2.4V 0.5V > DAO , DAO > VDDA-0.5V		10		Ω
R_{RSW}	Reference voltage switch(Vrefp switch resistance, Vrefn switch resistance)	V_{REFP} = 2.2V, V_{REFN} = 0V, VDDA = 2.4V		15	30	Ω
R_{LADDER}	One LSB resistance ladder		170	200	230	Ω
INL	Integral linearity error	VR+ = 2.4V, VR- = 0V (After compensation)		±3		LSB
DNL	Differential linearity error	VR+ = 2.4V, VR- = 0V (After compensation)			±1	LSB
E_{OS}	Offset error	VR+ = 2.4V, VR- = 0V			1	LSB
12-Bit Resistance Ladders.	(Vin Floating)	VDD3V=3.3V,VDDA=2.4V		0.1		uA

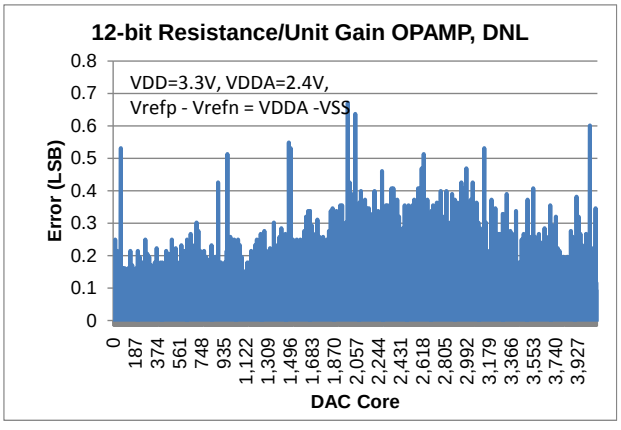


Figure5.9-1 12-Bit Resistance DNL

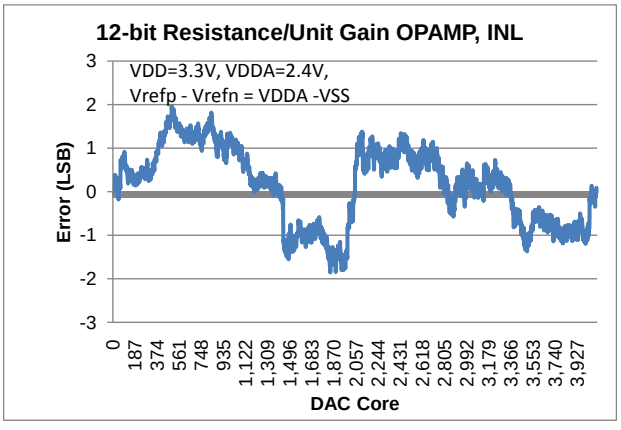


Figure5.9-2 12-Bit Resistance INL

5.10 Rail-to-rail OPAMP Management System

Typical values are at T_A=25℃, VDD3V = 3.0V, and C_{VLCD}=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power supply		2.4		3.6	V
V_{OUT}	Output range		0		VDDA	V
V_{IN}	Input common range		0		VDDA	V
I_{OPA}	OPAMP current			120		uA
I_{OPA_LOAD}	Output current loading (push or pull)	VDDA = 3.0V, 0.3V< Output voltage <VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V< Output voltage <VDDA-0.3V			0.5	mA
C_{LOAD}	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V to VDDA-0.3V		0.6		V/us
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V_{OS}	Offset error	Vin = 1.2V	-5		+5	mV
DFD	Digital filter delay	VDDA = 3.0V		2		us
C_{SA}	Sample capacitor			10		pF

5.11 LVD Comparator Management System

Typical values are at TA=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LVD	Operation current, I_{V12_BOR}			1		uA
	Operation current, I_{V12_BGR}			10		uA
	V12_BOR Reference Voltage		1.1	1.2	1.3	V
	V12_BOR Reference Voltage Temperature drift			50		PPM/℃
	V12_BOR Reference Voltage to VDD3V Voltage drift			±2		%/V
	V12_BGR Reference Voltage		1.15	1.2	1.25	V
	V12_BGR Reference Voltage Temperature drift			50		PPM/℃
	V12_BGR Reference Voltage to VDD3V Voltage drift			±0.2		%/V
	Compare reference voltage temperature drift, T_A = -40℃ ~ 85 ℃			50		ppm/℃
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1111b			3.4		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1110b			3.3		V
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1101b			3.2		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1100b			3.1		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1011b			3.0		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1010b			2.9		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1001b			2.8		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=1000b			2.7		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0111b			2.6		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0110b			2.5		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0101b			2.4		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0100b			2.3		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0011b			2.2		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0010b			2.1		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0001b			2.0		
	Detect V_{DD3V} voltage rang by user option, V_{SVS} VLDS [3:0]=0000b			LVDIN		
LVD：Low Voltage Detect						

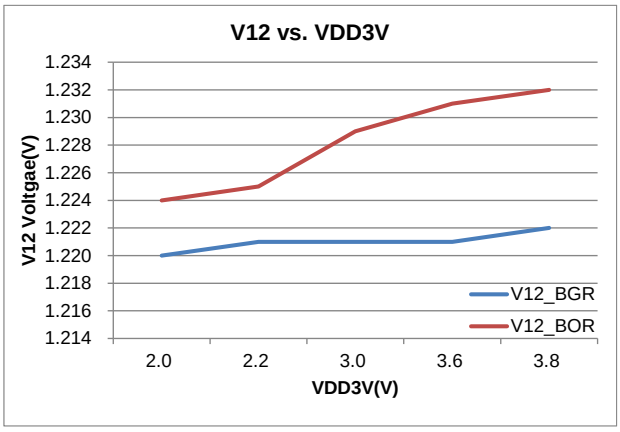


Figure5.11-1 V12 vs. VDD3V

5.12 LCD System

Typical values are at T_A=25℃, VDD3V = 3.3V, and C_{VLCD}=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LCD}	Operation Current Charge Pump Mode		W/O Panel		10		uA
VLCD	Supply Voltage Range	VLCD	With Buffer	2.50		3.80	V
VLCD	Embedded Charge Pump Output Voltage @ VLCD Pin	VDD3V = 2.4V CVLCD = 10uF	Mode1: Data[1]=00_011B (After trim) Note1	-5%	3.43	+5%	V
			Mode1: Data[1]=00_011B	-10%	3.30	+10 %	
			Mode2: Data[1]=00_100B (After trim) Note1	-5%	3.16	+5%	
			Mode2: Data[1]=00_100B	-10%	3.00	+10 %	
			Mode3: Data[1]=00_101B (After trim) Note1	-5%	2.93	+5%	
			Mode3: Data[1]=00_101B	-10%	3.00	+10 %	
			Mode4: Data[1]=11_101B (After trim) Note1	-5%	2.73	+5%	
			Mode4: Data[1]=11_101B	-10%	2.80	+10 %	
			Mode5: Data[1]=01_101B (After trim) Note1	-5%	2.55	+5%	
			Mode5: Data[1]=01_101B	-10%	2.6	+10 %	
Z_{LCD}	Output Impedance With LCD Buffer	F_{LCD} = LS_CK/32/9, VLCD = 3.16V			10		KΩ

Data1 Bit: 0X41B10 [EN_Rshift1, EN_Rshift0], 0X41B00 [VLCD2, VLCD1, VLCD0]
Note1 :
After Trim : According to the factory calibration parameters of VLCD to calibrate VLCD, and need to corresponding to the selected VLCD voltage. User can refer to the document “UG-HY16F3981_TC” to know how to use that in detail.

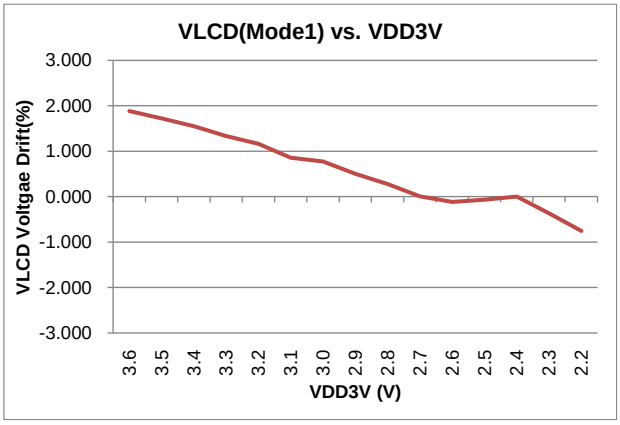


Figure5.12-1 VLCD(Mode1) vs. VDD3V

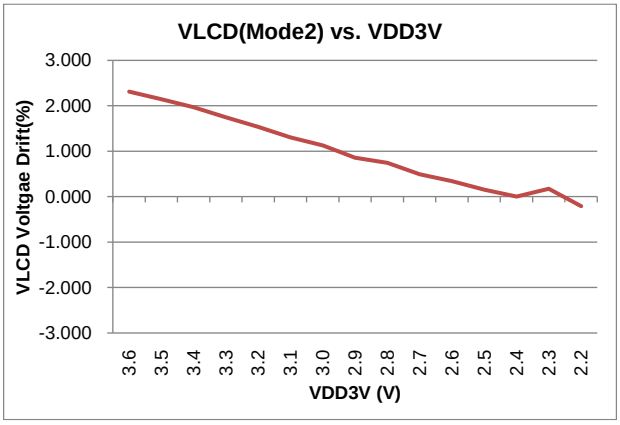


Figure5.12-2 VLCD(Mode2) vs. VDD3V

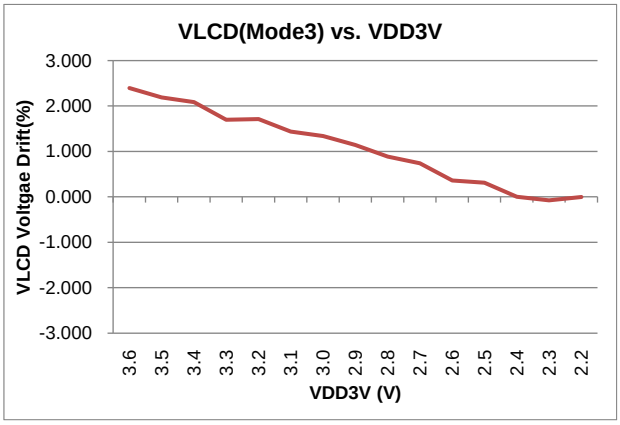


Figure5.12-3 VLCD(Mode3) vs. VDD3V

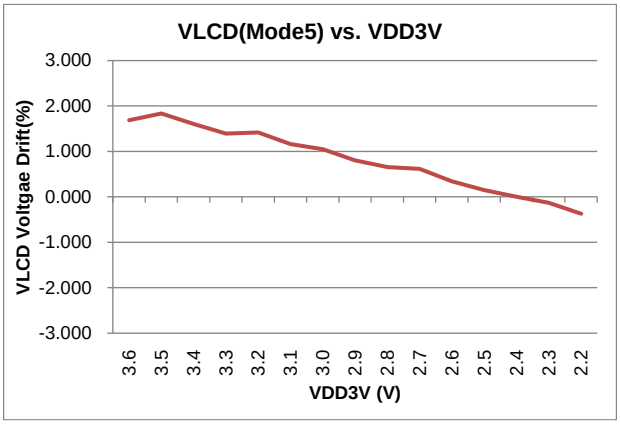


Figure5.12-5 VLCD(Mode5) vs. VDD3V

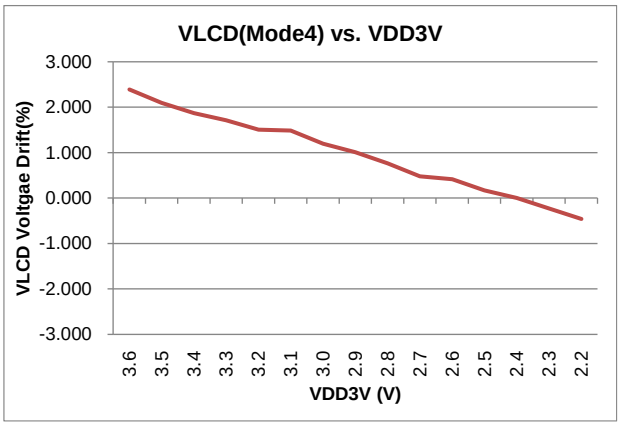


Figure5.12-4 VLCD(Mode4) vs. VDD3V

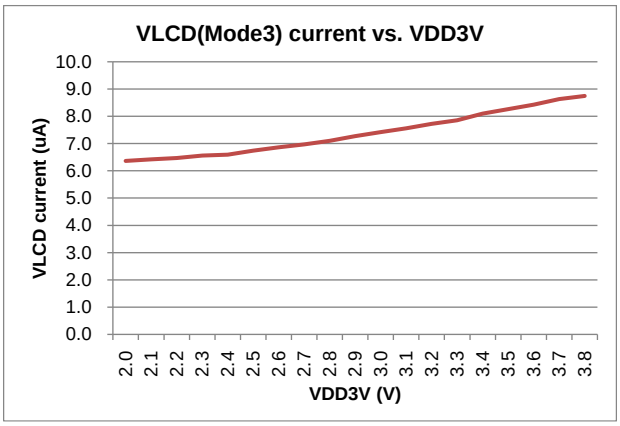


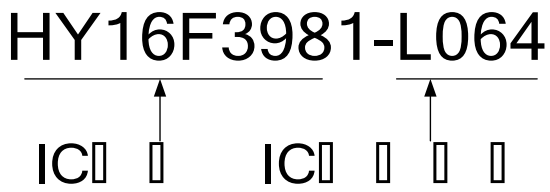
Figure5.12-6 VLCD current vs. VDD3V

6. 订货信息

6.1 HY16F3981 系列选型编码

下单品名 [1]	封装型式	引脚数	封装型式描述方式		程序代码编号 [2]	出货包装形式	个装数量	材料组成	MSL [3]
HY16F3981-D000	Die	-	D	000	-	-		Green[4]	-
HY16F3981-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F3981-E028	SSOP	28	E	028	000	Tube	48	Green4	MSL-3
HY16F3981-E028	SSOP	28	E	028	000	Tape & Reel	2000	Green4	MSL-3

[1] 下单品名: 描述的内容为：芯片型号 – 芯片封装型式



EX：你需求的是 LQFP 64 引脚封装. 下单品名就是 HY16F3981-L064.
当需要以 Tray 出货，在下订单时除下单品名外，请清楚指明出货包装形式为 Tray.

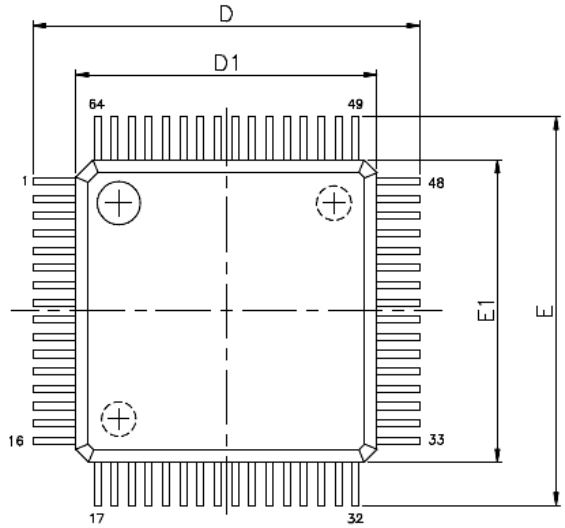
[3] MSL:
湿敏度等级符合 IPC/JEDEC J-STD-020 的行业分类工业标准.
产品的加工、包装、运输及使用都参考 IPC/JEDEC J-STD-033 行业标准.

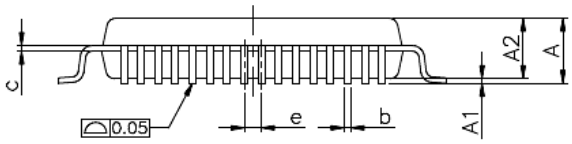
[4] Green (RoHS & no Cl/Br):
HYCON 产品皆为 Green Product，符合 RoHS 指令以及无卤素规定(Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)

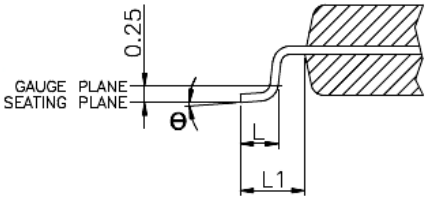
7. 封装尺寸信息

7.1 LQFP 7x7 64L(L064) 封装图

7.1.1 Package Dimensions







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

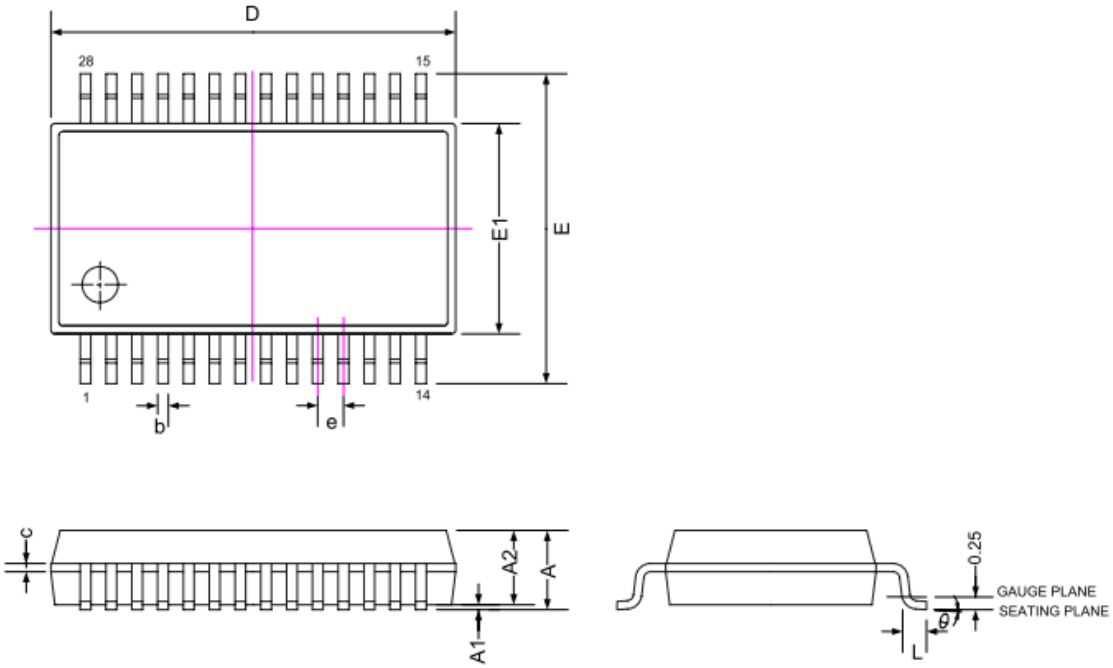
SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

7.2 SSOP28(209mil) 封装图

7.2.1 Package Dimensions



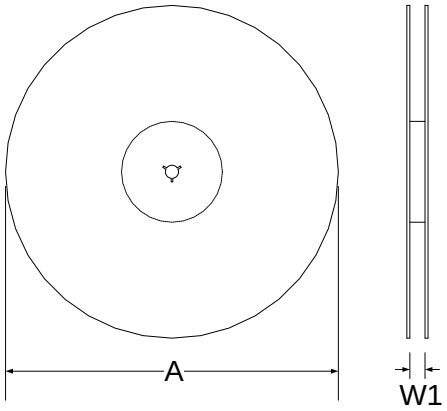
SYMBOLS	MIN	NOM	MAX
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	10.05	10.20	10.50
E1	5.00	5.30	5.60
E	7.65	7.80	7.90
L	0.55	0.75	0.95
e	0.65 BASIC		
θ°	0	4	8

Note:

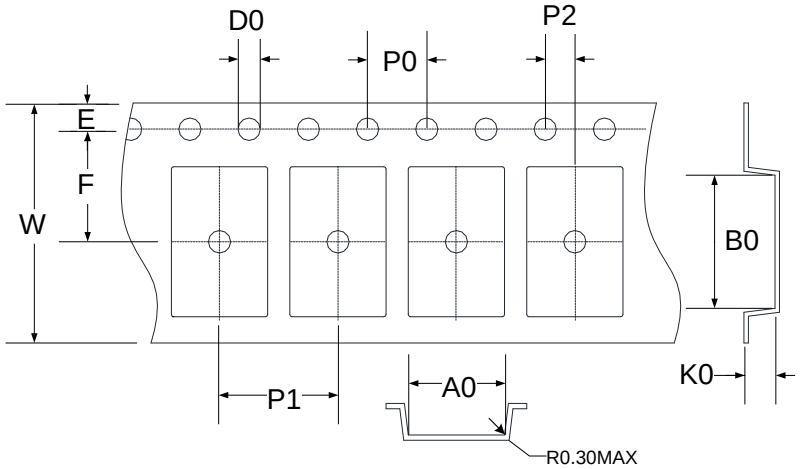
1. All dimensions refer to JEDEC OUTLINE MO-150.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

7.2.2 Tape & Reel Information

7.2.2.1 Reel Dimensions



7.2.2.2 Carrier Tape Dimensions

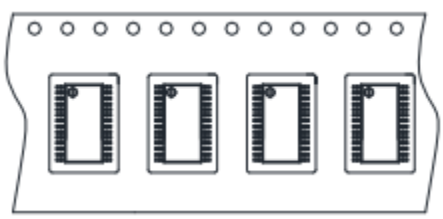


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	24.5	8.40	10.65	2.40	4.00	12.00	2.00	1.75	11.50	1.50	24.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	+0.1/-0	±0.30

Unit: mm

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

7.2.2.3 Pin1 direction



8. 修改记录

以下描述本文件差异较大的地方，而标点符号与字形的改变不在此描述范围。

版本	页数	变更摘要
V01	All	初版发行
V02	P12	E028, PIN7 为 PT7.2
	P37~P38	新增图表 Sleep / Idle / HAO Free Run(2M/4M/10M/16M) Current vs. VDD3V
	P50	新增图表 V12 vs. VDD3V
	P51	新增图表 VLCD Current vs. VDD3V
V03	All	新增各图表以及更新电器规格
V05	All	1.移除 PT3.2/PT3.3 脚位的 GPIO 复用功能，该脚位只保留 AIO4/AIO5 模拟功能. 2.修改 5.5 章节 RPU 参数规格(并且增加上下限) 3.新增 5.9 章节 RLADDER 参数规格(上下限) 4.修改 12-bit Resistance Ladder 网络图与增加电气规格说明 5.修正 ADC 网络图(ADCLK 更名为 ADCK) 6.修正 ADC ENOB(RMS)与 RMS noise Table 表
V06	All	1. 新增 SSOP28 无支持 LCD 功能的红外线传感器与血压计传感器应用参考线路 2. 移除硬件 I2C 功能描述，硬件 I2C 功能不开放使用
V07	All	1. 新增说明 Flash 闪存特性 2. 新增说明 VLCD 可透过校正函数提供 5 段 VLCD 偏压 3. 新增说明 VDDA Voltage 1~4 的寄存器控制说明 4. 修正应用电路图，连接外部 EEPROM 的引脚只需要连接外部上拉电阻,不需要接 GND. 5. 修正 IR 应用电路, Thermistor 线路, Rf 参考电阻为 100k, 分压电阻为 300k, REFO 新增设计可切换 Switch 开关短路到 AI1. 6. 修正 LVD 方块图，并且修正 LVDS 电气规格描述. 7. 新增 PT3.2/PT3.3 脚位的 GPIO 复用功能，该引脚可以工作于数字与模拟复用功能. 8. 新增硬件 I2C 功能 9. 新增 Note1 在 ADC 电气特性章节，说明 ADC 差动输入范围限制.

		10. Timer B 方块图的 TBCLK 修正为 TBCK, TMBC0/TMBC1/TMBC2 修正为 TBC0/TBC1/TBC2, ENTMB 修正为 TBEN. 11. Timer B2 方块图的 TBCLK 修正为 TB2CK, TMB2C0/TMB2C1/TMB2C2 修正为 TB2C0/TB2C1/TB2C2, ENTMB2 修正为 TB2EN. 12. Timer C 方块图的 ENTMC 修改为 TCEN.