HY17P48

Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 18-Bit ΣΔADC and 8x7 LED Driver

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1. Features

- 8-Bit RISC-like microcontrollers with 71 high-performance instruction set H08D (same as H08A),support C compiler
- Operating voltage and operating temperature range
  - V_{DD} : 2.2V ~ 5.5V
  - V_{DDA} : 2.4V ~ 4.5V
  - - 40°C ~ 85°C
- External Crystal Oscillator and Internal High Precision RC Oscillator, Many CPU clock rates enable users to have the most power-saving plan.
- Memory
  - 8K words OTP program memory
  - 512 bytes data memory
- Reset
  - Power On Reset
  - Brown Out Reset
  - Watch Dog Reset
  - Stack Over Reset
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function
- VDDA can select 7 different output voltages that equip with 10mA low dropout regulator function.
- 8 GPIO Supported Constant Current Control Circuits
  - Source current 2~15mA
  - Sink current 80mA
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function
- VDDA can select 7 different output voltages that equip with 10mA low dropout regulator function.
- 8 GPIO Supported Constant Current Control Circuits
  - Source current 2~15mA
  - Sink current 80mA
- 24-Bit ΣΔADC
  - Built-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x，10 input signal gain selection
  - Zero point bias translation controller
  - Sampling frequency 1MHz
  - Settable over-sampling rate is 64~65536
  - Diverse data output rate. Max. 15.6Ksps
  - Built-in absolute temperature sensor
- Timer
  - Watch Dog
    - Reset event
    - Interrupt event
  - 2 channels 8-bit Timer
    - Interrupt event
    - Compare events
  - 1 channel 16-bit Timer
    - 16-Bit PWM output
    - Two 8-Bit PWM output
    - Interrupt event
  - Time C Capture/Compare funtion
- 64 words Built-In EPROM (BIE), 2.75V low voltage programming control circuit
- Interface
  - 2 channels serial communication EUART module
  - 2 channels I2C communication (Master/Slave mode) module
  - 1 channel SPI module
- Package
  - SSOP28, SSOP20, QFN32

2. Pin Definition

2.1. Pin Diagram

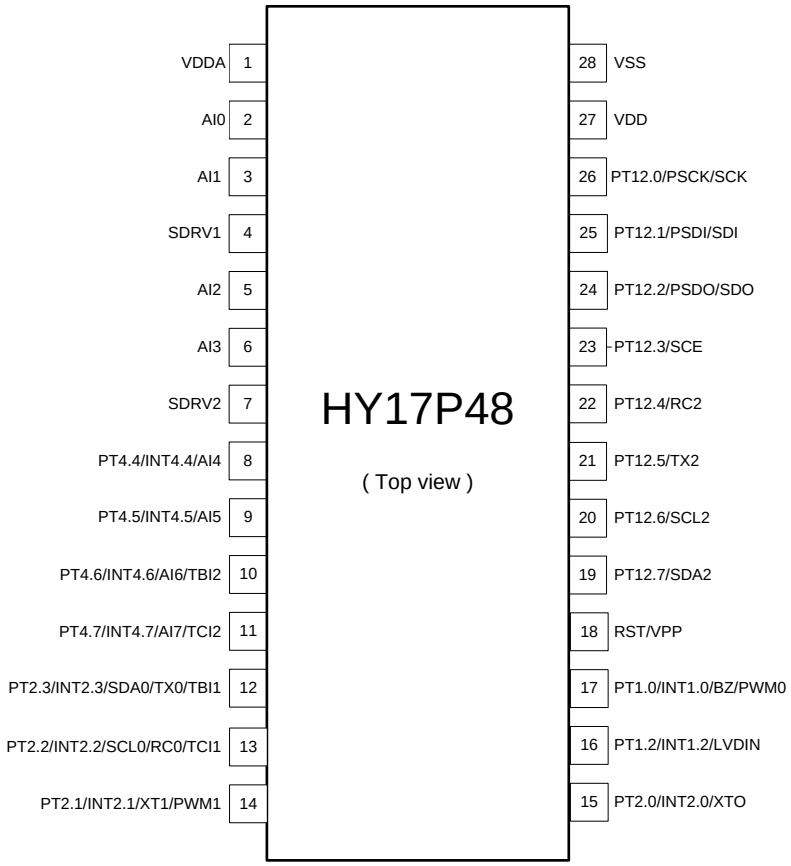


Figure 2-1 HY17P48 SSOP28 Diagram

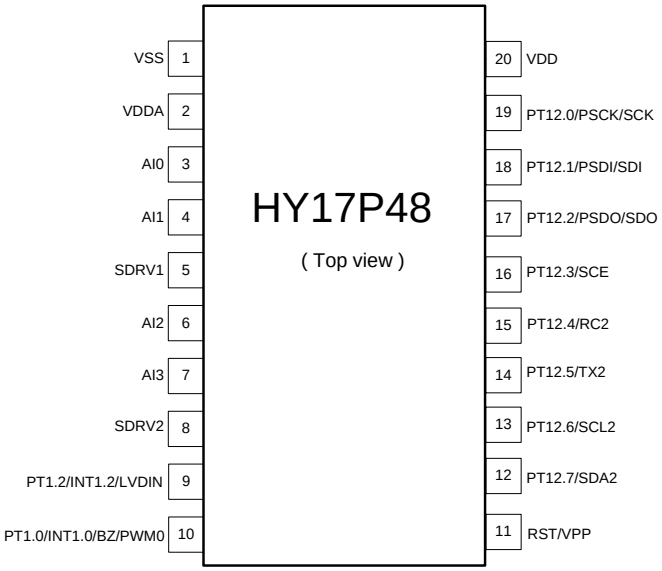


Figure 2-2 HY17P48 SSOP20 Diagram

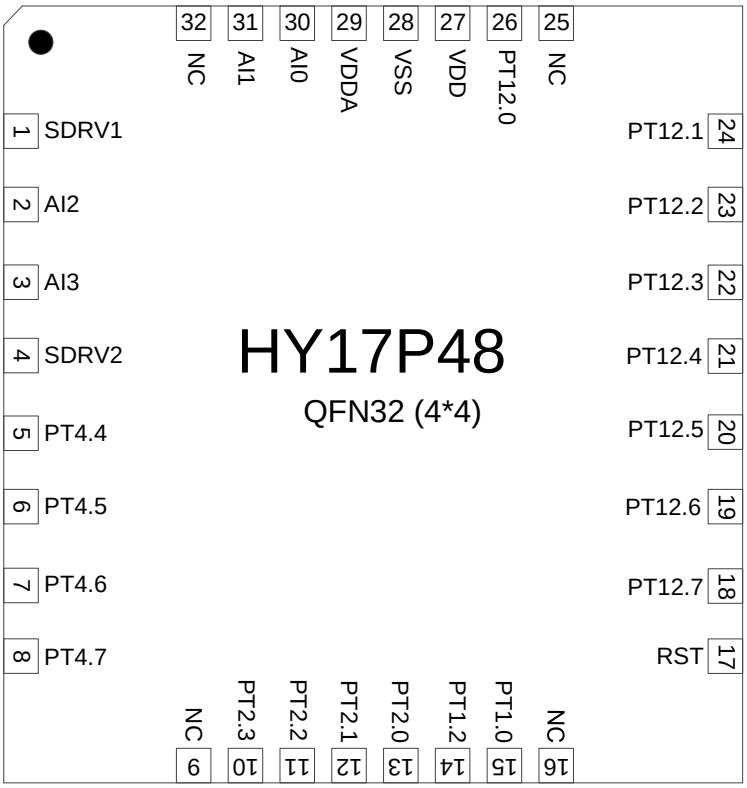


Figure 2-3 HY17P48 QFN32 Diagram

2.2. Pin Description

"I" : Input ,"O" : Output, "A" : Analog, "S" : Smith triggers, "C" : CMOS I/O,"P" : Power Source,"/" : or ,"X" : Ignorable

Pin No.			Pin Name	Characteristic		Description
SSOP20	SSOP28	QFN32		Type	Buffer	
2	1	29	VDDA	P	P	LDO output · Analog power (source: from VDD)
3	2	30	AI0	A	A	Analog input channel
4	3	31	AI1	A	A	Analog input channel
5	4	1	SDRV1	O	P	Sensor power
6	5	2	AI2	A	A	Analog input channel
7	6	3	AI3	A	A	Analog input channel
8	7	4	SDRV2	O	P	Sensor power
-	8	5	PT4.4/INT4.4/AI4			
			PT4.4	I	S	Digital input pin
			INT4.4	I	S	External interrupt source INTF4.4
			AI4	A	A	Analog input channel
-	9	6	PT4.5/INT4.5/AI5			
			PT4.5	I	S	Digital input pin
			INT4.5	I	S	External interrupt source INTF4.5
			AI5	A	A	Analog input channel
-	10	7	PT4.6/INT4.6/AI6/TBI2			
			PT4.6	I	S	Digital input pin
			INT4.6	I	S	External interrupt source INTF4.6
			AI6	A	A	Analog input channel
			TBI2	I	S	TimerB Enable input
-	11	8	PT4.7/INT4.7/AI7/TCI2			
			PT4.7	I	S	Digital input pin
			INT4.7	I	S	External interrupt source INTF4.7
			AI7	A	A	Analog input channel
			TCI2	I	S	TimerC clock source input port
-	12	10	PT2.3/INT2.3/SDA0/TX0 /TBI1			
			PT2.3	I/O	S/C	Digital input / Output pin
			INT2.3	I	S	External interrupt source INTF2.3
			SDA0	I/O	S	I^2C communication data pin
			TX0	O	S	TX pin of EUART interface
			TBI1	I	S	TimerB Enable input

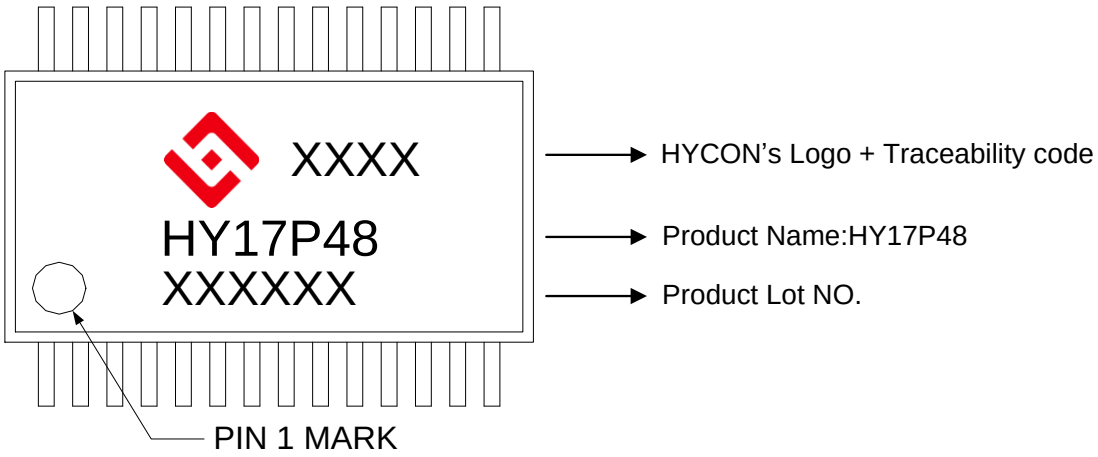
Pin No.			Pin Name	Characteristic		Description
SSOP20	SSOP28	QFN32		Type	Buffer	
			PT2.2/INT2.2/SCL0/RC0 /TCI1			
-	13	11	PT2.2	I/O	S/C	Digital input / Output pin
			INT2.2	I	S	External interrupt source INTF2.2
			SCL0	I/O	S	I^2C communication clock pin
			RC0	I	S	RC pin of EUART interface
			TCI1	I	S	TimerC clock source input port
			PT2.1/INT2.1/XTI/PWM1			
-	14	12	PT2.1	I/O	S/C	Digital input / Output pin
			INT2.1	I	S	External interrupt source INTF2.1
			XTI	A	A	External oscillator input
			PWM1	O	C	PWM1 out port
			PT2.0/INT2.0/XTO			
-	15	13	PT2.0	I/O	S/C	Digital input / Output pin
			INT2.0	I	S	External interrupt source INTF2.0
			XTO	A	A	External oscillator output
			PT1.2/INT1.2/LVDIN			
9	16	14	PT1.2	I/O	S/C	Digital input / Output pin
			INT1.2	I	S	External interrupt source E2IF
			LVDIN	A	A	LVD external signal input port
			PT1.0/INT1.0/BZ/PWM0			
10	17	15	PT1.0	I/O	S/C	Digital input / Output pin
			INT1.0	I	S	External interrupt source E0IF
			BZ	O	C	Buzzer output
			PWM0	O	C	PWM0 out port
			RST/VPP			
11	18	17	RST	I	S	IC Reset Pin
			VPP	P	P	OTP burning voltage source input pin
			PT12.7/SDA2			
12	19	18	PT12.7	I/O	S/C	Digital input / Output pin
			SDA2	I/O	S	I^2C communication data pin
			PT12.6/SCL2			
13	20	19	PT12.6	I/O	S/C	Digital input / Output pin
			SCL2	I/O	S	I^2C communication clock pin
14	21	20	PT12.5/TX2			

Pin No.			Pin Name	Characteristic		Description
SSOP20	SSOP28	QFN32		Type	Buffer	
			PT12.5	I/O	S/C	Digital input / Output pin
			TX2	O	S	TX pin of EUART interface
15	22	21	PT12.4/RC2			
			PT12.4	I/O	S/C	Digital input / Output pin
			RC2	I	S	RC pin of EUART interface
16	23	22	PT12.3/SCE			
			PT12.3	I/O	S/C	Digital input / Output pin
			SCE	I	S	SPI interface SCE
17	24	23	PT12.2/PSDO/SDO			
			PT12.2	I/O	S/C	Digital input / Output pin
			PSDO	O	S	OTP read / write interface pin, PSDO
18	25	24	PT12.1/PSDI/SDI			
			PT12.1	I/O	S/C	Digital input / Output pin
			PSDI	I	S	OTP read / write interface pin, PSDI
19	26	26	PT12.0/PSCK/SCK			
			PT12.0	I/O	S/C	Digital input / Output pin
			PSCK	I	S	OTP read / write interface pin, PSCK
			SCK	I/O	S	SPI interface pin, SCK
20	27	27	VDD/VDD1	P	P	Power input for system · External 1~10uF capacitor to VSS.
1	28	28	VSS/VSS1	P	P	System Power Ground
-	-	9 16 25 32	NC	-	-	Unused pins, Not Connect

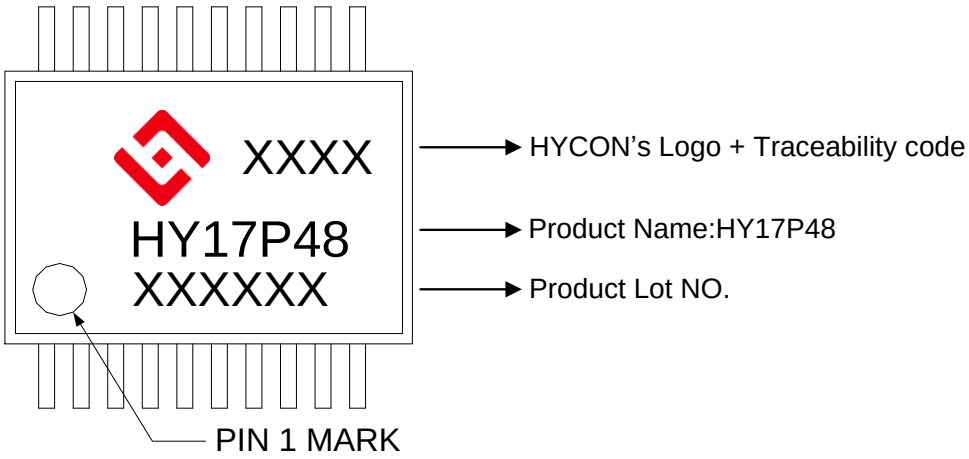
Table 2-1 Pin Definition and Function Description

2.3. Package marking information

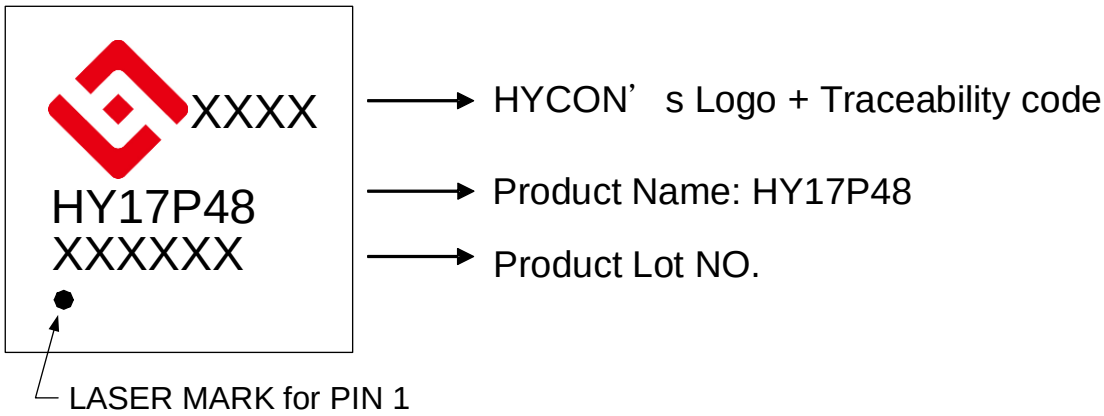
2.3.1. SSOP28 Package marking information



2.3.2. SSOP20 Package marking information



2.3.3. QFN32 Package marking information



3. Application Circuit

3.1. Bridge Sensor with 8x7 LED display

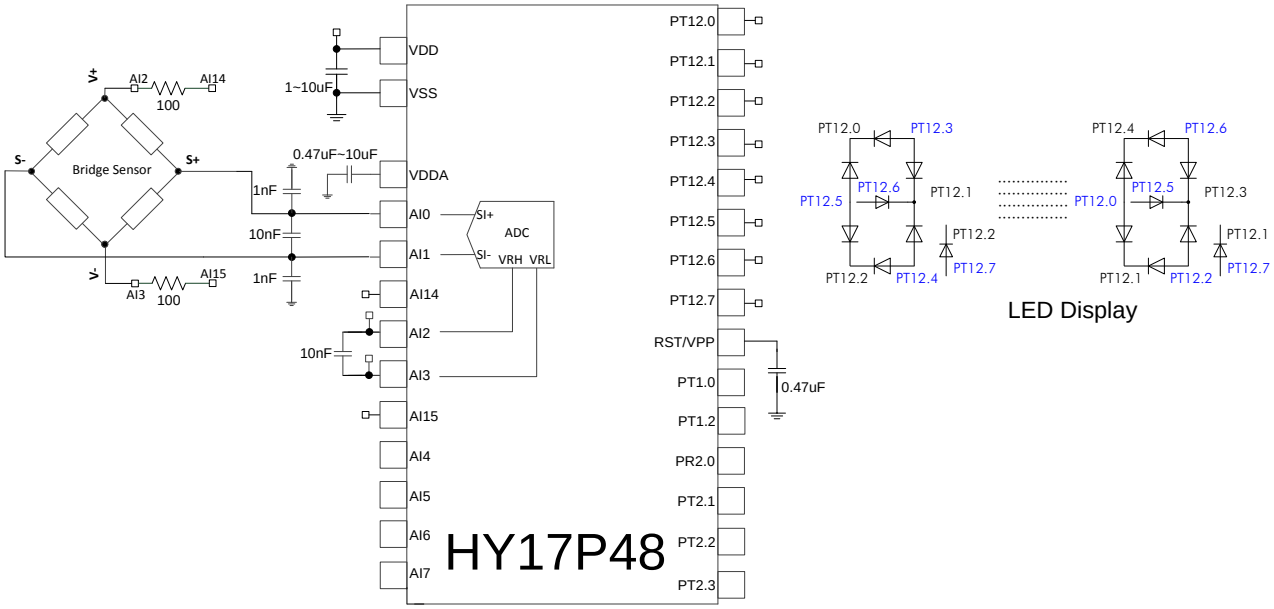


Figure 3-1 Bridge Sensor application reference circuit

4. Function Outline

4.1. Internal Block Diagram

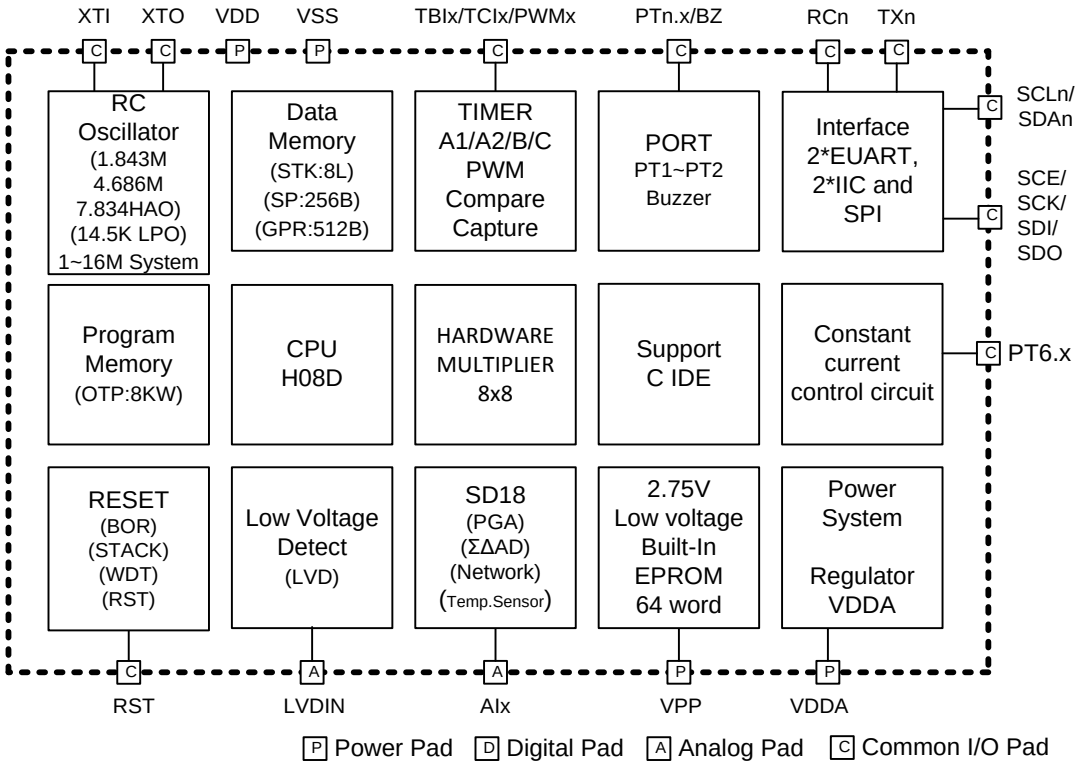


Figure 4-1 Internal Block Diagram

4.2. Related Description and Supporting Document

File Name	Description
DS-HY17P48	HY17P48 Datasheet
UG-HY17P48	HY17P48 User guide
APD-CORE005	H08D instruction manual
APD-HY17PIDE001	HY17P Series development tool software user manual
APD-HY17PIDE002	HY17P Series development tool hardware user manual
APD-OTP00X	OTP PIN manual
APD-HY17PIDE003	HY17P Series HexLoader user manual
APD-HY17PIDE004	HY10000-WK08C Integrated writer user manual
BDI-HY17P48	HY17P48 Bonding information

4.3. Clock System

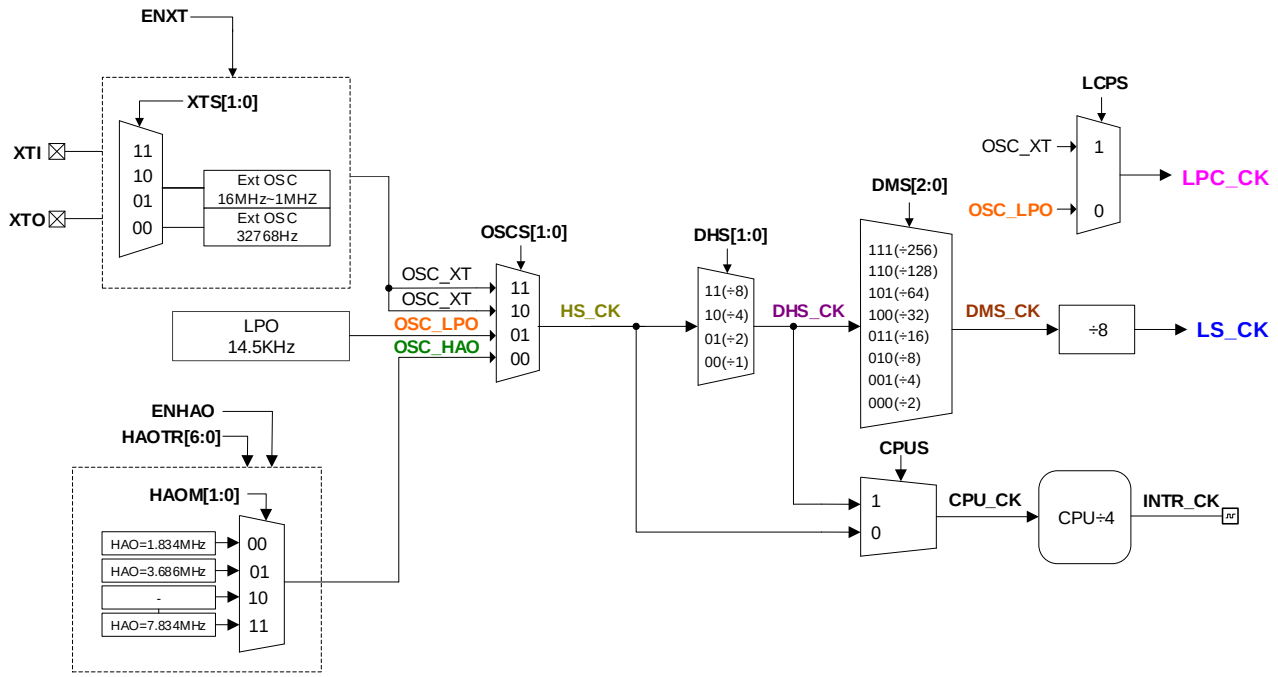


Figure 4-2 Clock System block diagram (1)

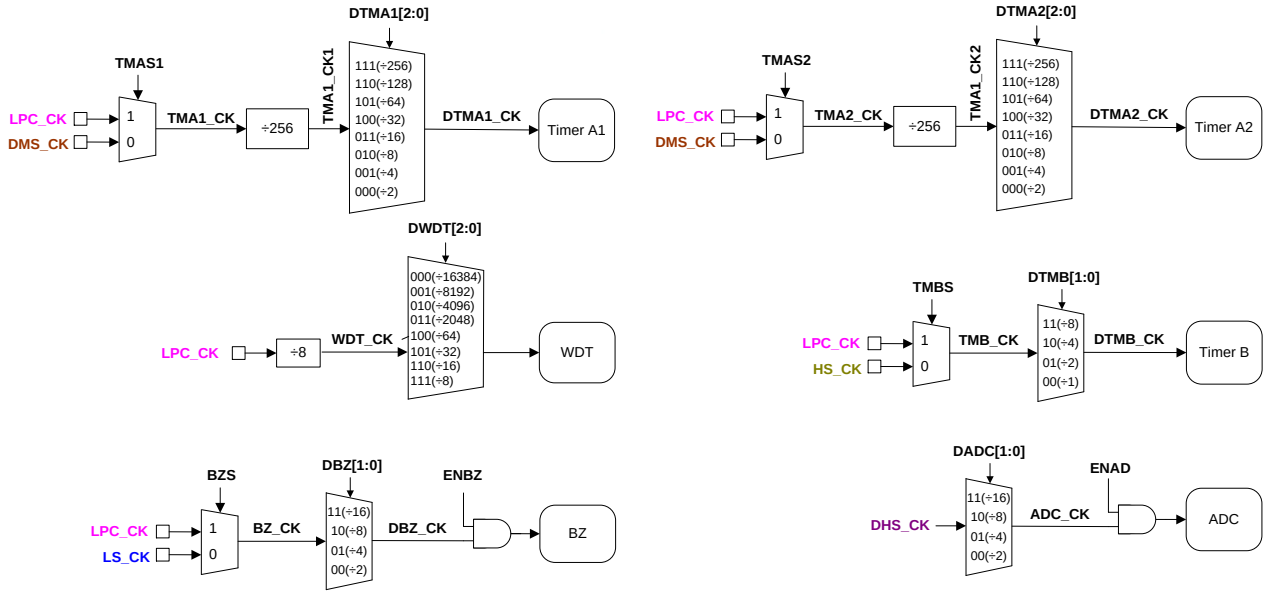


Figure 4-3 Clock System block diagram (2)

4.4. Low Voltage Detect(LVD)

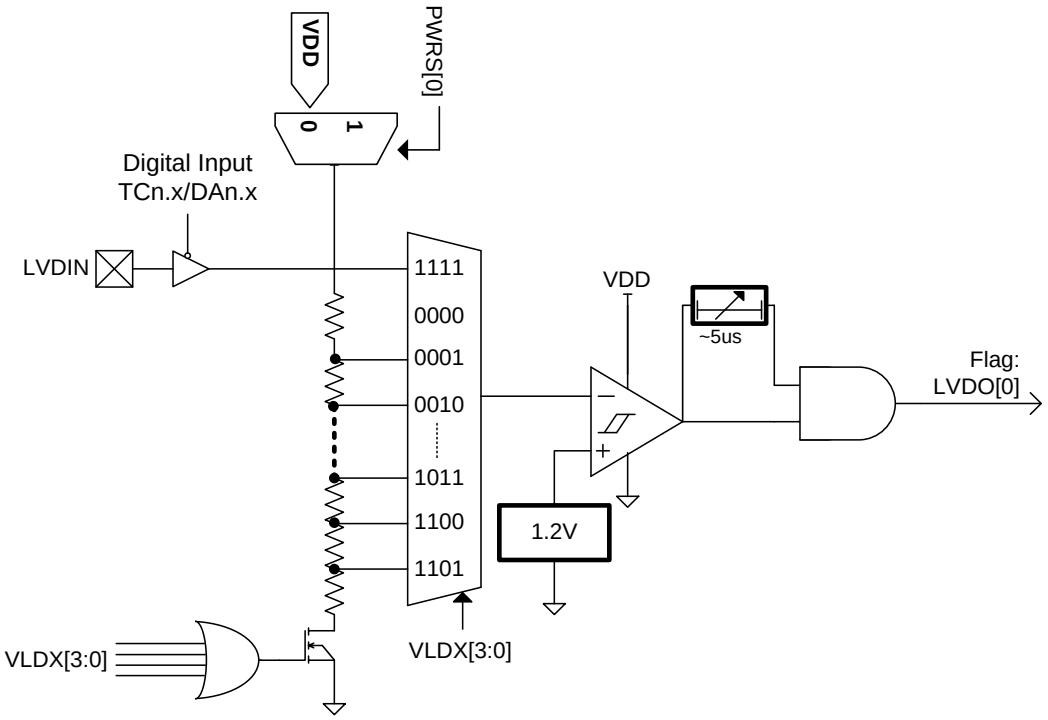


Figure 4-4 Low Voltage Detect block diagram

4.5. Reset

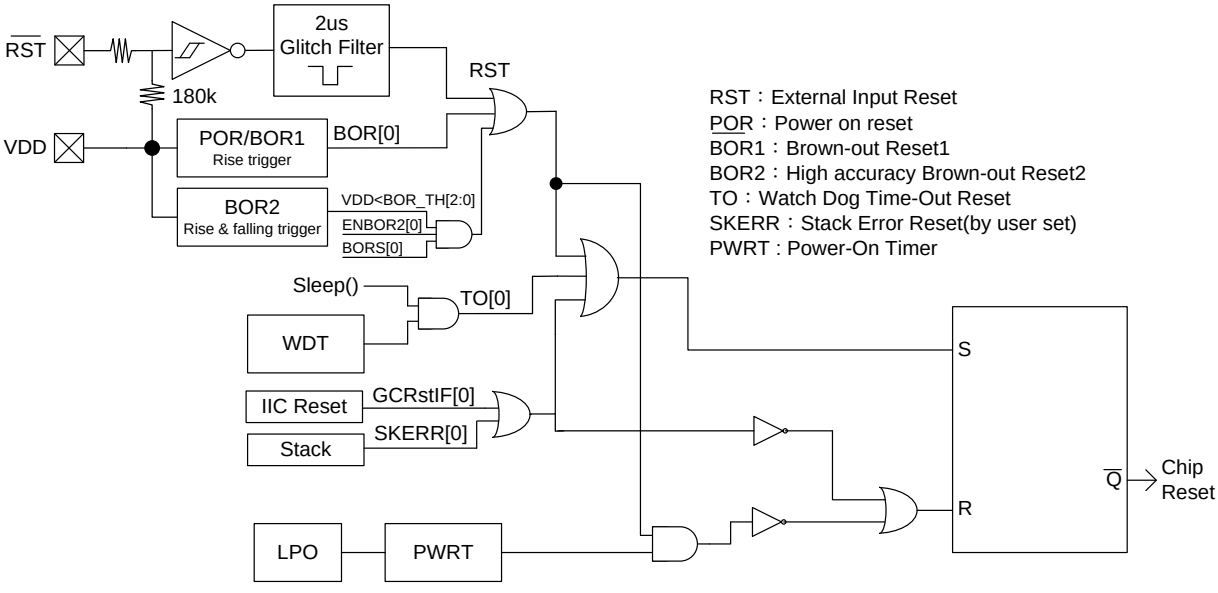


Figure 4-5 Reset block diagram

4.6. Power System

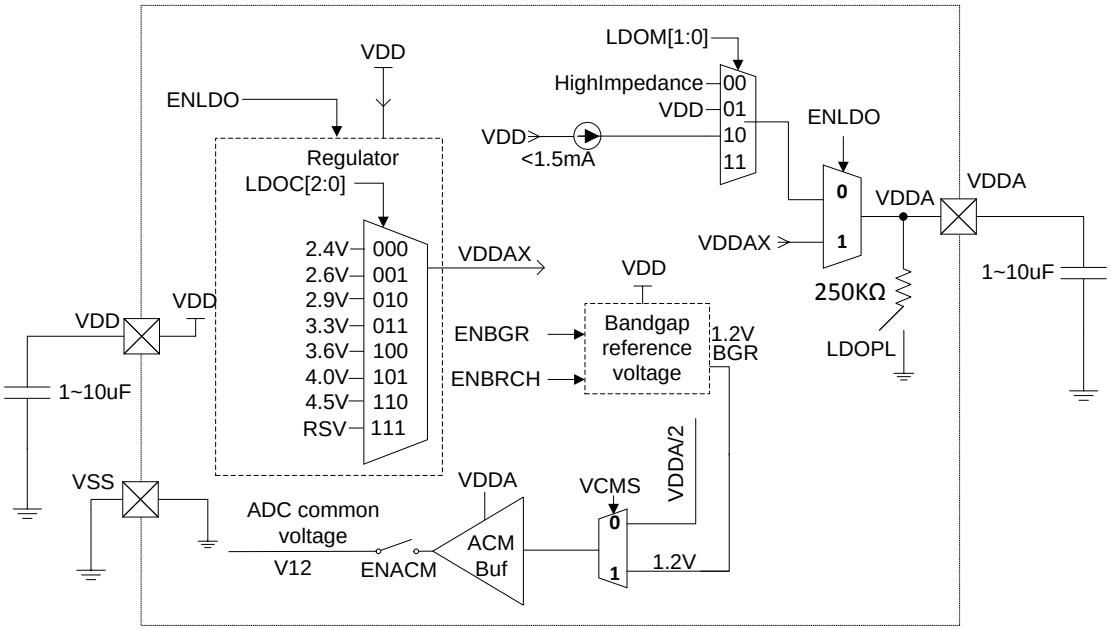
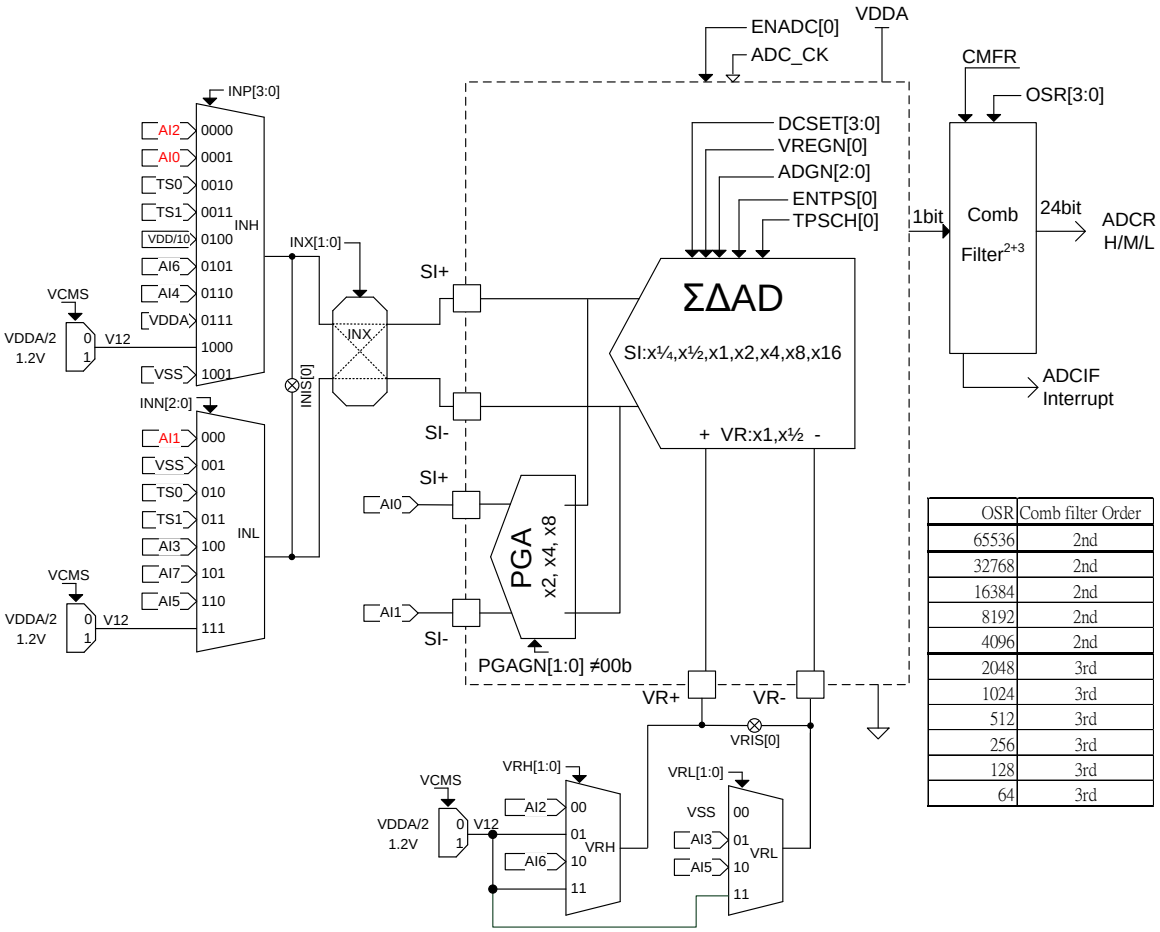


Figure 4-6 Power System block diagram

4.7. ΣΔADC Network



OSR	Comb filter Order
65536	2nd
32768	2nd
16384	2nd
8192	2nd
4096	2nd
2048	3rd
1024	3rd
512	3rd
256	3rd
128	3rd
64	3rd

Figure 4-7 SD18 Network

4.8. GPIO PT1、2、4、12

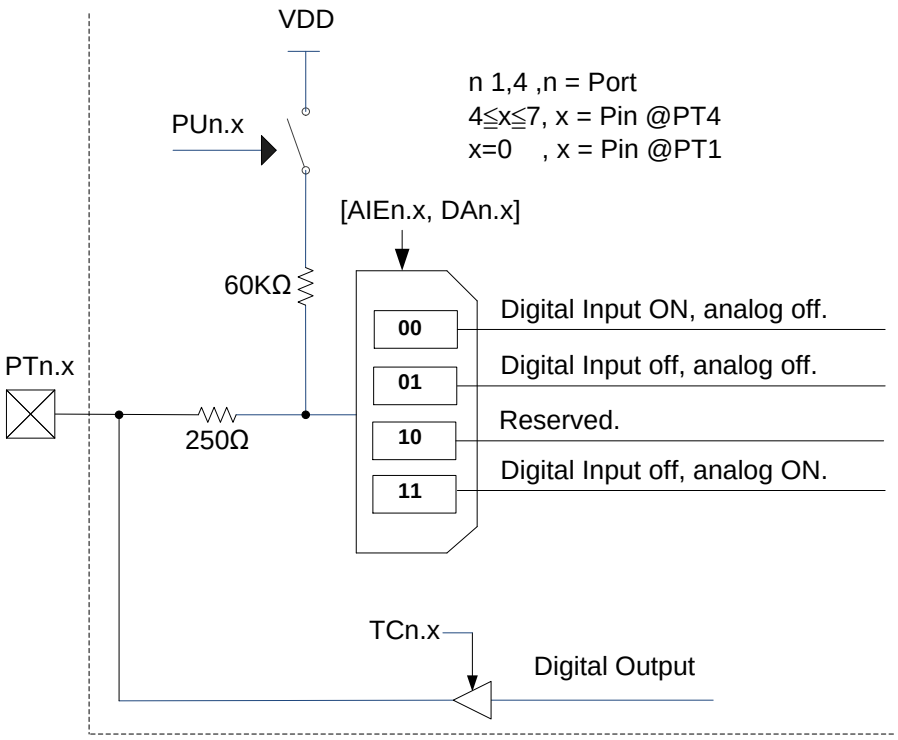


Figure 4-8 PT1、PT4GPIO block diagram

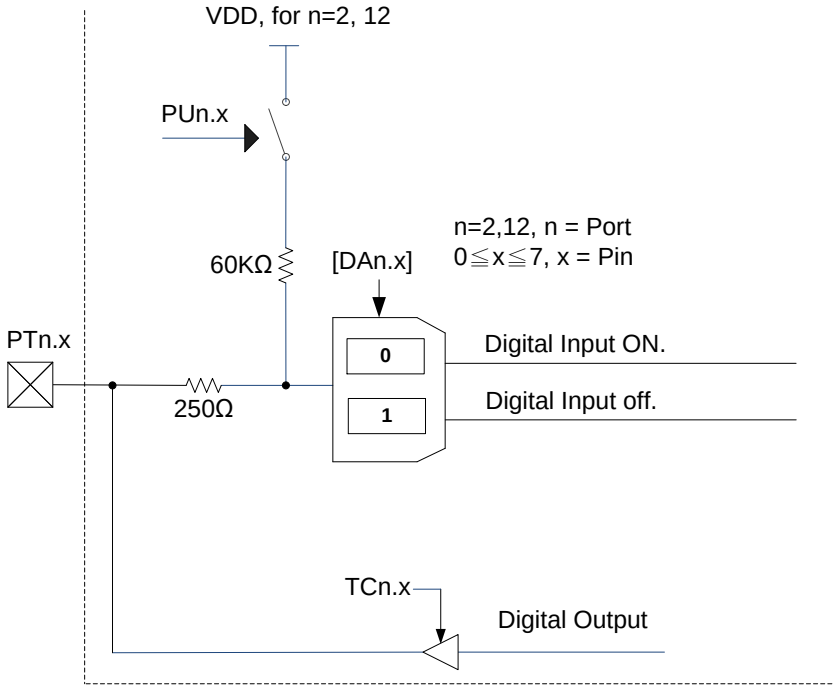


Figure 4-9 PT2、PT12GPIO block diagram

4.9. Watch Dog System

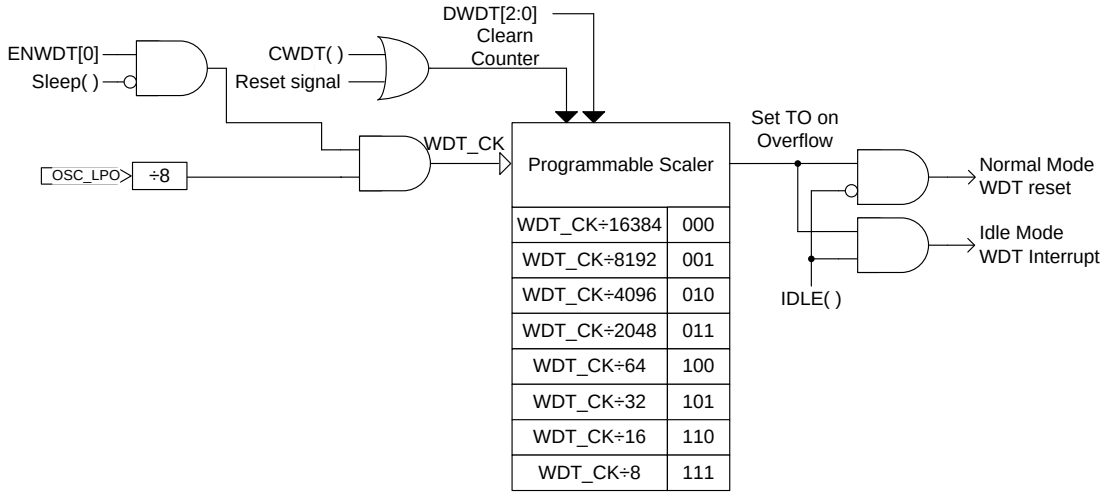


Figure 4-10 Watch Dog block diagram

4.10. 8-bit Timer A1 System

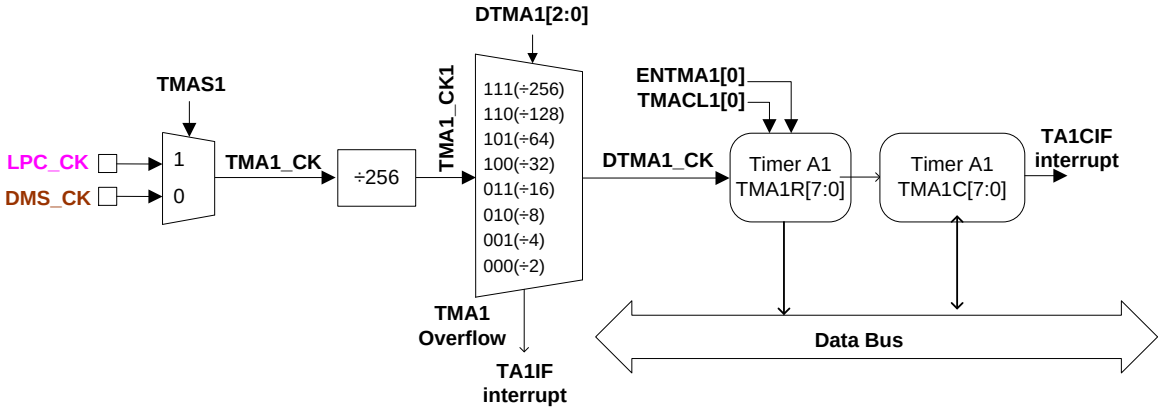


Figure 4-11 8-bit Timer A1 block diagram

4.11. 8-bit Timer A2 System

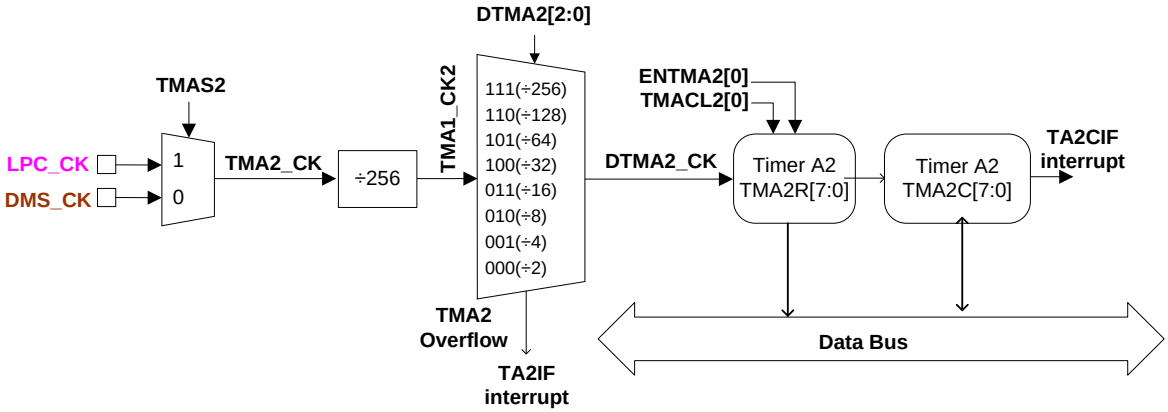


Figure 4-12 8-bit Timer A2 block diagram

4.12. 16-bit Timer B System

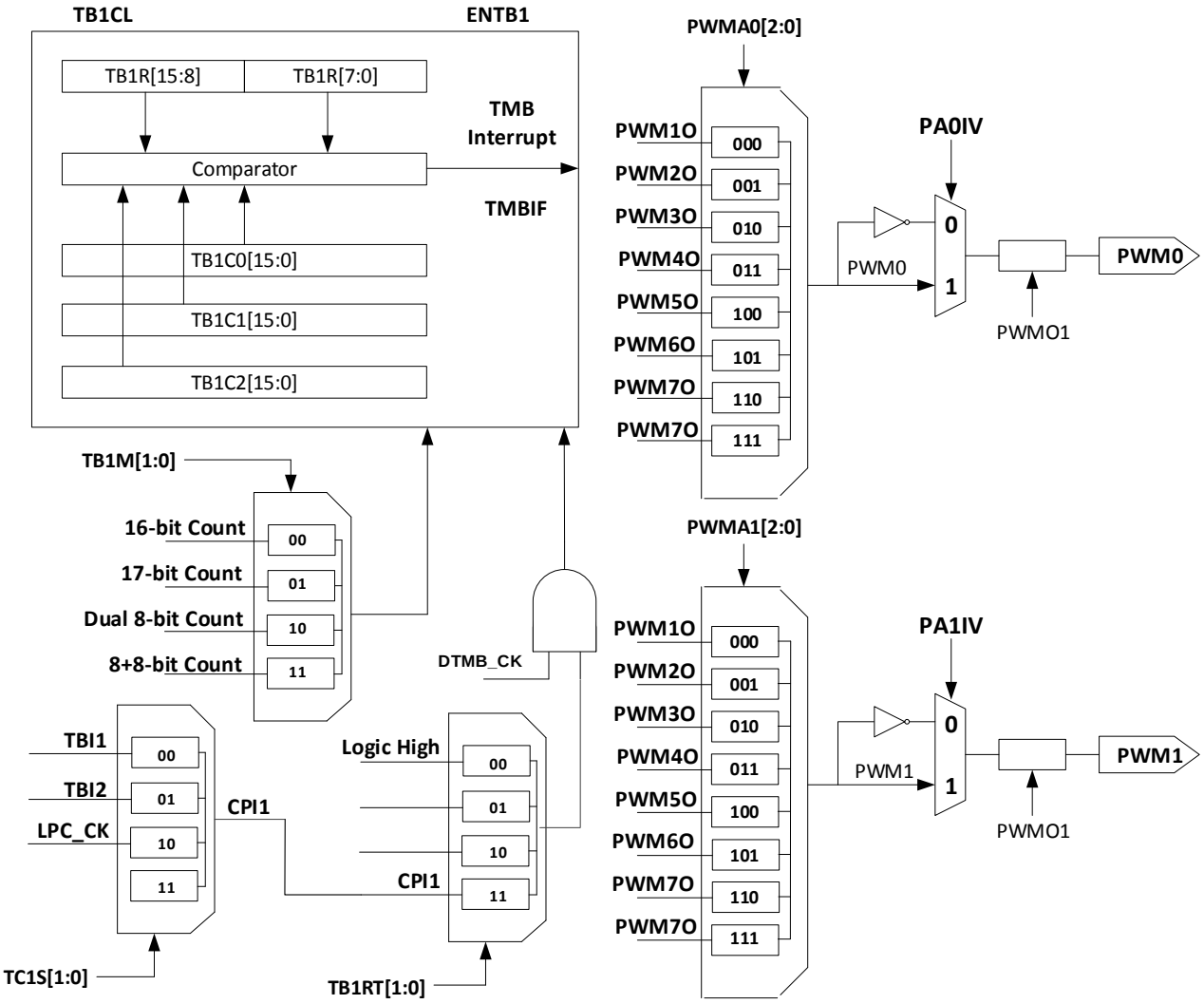


Figure 4-13 16-bit Timer B block diagram

4.13. Time C

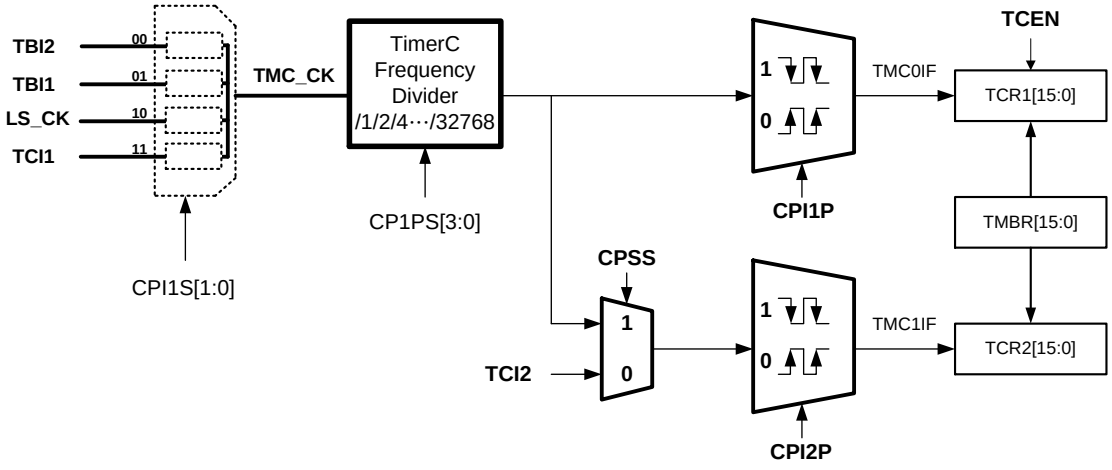


Figure 4-14 Time C block diagram

4.14. EUART and EUART1

EUART TRANSMIT BLOCK DIAGRAM

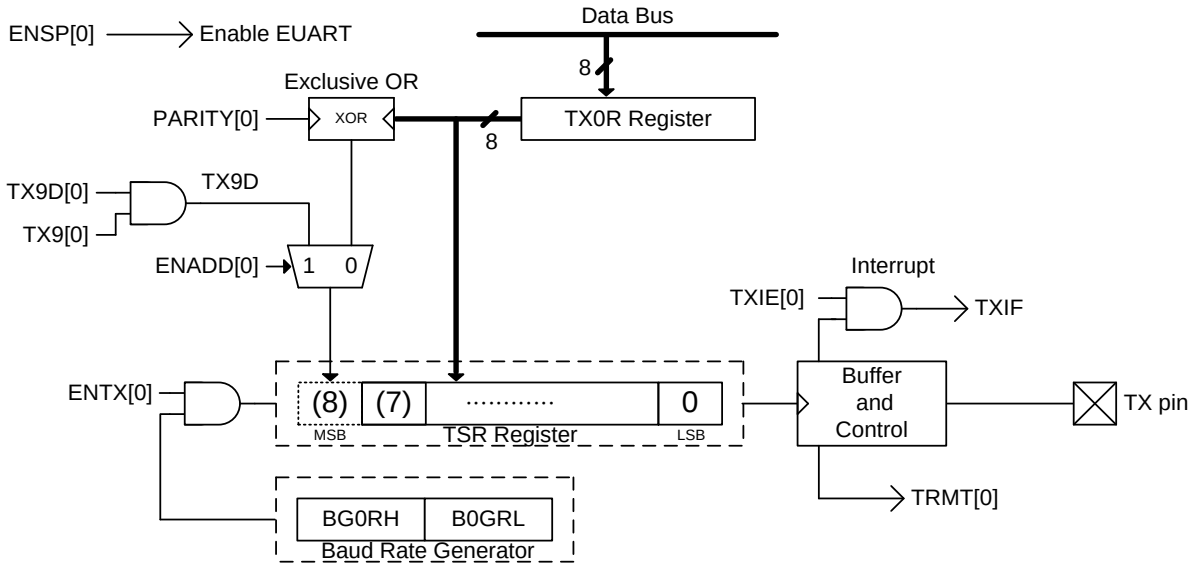
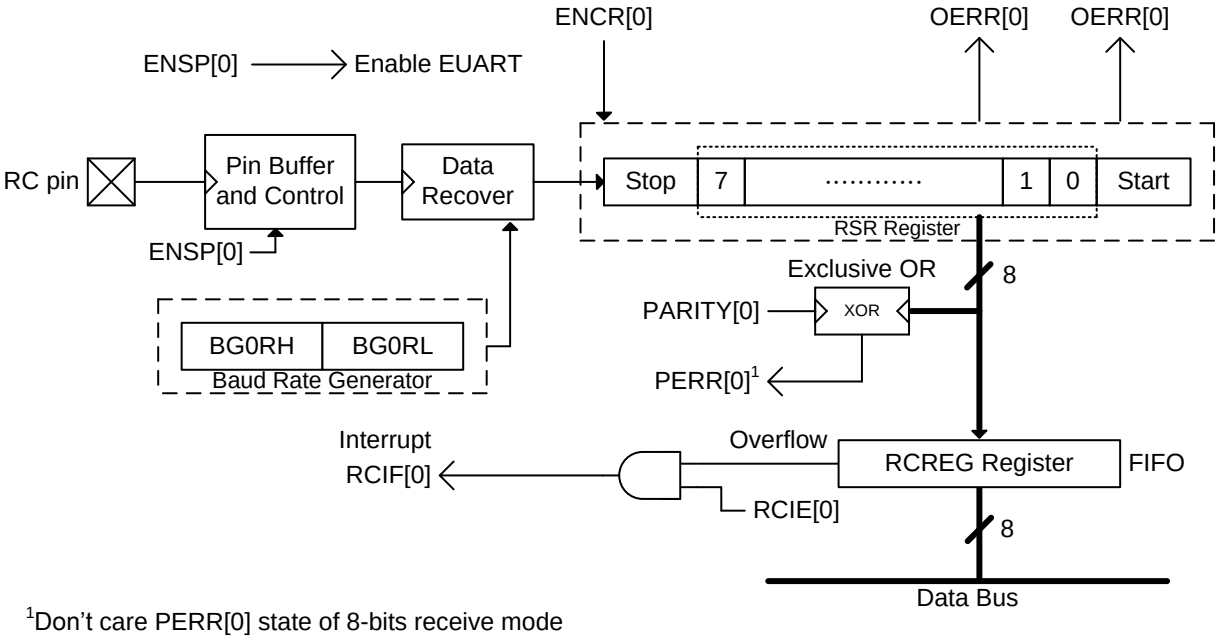


Figure 4-15 EUART transmit block diagram

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

Figure 4-16 EUART 8-bits receive block diagram

4.15. I2C and I2C1

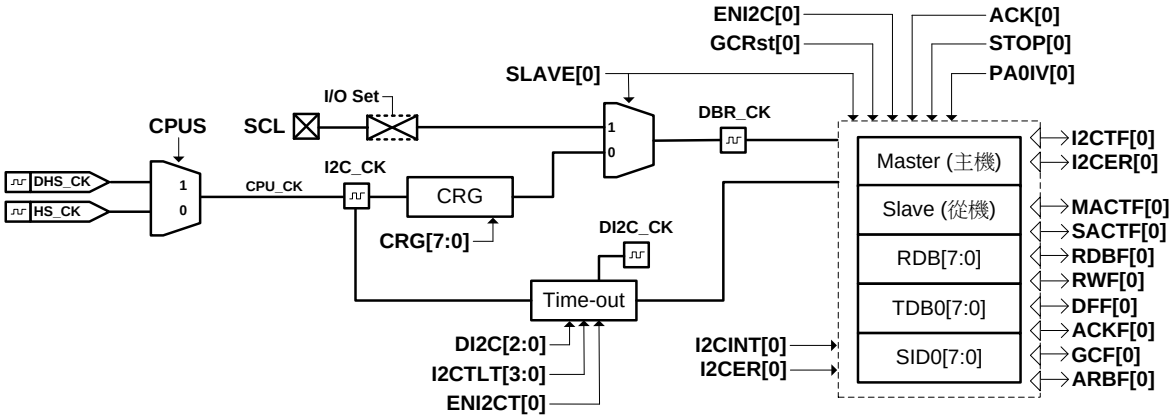


Figure 4-17 I²C transmission block diagram

4.16. SPI

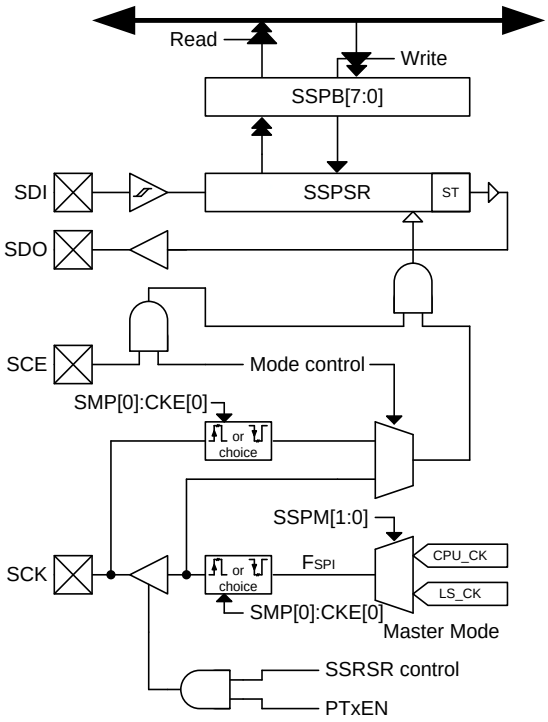


Figure 4-18 SPI transmission block diagram

5. Register list

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memory value of FSR0 post-increment								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decrement								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremente								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005h	INDF1	Contents of FSR1 to address data memory value of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006h	POINC1	Contents of FSR1 to address data memory value of FSR1 post-increment								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007h	PODEC1	Contents of FSR1 to address data memory value of FSR1 post-decrement								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008h	PRINC1	Contents of FSR1 to address data memory value of FSR1 pre-incremente								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009h	PLUSW1	Contents of FSR1 to address data memory value of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ah	INDF2	Contents of FSR2 to address data memory value of FSR2 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Bh	POINC2	Contents of FSR2 to address data memory value of FSR2 post-increment								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ch	PODEC2	Contents of FSR2 to address data memory value of FSR2 post-decrement								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Dh	PRINC2	Contents of FSR2 to address data memory value of FSR2 pre-incremente								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Eh	PLUSW2	Contents of FSR2 to address data memory value of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Fh	FSR0H	-	-	-	-	-	-	FSR0[9:8]		00	.... uuuu	-,-,-,-,*,*,*,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR1H	-	-	-	-	-	-	FSR1[9:8]		00	.... .uuu	-,-,-,-,*,*,*,*
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
013h	FSR2H	-	-	-	-	-	-	FSR2[9:8]		00	.... .uuu	-,-,-,-,*,*,*,*
014h	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	TOS[12:8]					...0 0000	.uuu uuuu	-,*,*,*,*,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000.	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	SKPRT[3:0]				000. 0000	u$$. $$$$	rw0,rw0,rw0,- *,*,*,*
01Ah	PCLATH	-	-	-	PC[12:8]					...0 0000	..00 0000	*,*,*,*,*,*,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Dh	TBLPTRH	-	-	-	TBLPTR[12:8]					...x xxxx	..uu uuuu	-,-,*,*,*,*,*,*
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021h	PRODH	Product Register of Multiply High Byte								0001 0010	uuuu uuuu	*,*,*,*,*,*,*,*
022h	PRODL	Product Register of Multiply Low Byte								0011 0100	uuuu uuuu	*,*,*,*,*,*,*,*
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE	-	-	E0IE	0000 0..0	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	TA1IE	SPIIE	TXIE	RCIE	I2CERIE	I2CIE	-	E2IE	0000 00.0	uuuu uuuu	*,*,*,*,*,*,*,*
025h	INTE2	TA2IE	TA2CIE	TC12IE	TC11IE	TX2IE	RC2IE	-	BOR2IE	0000 00.0	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF	-	-	E0IF	.000 0..0	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	TA1IF	SPIIF	TXIF	RCIF	I2CERIF	I2CIF	-	E2IF	0100 00.0	uuuu uuuu	*,*,*,* r,r,*,*
028h	INTF2	TA2IF	TA2CIF	TC2IF	TC1IF	TX2IF	RC2IF	-	BOR2IF	0000 10.0	uuuu uuuu	*,*,*,*,*,*,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Ah	BSRCN	-	-	-	-	-	-	BSR[1:0]		00	.... ..uu	-,-,-,-,- -,-,*,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	BOR2LV	GCRstIF	$000 $000	uu$u u$uu	rw0,rw0,rw0,rw0 rw0,rw0,r,rw0
02Eh	INTE3	-	-	-	-	-	-	I2CER2IE	I2C2IE	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
030h	INTF3	-	-	-	-	-	-	I2CER2IF	I2C2IF	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
031h	BIECN	1			ENBVD	VPPHV	ENBCP	BIEWR	BIERD	1.00 $000	1.00 $uuu	r1,-,*,* r,*,*,*
033h	BIEARL			BIE Address Register as BIEAL[5:0]						...1 1111	uuuu uuuu	*,*,*,*,*,*,*,*
034h	BIEDRH	BIE High Byte Data Register								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
035h	BIEDRL	BIE Low Byte Data Register								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
036h	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	CSFON	1000 0000	uuuu uu0u	*,*,*,*,*,*,*,*
037h	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
038h	OSCCN1	CCOPT	LCPS	DADC[1:0]		DTMB[1:0]		TMBS	-	0000 0000	uuuu uuu.	*,*,*,*,*,*,*,-
039h	OSCCN2	-	-	ENXT	XTS[1:0]		HAOM[1:0]		ENHAO	0000 0001	uuuu uuu1	*,*,*,*,*,*,*,*

Table 5-1 Data memory list (1)

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
03Ah	CSFCN0	SKRST	HAOTR[6:0]							xxxx xxxx	....	-,-,-,- -,-,-,-
03Bh	CSFCN1	ENSDRV	-	-	BOR_TH[2:0]			BORS	ENBOR2	0..0 0011	uuuu uuuu	-,-,-,*,*,*,*
03Eh	WDTCN	ENBZ	BZS	BZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,** rw 1,*,**
03Fh	AD1H	ADC1 conversion high byte data register								0000 0000	..uu uuuu	-,-,*,*,*,*,*,*
040h	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
041h	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
042h	AD1CN0	ENAD1	-		OSR[3:0]				CMFR	000. 0000	uuu. uuuu	*,*,*,*,*,*,*,*
043h	AD1CN1	-	-	VREGN	PGAGN[1:0]		ADGN[2:0]			..00 0000	uuuu uuuu	*,*,*,*,*,*,*,*
044h	AD1CN2	INIS1	-	-	-	DCSET[3:0]				xxxx 0000	uuuu uuuu	*,*,*,*,*,*,*,*
045h	AD1CN3	INP[3:0]				INN[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
046h	AD1CN4	VRH[1:0]		VRL[1:0]		INX[1:0]		VRIS	INIS	0000 00xx	uuuu uuuu	*,*,*,*,*,*,*,*
047h	AD1CN5	ENACM	-	VCMS	LDOPL	-	-	ENTPS	TPSCH	0.00 xx00	uuuu uuuu	*,*,*,*,*,*,*,*
048h	LVDCN	-	-	PWRS	LVDS[3:0]				LVDO	xx00 0000	uuuu uuuu	*,*,*,*,*,*,*,*
049h	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-		0000 00..	u0uu uu.u	*,rw 1,*,*,*,-,*
04Ah	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
04Bh	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
04Ch	TB1Flag	-	PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	.001 1111	.uuu uuuu	-,r,r,r r,r,r,r
04Dh	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	PWMO1	PWMO0	0000 0000	uuuu u0uu	*,*,*,*,*,rw 1,*,*
04Eh	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Fh	TB1RH	TimerB1 counter Register [15:8]								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
050h	TB1RL	TimerB1 counter Register [7:0]								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
051h	TB1C0H	TimerB1 counter Condition Register [15:8]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
052h	TB1C0L	TimerB1 counter Condition Register [7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
053h	TB1C1H	TimerB1 counter Condition Register [15:8]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
054h	TB1C1L	TimerB1 counter Condition Register [7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
055h	TB1C2H	TimerB1 counter Condition Register [15:8]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
056h	TB1C2L	TimerB1 counter Condition Register [7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
057h	TC1CN0		TC1S[1:0]				CPI2P	CPI1P	TCEN	0000 0000	uuuu uuuu	uuuu uuuu
058h	TC1CN1	CPI1R	CPSS	CPI1S[1:0]		CP1PS[3:0]				0000 0000	uuuu uuuu	uuuu uuuu
059h	TC1R0H	Capture 0 High Byte Data Register								0000 0000	uuuu uuuu	uuuu uuuu
05Ah	TC1R0L	Capture 0 Low Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
05Bh	TC1R1H	Capture 1 High Byte Data Register								0000 0000	uuuu uuuu	uuuu uuuu
05Ch	TC1R1L	Capture 1 Low Byte Data Register								xxxx xxxx	uuuu uuuu	uuuu uuuu
05Dh	PT1	-	-	-	-	-	PT1.2	-	PT1.0	.... .0.0	xxxx xxxx	*,*,*,*,*,*,*,*
05Eh	TRISC1	-	-	-	-	-	TC1.2	-	TC1.0	.... .0.0	uuuu uuuu	*,*,*,*,*,*,*,*
05Fh	PT1DA	-	-	-	-	-	DA1.2	-	DA1.0	.... .1.1	uuuu uuuu	*,*,*,*,*,*,*,*
060h	PT1PU	-	-	-	-	-	PU1.2	-	PU1.0	.... .0.0	uuuu uuuu	*,*,*,*,*,*,*,*
061h	PT1M1	-	-	-	-	-	-	INTEG0[1:0]		00	uuuu uuuu	*,*,*,*,*,*,*,*
063h	PT1INT	-	-	-	-	-	INTEG2	-	-	.... .0..	uuuu uuuu	*,*,*,*,*,*,*,*
064h	PT2	-	-	-	-	PT2.3	PT2.2	PT2.1	PT2.0	 0000	uuuu uuuu	*,*,*,*,*,*,*,*
065h	TRISC2	-	-	-	-	TC2.3	TC2.2	TC2.1	TC2.0	 0000	uuuu uuuu	*,*,*,*,*,*,*,*
066h	PT2DA	-	-	-	-	DA2.3	DA2.2	DA2.1	DA2.0	 1111	uuuu uuuu	*,*,*,*,*,*,*,*
067h	PT2PU	-	-	-	-	PU2.3	PU2.2	PU2.1	PU2.0	 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Ah	PT2INT	-	-	-	-	INTG2.3	INTG2.2	INTG2.1	INTG2.0	 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Bh	PT2INTE	-	-	-	-	INTE2.3	INTE2.2	INTE2.1	INTE2.0	 0000	uuuu uuuu	
06Ch	PT2INTF	-	-	-	-	INTF2.3	INTF2.2	INTF2.1	INTF2.0	 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Dh	PT4	PT4.7	PT4.6	PT4.5	PT4.4	-	-	-	-	0000	xxxx xxxx	*,*,*,*,*,*,*,*
06Fh	PT4DA	DA4.7	DA4.6	DA4.5	DA4.4	-	-	-	-	1111	uuuu uuuu	*,*,*,*,*,*,*,*
070h	PT4PU	PU4.7	PU4.6	PU4.5	PU4.4	-	-	-	-	0000	uuuu uuuu	*,*,*,*,*,*,*,*
073h	PT4INT	INTG4.7	INTG4.6	INTG4.5	INTG4.4	-	-	-	-	0000	uuuu uuuu	*,*,*,*,*,*,*,*
074h	PT4INTE	INTE4.7	INTE4.6	INTE4.5	INTE4.4		-	-	-	0000	uuuu uuuu	*,*,*,*,*,*,*,*
075h	PT4INTF	INTF4.7	INTF4.6	INTF4.5	INTF4.4	-	-	-	-	0000	uuuu uuuu	*,*,*,*,*,*,*,*
076h	PT12	PT12.7	PT12.6	PT12.5	PT12.4	PT12.3	PT12.2	PT12.1	PT12.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
077h	TRISC12	TC12.7	TC12.6	TC12.5	TC12.4	TC12.3	TC12.2	TC12.1	TC12.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
078h	PT12DA	DA12.7	DA12.6	DA12.5	DA12.4	DA12.3	DA12.2	DA12.1	DA12.0	1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
079h	PT12PU	PU12.7	PU12.6	PU12.5	PU12.4	PU12.3	PU12.2	PU12.1	PU12.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

Table 5-2 Data memory list (2)

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
07Ah	TMA2CN	ENTMA2	TMACL2	TMAS2	DTMA2[2:0]			-	-	0000 00..	u0uu uu..	*,rw1,*,*,*,-,-
07Bh	TMA2R	TMA2 counter Register								0000 0000	uuuu uuuu	w0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
07Ch	TMA2C	TMA2C counter Register								0000 0000	uuuu uuuu	w0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
07Dh	SSPCN0	ENSSP	CKP	CKE	SMP	-	-	SSPM[1:0]		0000 ..00	uuuu ..uu	*,*,*,*,-,-,*,*
07Eh	SSPSTA0	SSPBY	SSPOV	-	-	-	-	-	BF	00.. ...0	uu.. ...u	*,*,-,- -,-,-,*
07Fh	SSPBUF0	SSP Receive/Transmit Buffer Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
180h	CFG0	-	-	-	-	-	GCRst	ENI2CT	ENI2C	.... .000	.... .uuu	-,-,-,- -,*,*,*
181h	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0..0 0000	uuuu uuuu	*,*,*,*,*,*,*,*
182h	STA0	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0011 0000	uuuu uuuu	*,*,*,*,*,*,*,*
183h	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
184h	TOC0	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
185h	RDB0	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
186h	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
187h	SID0	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
188h	CFG2	-	-	-	-	-	GCRst	ENI2CT	ENI2C	0000 0000	.... .uuu	-,-,-,- -,*,*,*
189h	ACT2	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18Ah	STA2	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0011 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18Bh	CRG2	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18Ch	TOC2	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18Dh	RDB2	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Eh	TDB2	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Fh	SID2	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
190h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	000x x..0	uuuu u..u	*,*,*,*,-,-,*
191h	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.x00 0110	.uuu uuuu	-,r,r,r r,r,r,rw0
192h	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD	 0000	.... uuuu	-,-,-,- *,*,*'
193h	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
194h	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
195h	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
196h	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
197h	UR2CN	ENSP2	ENTX2	TX92	TX9D2	PARITY2	-	-	WUE2	000x x..0	uuuu u..u	*,*,*,*,-,-,*
198h	UR2STA	-	RC9D2	PERR2	FERR2	OERR2	RCIDL2	TRMT2	ABDOVF2	.x00 0110	.uuu uuuu	-,r,r,r r,r,r,rw0
199h	BA2CN	-	-	-	-	ENCR2	RC92	ENADD2	ENABD2	 0000	.... uuuu	-,-,-,- *,*,*'
19Ah	BG2RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
19Bh	BG2RL	Baud Rate2 Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19Ch	TX2R	UART2 Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19Dh	RC2REG	UART2 Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
19Eh	CCNT	-	-	-	-		CCLevel[2:0]			xxxx x000	uuuu uuuu	*,*,*,*,*,*,*,*
19Fh	ENCCMode	ENCC7	ENCC6	ENCC5	ENCC4	ENCC3	ENCC2	ENCC1	ENCC0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B0h	PT1AIE	-	-	-	-	-	AIE12	-	-	uuuu u0u0	uuuu u0u0	*,*,*,*,*,*,*,*
1B3h	PT4AIE	AIE47	AIE46	AIE45	AIE44	-	-	-	-	0000 uuuu	0000 uuuu	*,*,*,*,*,*,*,*
080h ~ 0FFh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
100h ~ 17Fh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
200h ~ 2FFh		SRAM as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

Table 5-3 Data memory list (3)

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . . −0.2 V to 6.0 V

Voltage applied to any pin . . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to VPP pin . . . . . −0.2 V to 8.75 V

Diode current at any device terminal . . . . . ±2 mA

Operating temperature range . . . . . −40℃ to 85℃

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT2 I/O pin 20mA

Maximum output current sink by any PORT12 pin 90mA

6.1. Recommended Operating Conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		All digital peripherals and CPU		2.2		5.5	V
V_{DDA}	Supply Voltage		Analog peripherals		2.4		4.5	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD}=2.2V~5.5V, ENXT[0]=1	XTS[1:0]=0x		32768		Hz
		Ceramic resonator		XTS[1:0]=10	450K		8M	
		Crystal		XTS[1:0]=11	1M		8M	
		Ceramic resonator	V_{DD}=3.6V~5.5V, ENXT[0]=1	XTS[1:0]=10	450K		16M	
		Crystal		XTS[1:0]=11	1M		16M	

6.2. Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency	1.843MHz Mode: ENHAO[0]=1, HAOM[1:0]=00b,	-20%	1.843	+20%	MHz
		3.686MHz Mode: ENHAO[0]=1, HAOM[1:0]=01b	-20%	3.686	+20%	
		7.834MHz Mode: ENHAO[0]=1, HAOM[1:0]=11b	-20%	7.834	+20%	
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	-20%	14.5	+20%	KHz

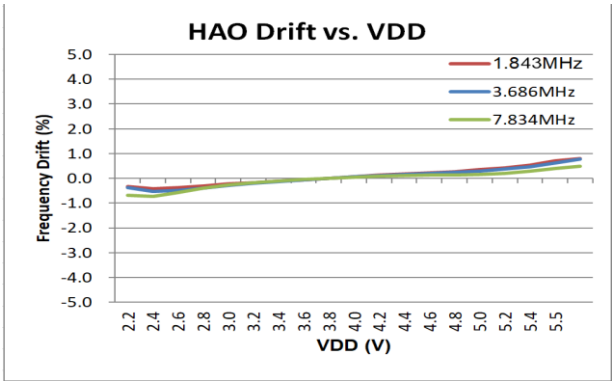


Figure 6.2-1 HAO vs. VDD

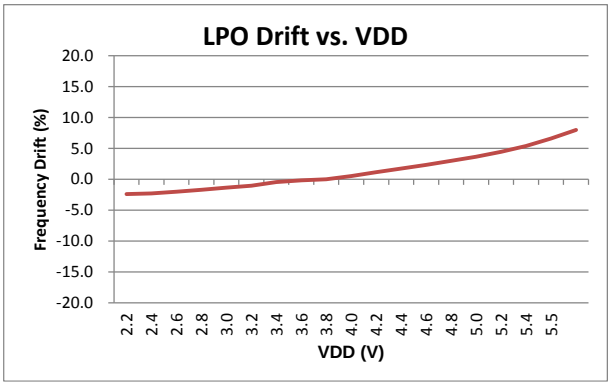


Figure 6.2-2 LPO vs. VDD

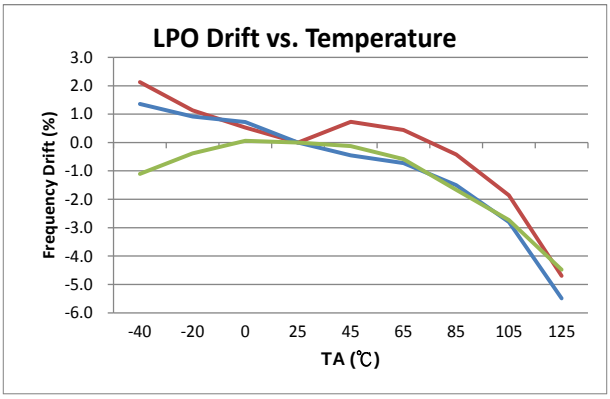


Figure 6.2-3 LPO vs. Temperature

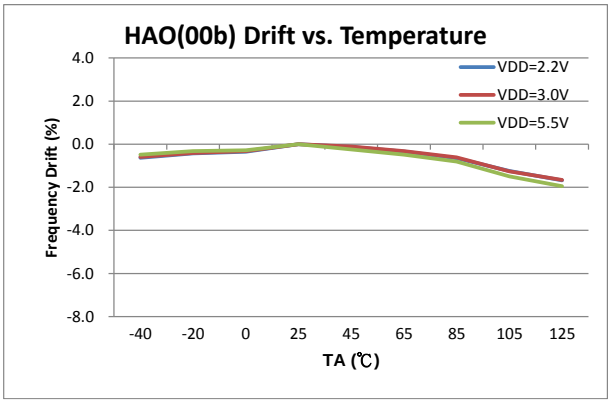


Figure 6.2-4 HAO(00b) vs. Temperature

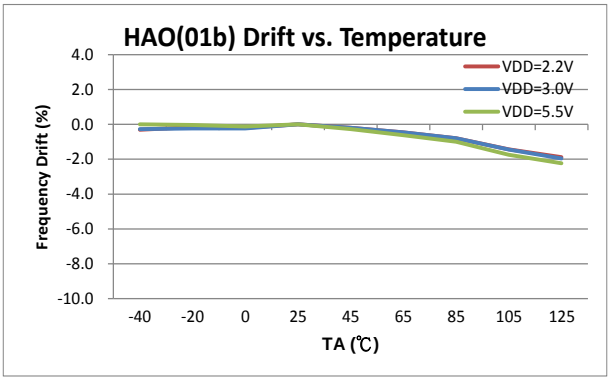


Figure 6.2-5 HAO(01b) vs. Temperature

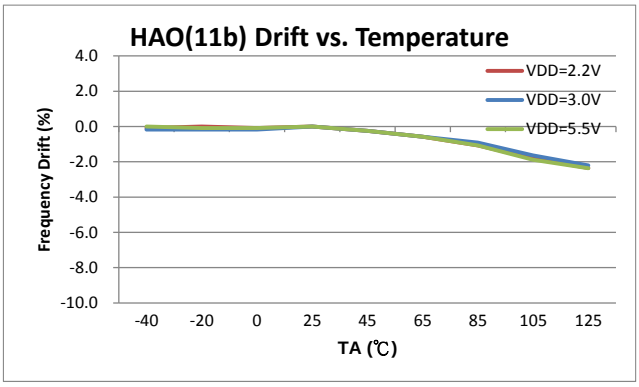


Figure 6.2-6 HAO(11b) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 14.5KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 7.834MHz, CPU_CK = 7.834MHz		600	1000	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =3.686MHz, CPU_CK = 3.686MHz		320	650	uA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz		210	450	uA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz/2		160	350	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		2	5	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.0	2.5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.25	1.0	uA
I_{LP4}	Low Power 4	OSC_CY = 32768, OSC_HAO = off, CPU_CK = 32768, Idle state		3.23		uA
I_{LP5}	Low Power 5	OSC_CY = 32768, OSC_HAO = off, CPU_CK = off, Sleep state		1.75		uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

T_A = 25℃,V_{DD} = 5.5V,OSC_LPO = 14.5KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 7.834MHz, CPU_CK = 7.834MHz		1200	1800	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =3.686MHz, CPU_CK = 3.686MHz		720	1200	uA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz		500	1000	uA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz/2		400	800	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		4	10	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		2.5	5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.4	2	uA
I_{LP4}	Low Power 4	OSC_CY = 32768, OSC_HAO = off, CPU_CK = 32768, Idle state		8.56		uA
I_{LP5}	Low Power 5	OSC_CY = 32768, OSC_HAO = off, CPU_CK = off, Sleep state		4.97		uA

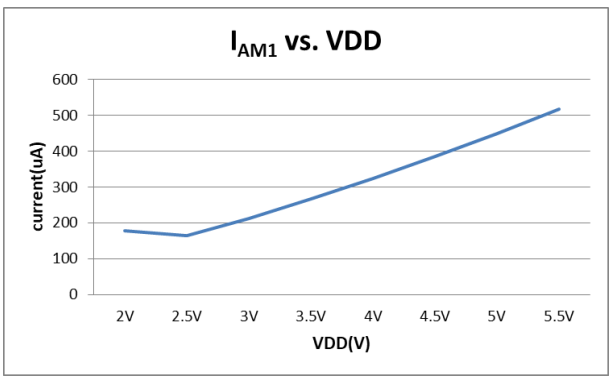


Figure 6.3-1 I_{AM1} vs. VDD

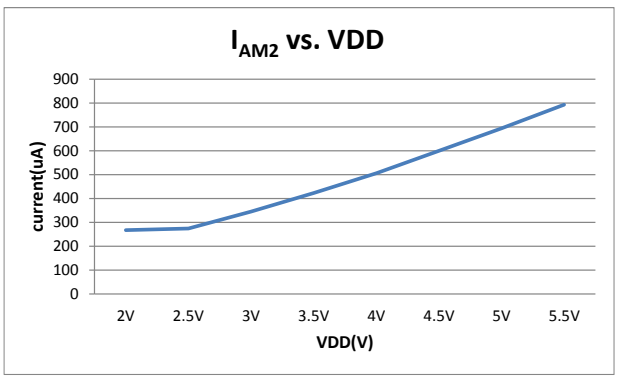


Figure 6.3-2 I_{AM2} vs. VDD

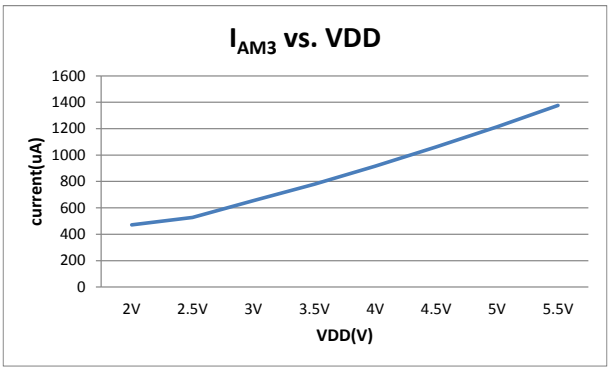


Figure 6.3-3 I_{AM3} vs. VDD

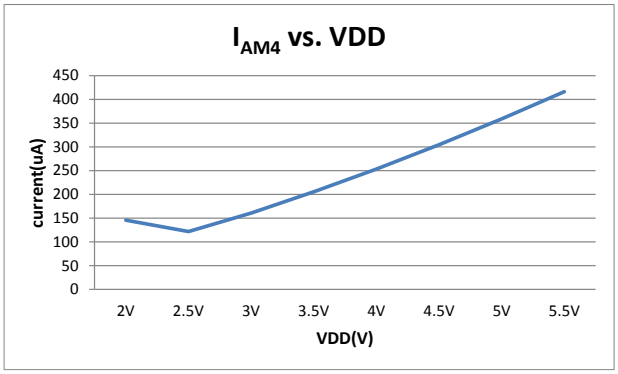


Figure 6.3-4 I_{AM4} vs. VDD

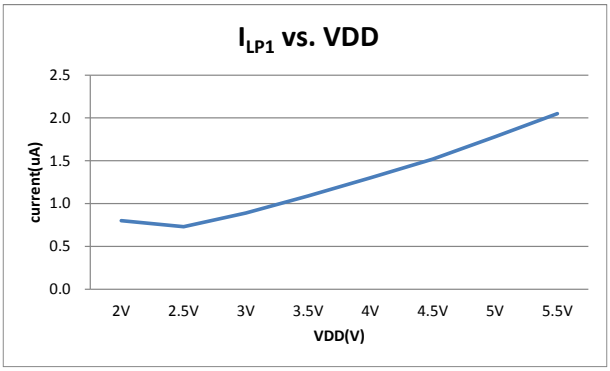


Figure 6.3-5 I_{LP1} vs. VDD

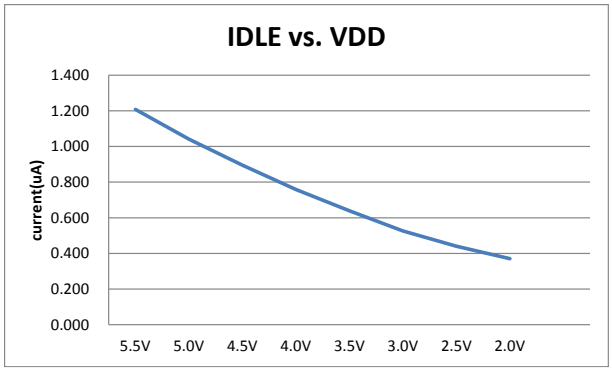


Figure 6.3-6 I_{LP2} vs. VDD

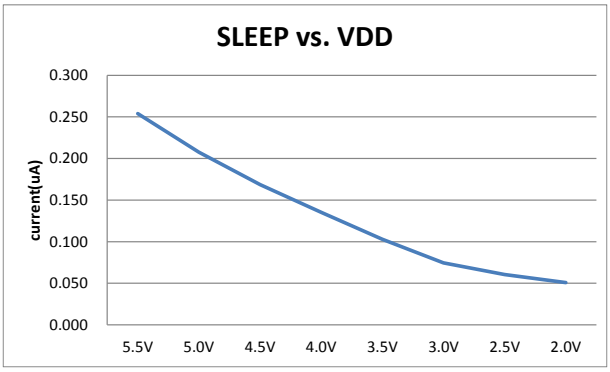


Figure 6.3-7 I_{LP3} vs. VDD

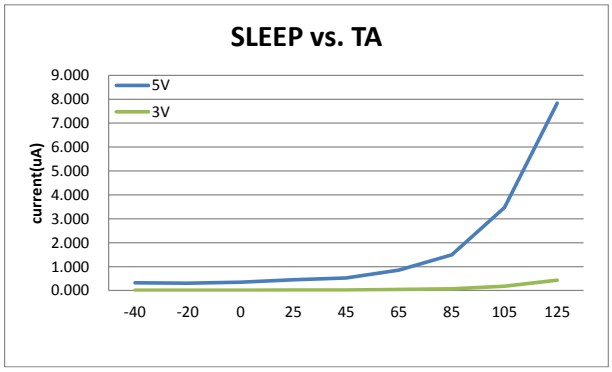


Figure 6.3-8 I_{LP3} vs. Temperature

6.4. Port1、2

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.4		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD=3V, IOH=-10mA,	VDD -0.4			V
		VDD=5V, IOH=-15mA,	VDD -0.4			
V_{OL}	Low-level output voltage	VDD=3V, IOL=10mA			VSS +0.4	
		VDD=5V, IOL=15mA			VSS +0.4	

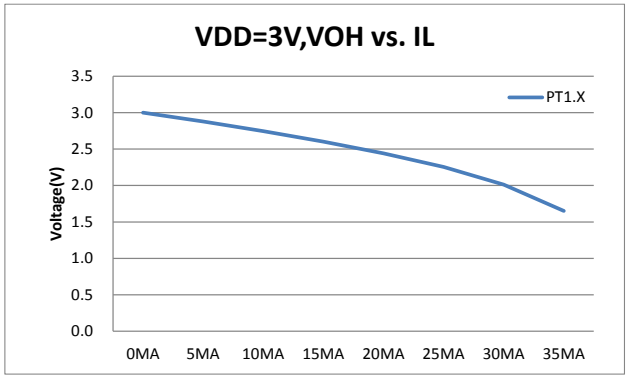


Figure 6.4-1 V_{OH} vs. I_{OH}

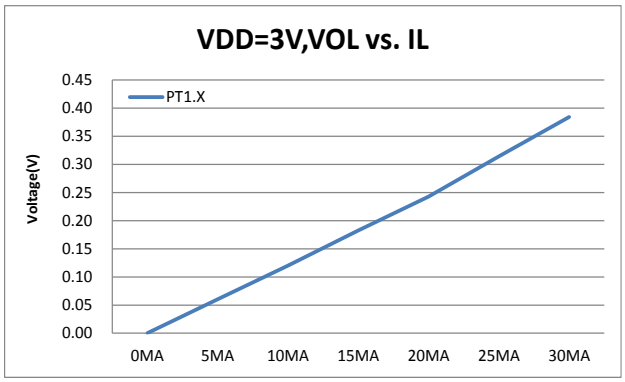


Figure 6.4-2 V_{OL} vs. I_{OL}

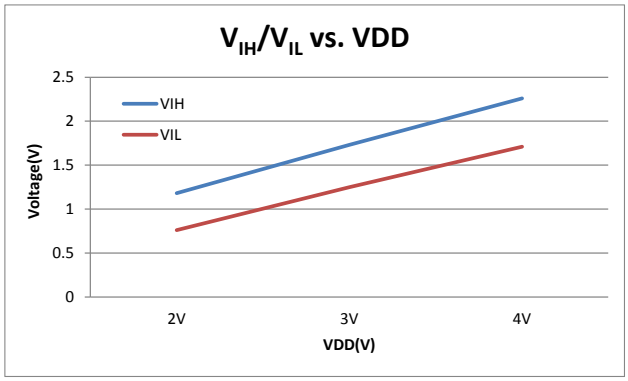


Figure 6.4-3 V_{IH}/V_{IL} vs. VDD

6.5. Port12 and Constant current control circuit

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	VDD	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing							
V_{IH}	High-Level input voltage	3				2.1	V
V_{IL}	Low-Level input voltage	3		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)	3			0.4		V
I_{LKG}	Leakage Current	3				0.1	uA
R_{PU}	Port pull high resistance	-			60		kΩ
Output voltage and current							
I_{OH}	Standard GPIO, SEG and COM Source Current	3V	Voh=0.9*VDD	-4	-8		mA
		5V		-8	-15		mA
I_{OL}	COM Sink Current	3V	Vol=0.1*VDD	16	32		mA
		5V		40	80		mA
CC	Constant current level	5V	CCLevel=2'b111		-15		mA
			CCLevel =2'b110		-13		
			CCLevel =2'b101		-11		
			CCLevel =2'b100		-9		
			CCLevel =2'b011		-7		
			CCLevel =2'b010		-5		
			CCLevel =2'b001		-3		
			CCLevel =2'b000		-2		
	Current Skew (Channel)	3V/5V	Vds=0.5V, CCLevel=2'b111		±3		%
	Current Skew (IC)	3V/5V	Vds=0.5V, CCLevel=2'b111		±3		%
	Output Current vs. Output Voltage Regulation	5V	Vds=0.5V~3.5V, CCLevel=2'b111		±0.3		%/V
	Output Current vs. Supply Voltage Regulation	-	VDD=3.0V~5.5V, Vds=0.5V, CCLevel=2'b111			1.5	%

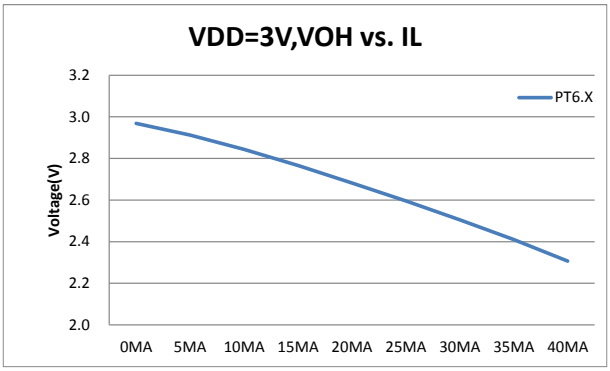


Figure 6.5-1 V_{OH} vs. I_{OH}

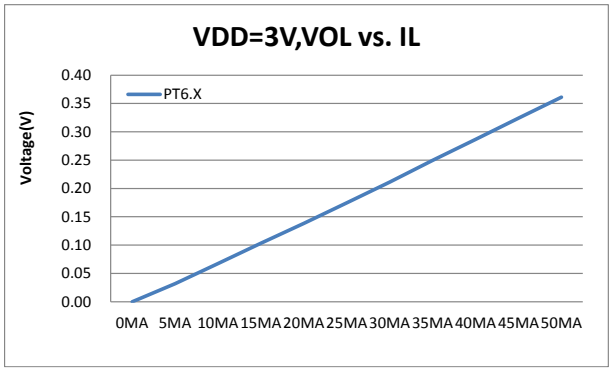


Figure 6.5-2 V_{OL} vs. I_{OL}

6.6. Reset(Brownout, External RST pin, Low Voltage Detect)

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BOR1	Pulse length needed to accepted reset internally, td-LVR		2			uS
	VDD Start Voltage to accepted reset internally (L➔H),VLVR	TA = 25℃	1.0	1.3	1.6	V
	VDD Start Voltage to accepted reset internally (L➔H),VLVR,	TA = -40℃ ~ 125 ℃	1.0		1.6	V
	Current consumption	VDD=3.3V		0.2		uA
		VDD=5.5V		0.3		uA
BOR2	Pulse length needed to accepted reset internally, td-LVR		2			uS
	VDD Start Voltage to accepted reset internally (L➔H)	BOR_TH[2:0]=001b, TA=25°C	-8%	2.0	+8%	V
		BOR_TH[2:0]=001b, TA=-40°C~85°C	-8%	2.0	+8%	V
	VDD Start Voltage to accepted reset internally (H➔L)	BOR_TH[2:0]=001b, TA=25°C	-8%	1.95	+8%	V
		BOR_TH[2:0]=001b, TA=-40°C~85°C	-8%	1.95	+8%	V
	Hysteresis, VHYS-LVR			50		mV
	VDD Start Voltage to accepted reset internally (L➔H)	BOR_TH[2:0]=010b	-8%	2.2	+8%	V
	VDD Start Voltage to accepted reset internally (L➔H)	BOR_TH[2:0]=011b	-8%	2.5	+8%	V
	VDD Start Voltage to accepted reset internally (L➔H)	BOR_TH[2:0]=100b	-8%	2.8	+8%	V
	VDD Start Voltage to accepted reset internally (L➔H)	BOR_TH[2:0]=101b	-8%	3.0	+8%	V
	VDD Start Voltage to accepted reset internally (L➔H)	BOR_TH[2:0]=110b	-10%	3.7	+10%	V
	VDD Start Voltage to accepted reset internally (L➔H)	BOR_TH[2:0]=111b	-10%	4.0	+10%	V
	Current consumption	VDD=3.3V		8		uA
		VDD=5.5V		10		uA
RST	Pulse length needed as RST/VPP pin to accepted reset internally, td-RST		2			us
	Input Voltage to accepted reset voltage			1.1		V
	Reset release voltage			2		V
LVD	Operation current, ILVD			2.5		uA
	External input voltage to compare reference voltage		1.15	1.2	1.25	V
	Compare reference voltage temperature drift	TA = -40℃ ~ 85 ℃	1.147		1.255	V
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1110b		-5%	4.0	+5%	V
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1101b			3.6		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1100b			3.3		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1011b			3.0		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1010b			2.9		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1001b			2.8		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=1000b			2.7		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0111b			2.6		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0110b			2.5		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0101b			2.4		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0100b			2.3		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0011b			2.2		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0010b			2.1		
	Detect VDD voltage rang by user option, VSVS VLDx[3:0]=0001b			2.0		

BOR1/BOR2：Brownout Reset; LVR：Low Voltage Reset of BOR; LVD：Low Voltage Detect; RST：External Reset pin

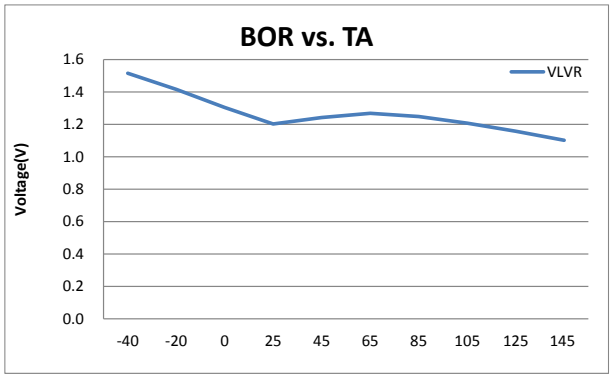


Figure 6.6-1 BOR vs. Temperature

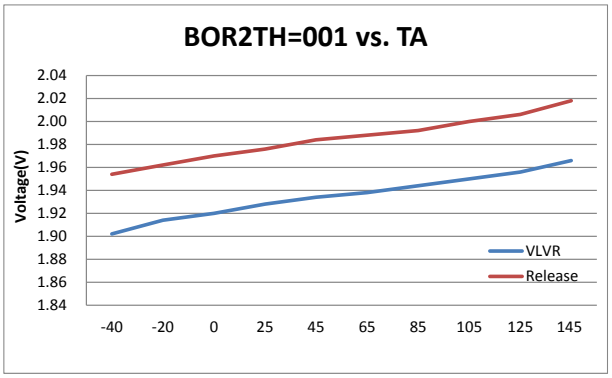


Figure 6.6-2 BOR2 vs. Temperature

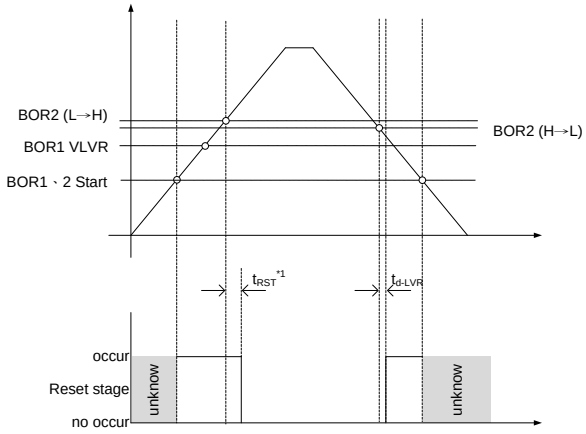


Figure 6.6-3 BOR Reset diagram

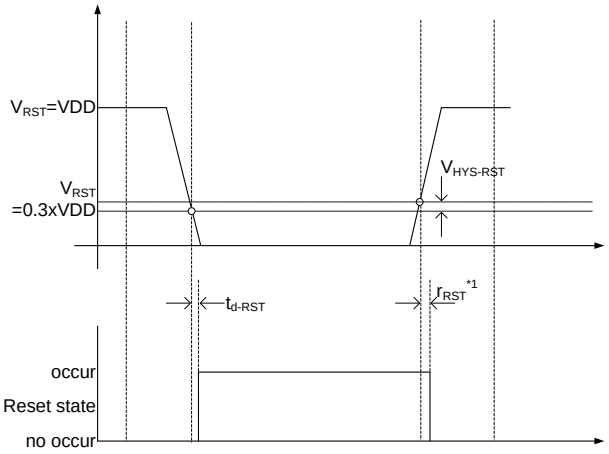


Figure 6.6-4 RST Reset diagram

6.7. Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	IL = 0.1mA, VDD=5.5V	LDOC [2:0]=000b	-5%	2.4	5%	V
			LDOC [2:0]=001b		2.6		V
			LDOC [2:0]=010b		2.9		V
			LDOC [2:0]=011b		3.3		V
			LDOC [2:0]=100b		3.6		V
			LDOC [2:0]=101b		4.0		V
			LDOC [2:0]=110b		4.5		V
			LDOC [2:0]=111b		5.0		V
		IL = 10mA, VDD=2.6V	LDOC [2:0]=000b	-6%	2.4		V
	Dropout voltage	VDD=2.9V, VDDA=2.9V mode (LDOC [2:0]=010b), IL = 10mA			200		mV
	Temperature drift	LDOC [2:0]=000b I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	LDOC [2:0]=000b	V_{DD}=2.2V~5.5V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	VDDA=2.4V, ENADC[0]=1b, ENACM=1b			50		uA
	Internal Analog Common Mode Voltage ,V_{ACM}=1.2V or V_{ACM} VDDA/2		VCMS=0b, I_L = 0uA		VDDA/2		V
			VCMS=1b, I_L = 0uA		1.2		V
	Temperature drift		T_A=-40℃~85℃, ENACM [0]=1b		50		ppm/℃
VDDA：Adjust Voltage Regulator, ACM：Internal Analog Common Mode Voltage VDDA/2 (No voltage output) or 1.2V							

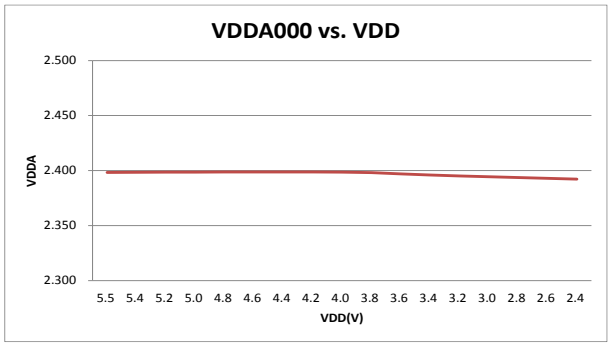


Figure 6.7-1 VDDA(000b) vs. VDD

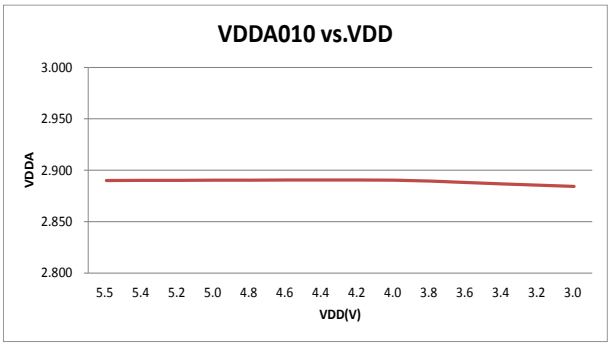


Figure 6.7-2 VDDA(010b) vs. VDD

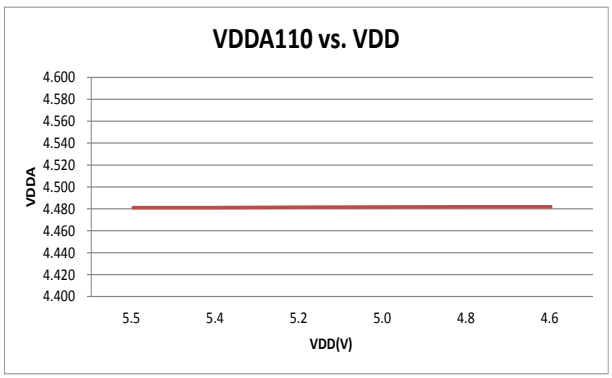


Figure 6.7-3 VDDA(110b) vs. VDD

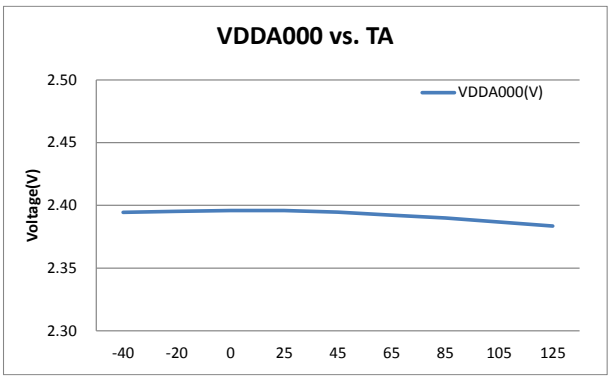


Figure 6.7-4 VDDA(000b) vs. Temperature

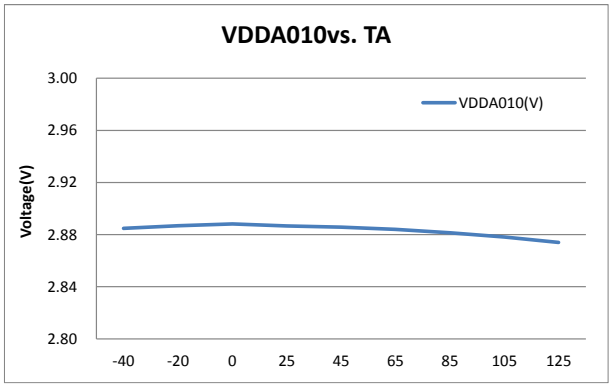


Figure 6.7-5 VDDA(010b) vs. Temperature

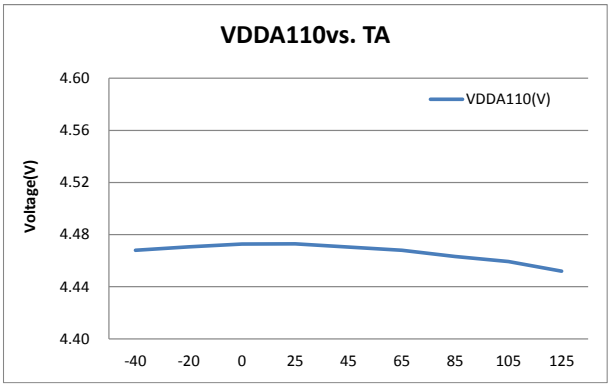


Figure 6.7-6 VDDA(110b) vs. Temperature

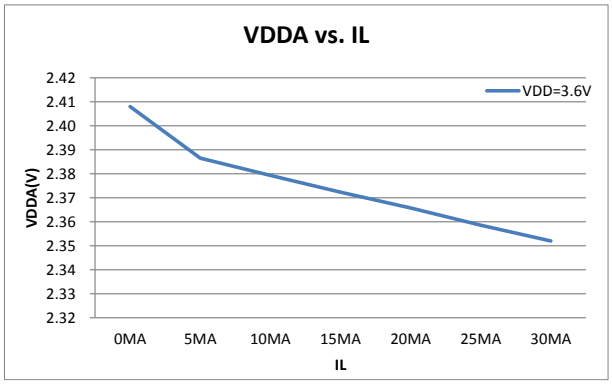


Figure 6.7-7 VDDA vs. Load current

6.8. SD18, Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		4.5	V
f_{SD18}	Modulator sample frequency, ADC_CK				1000		KHz
	Over Sample Ratio, OSR			64		65536	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1	GAIN =16, ADC_CK=1MHz		260		uA

6.8.1. PGA, Power Supply and recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		4.5	V
I_{PGA}	Operation supply current				400		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=8*16		10		ppm/℃
	Input RMS Noise	ADC CLK=1MHz, OSR=65536, ADC VR=1.2V w/ chopper mode	GAIN=8*16		106		nV

6.8.2. SD18,performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,V_{VR}=1.0V,GAIN=1 without PGA,fSD18=1MHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV			±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV					
	No Missing Codes[3]	ADC_CK=1MHz,OSR=65536		23			Bits
G_{SD18}	Temperature drift Gain x16	T_A = -40℃~ 85℃			10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=1.2V DCSET[3:0]=<0000> *ΔAI is external short	Gain=2			1	%FSR
	Offset error temperature drift with chopper without PGA		GAIN=1		0.05		uV/℃
			GAIN=2		0.06		
			GAIN=4		0.06		
			GAIN=16		0.06		
	Offset temperature drift without chopper		GAIN=128		0.09		uV/℃
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16		75		
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off		75		dB
			GAIN=16 PGA=8				

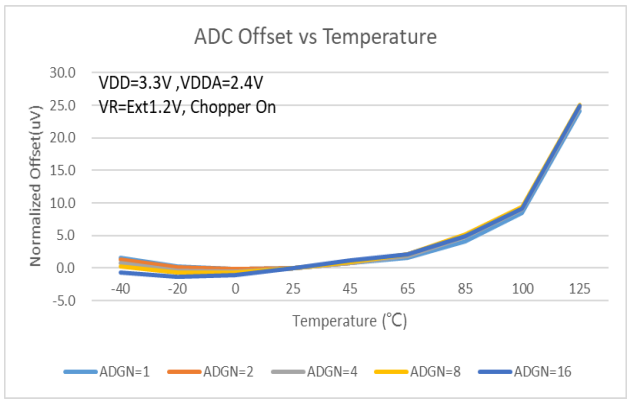


Figure 6.8-1 ADC Offset drift with Temperature

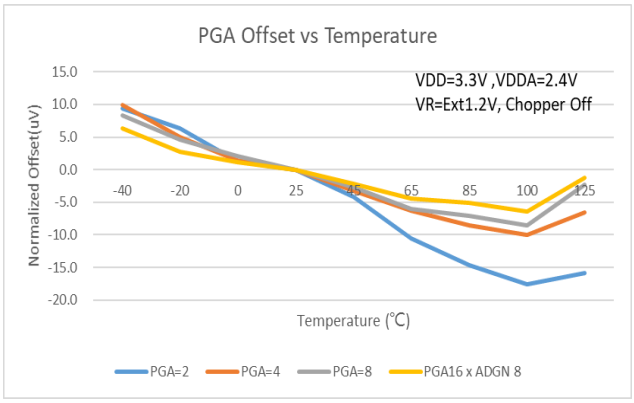


Figure 6.8-2 PGA Offset drift with Temperature

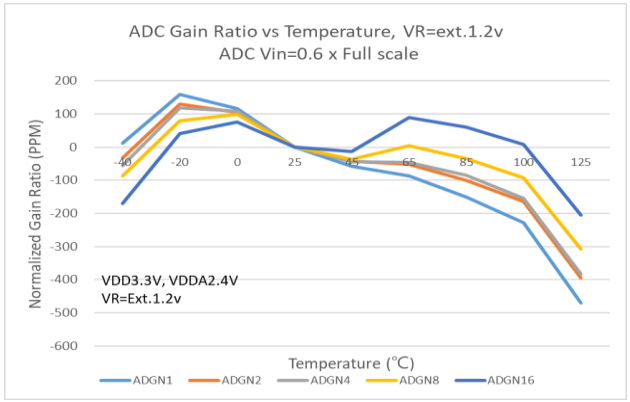


Figure 6.8-3 ADC Gain drift with Temperature

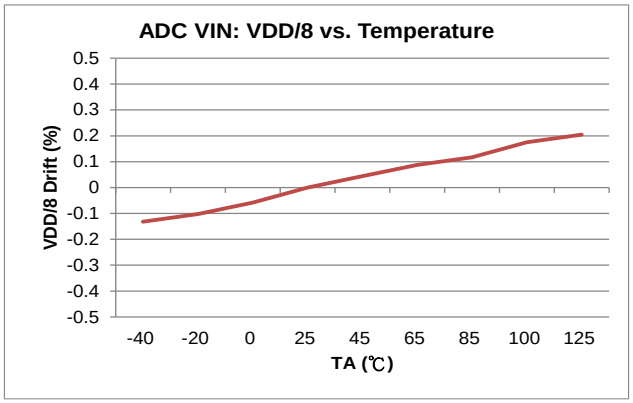


Figure 6.8-4 VDD/8 drift with Temperature

6.8.3. ΣΔADC Noise Performance

Provide important input noise specifications for the ΣΔ ADC. Table 6.7-2 (a), Table 6.7-2 (b) lists typical noise specifications such as gain, output rate and single-ended maximum input voltage, etc. The test conditions are set on the AI3-AI4 external input short, and the ADC reference voltage source is using the internal V12 and VSS, when the reference voltage network, the equivalent reference voltage is 1.2V, sampling 1024 data.

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, Vin=Ext.Short, VREF=(SDRV)/2=1.2V,

Max. Vin(mV) =0.9VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(Hz)					15625	7813	3906	1953	977	488	244	122	61	31	15
	Gain	=	PGAGN	x	ADGN											
±2160	0.25	=	off	x	0.25	13.75	16.82	17.63	18.04	18.64	19.12	19.46	19.95	20.33	20.71	20.81
±2160	0.5	=	off	x	0.5	13.22	16.75	17.45	17.93	18.5	19.04	19.41	19.85	20.17	20.68	20.87
±1080	1	=	off	x	1	13.05	16.59	17.3	17.85	18.37	18.8	19.19	19.58	20.03	20.4	20.65
±540	2	=	off	x	2	13.84	16.52	17.05	17.56	18.08	18.45	18.91	19.37	19.71	20.09	20.38
±270	4	=	off	x	4	11.21	16.14	16.81	17.29	17.8	18.23	18.58	18.99	19.28	19.59	19.86
±135	8	=	off	x	8	11.85	15.78	16.32	16.82	17.22	17.69	18.04	18.56	18.92	19.28	19.51
±68	16	=	off	x	16	9.71	15.35	15.89	16.32	16.71	17.25	17.54	17.91	18.48	18.87	18.87
±540	2	=	2	x	1	13.71	16.39	17.11	17.63	18.2	18.68	19.01	19.44	19.84	20.31	20.57
±270	4	=	4	x	1	14.16	16.34	16.94	17.54	17.96	18.5	18.87	19.28	19.82	20.08	20.45
±135	8	=	8	x	1	13.01	16.08	16.78	17.26	17.7	18.24	18.56	19.05	19.59	20	20.35
±8	128	=	8	x	16	10.91	12.6	13.16	13.67	14.15	14.59	14.99	15.54	16.01	16.51	17.03

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, Vin=Ext.Short, VREF=(SDRV)/2=1.2V, at High Accuracy Mode

Max. Vin(mV) =0.9VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(Hz)					15625	3906	1953	977	488	244	122	61	31	15	8
	Gain	=	PGAGN	x	ADGN											
±2160	0.25	=	off	x	0.25	15.71	17.35	18.14	18.59	19.09	19.69	20	20.45	20.93	21.41	21.8
±2160	0.5	=	off	x	0.5	15.68	17.28	17.99	18.51	19.1	19.55	19.87	20.41	20.88	21.25	21.76
±1080	1	=	off	x	1	15.74	17.16	17.81	18.32	18.86	19.34	19.73	20.2	20.7	21.05	21.5
±540	2	=	off	x	2	15.65	16.94	17.57	18.07	18.56	19.1	19.42	19.96	20.37	20.81	21.2
±270	4	=	off	x	4	15.4	16.68	17.24	17.76	18.24	18.75	19.11	19.57	20.02	20.4	20.79
±135	8	=	off	x	8	15.44	16.28	16.83	17.34	17.79	18.25	18.6	19.09	19.64	20.02	20.42
±68	16	=	off	x	16	15.05	15.75	16.36	16.73	17.28	17.65	17.99	18.48	19.12	19.62	19.84
±540	2	=	2	x	1	15.72	16.93	17.66	18.11	18.65	19.05	19.44	19.95	20.42	20.89	21.31
±270	4	=	4	x	1	15.72	16.78	17.38	17.9	18.44	18.91	19.26	19.81	20.33	20.77	21.17
±135	8	=	8	x	1	15.38	16.55	17.08	17.7	18.19	18.64	19.01	19.43	19.95	20.52	20.99
±8	128	=	8	x	16	12.32	12.84	13.42	13.88	14.51	14.91	15.4	15.98	16.4	16.85	17.38

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

Table6.8-1 SD18 ENOB Table

RMS(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, Vin=Ext.Short, VREF=(SDRV)/2=1.2V,

Max. Vin(mV) =0.9VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(Hz)					15625	7813	3906	1953	977	488	244	122	61	31	15
	Gain	=	PGAGN	x	ADGN											
±2160	0.25	=	off	x	0.25	671.89	80.16	45.86	34.33	22.66	16.24	12.85	9.17	7.02	5.40	5.03
±2160	0.5	=	off	x	0.5	485.91	42.06	25.98	18.61	12.47	8.62	6.65	4.90	3.93	2.75	2.42
±1080	1	=	off	x	1	273.55	23.55	14.41	9.83	6.85	5.08	3.89	2.96	2.17	1.68	1.41
±540	2	=	off	x	2	79.17	12.35	8.56	5.98	4.19	3.23	2.35	1.72	1.35	1.03	0.85
±270	4	=	off	x	4	245.11	8.02	5.06	3.61	2.55	1.89	1.48	1.12	0.91	0.73	0.61
±135	8	=	off	x	8	78.63	5.16	3.54	2.50	1.90	1.37	1.07	0.75	0.58	0.46	0.39
±68	16	=	off	x	16	173.38	3.47	2.39	1.77	1.35	0.93	0.76	0.59	0.40	0.30	0.30
±540	2	=	2	x	1	86.43	13.49	8.21	5.73	3.85	2.75	2.20	1.63	1.24	0.89	0.74
±270	4	=	4	x	1	31.73	6.98	4.62	3.03	2.27	1.56	1.21	0.91	0.63	0.52	0.41
±135	8	=	8	x	1	35.19	4.20	2.58	1.85	1.36	0.93	0.75	0.53	0.37	0.28	0.22
±8	128	=	8	x	16	9.44	2.91	1.98	1.39	1.00	0.73	0.56	0.38	0.27	0.19	0.14

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

RMS(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.3V, VDDA=2.4V, Vin=Ext.Short, VREF=(SDRV)/2=1.2V, at High Accyracy Mode

Max. Vin(mV) =0.9VREF(1)	OSR					64	128	256	512	1024	2048	4096	8196	16384	32768	65536
	Output rate(Hz)					15625	3906	1953	977	488	244	122	61	31	15	8
	Gain	=	PGAGN	x	ADGN											
±2160	0.25	=	off	x	0.25	172.75	55.41	32.04	23.45	16.57	10.98	8.87	6.48	4.64	3.32	2.53
±2160	0.5	=	off	x	0.5	88.54	29.11	17.86	12.45	8.25	6.04	4.82	3.32	2.41	1.85	1.30
±1080	1	=	off	x	1	42.21	15.82	10.11	7.08	4.87	3.48	2.66	1.92	1.36	1.07	0.78
±540	2	=	off	x	2	22.46	9.20	5.98	4.22	3.00	2.06	1.65	1.14	0.86	0.63	0.48
±270	4	=	off	x	4	13.40	5.52	3.74	2.60	1.88	1.31	1.02	0.74	0.54	0.42	0.32
±135	8	=	off	x	8	6.53	3.64	2.50	1.75	1.28	0.93	0.73	0.52	0.35	0.27	0.21
±68	16	=	off	x	16	4.28	2.62	1.72	1.33	0.91	0.71	0.56	0.40	0.25	0.18	0.15
±540	2	=	2	x	1	21.48	9.27	5.60	4.11	2.81	2.13	1.63	1.15	0.83	0.60	0.45
±270	4	=	4	x	1	10.72	5.14	3.39	2.37	1.62	1.18	0.93	0.63	0.44	0.32	0.25
±135	8	=	8	x	1	6.80	3.01	2.09	1.36	0.97	0.71	0.55	0.41	0.29	0.19	0.14
±8	128	=	8	x	16	3.54	2.46	1.65	1.20	0.77	0.59	0.42	0.28	0.21	0.15	0.11

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

Table6.8-2 SD18 RMS Noise Table

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \frac{\ln\left(\frac{FSR}{RMS\ Noise}\right)}{\ln(2)}$$

$$RMS\ Noise = \frac{\left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right)}{2^{23}}$$

$$Where\ FSR\ (Full - Scale\ Range) = 2 \times VREF/Gain.$$

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$

6.8.4. SD18 ,Temperature Sensor

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			-272		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

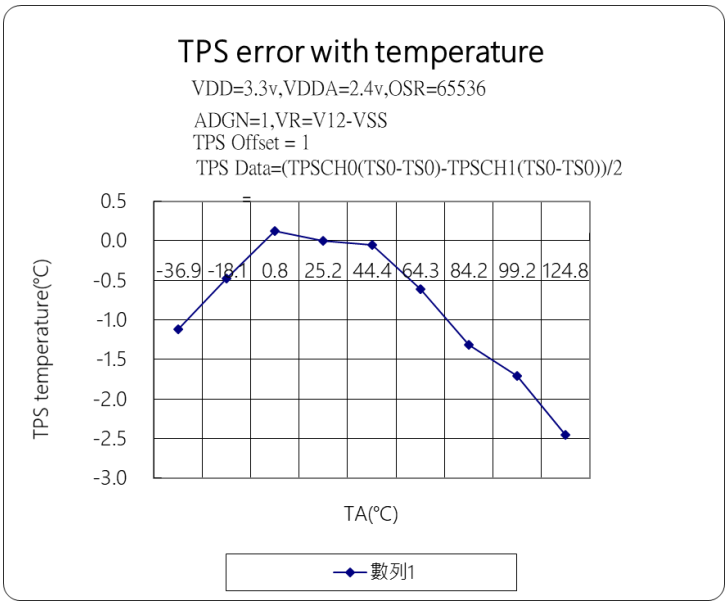


Figure 6.8-3 ADC Temperature Error

6.9. Build-In EPROM(BIE)

TA = 25℃,VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{BIE}	Supply Voltage at VPP PIN			8.5	8.75	V
I_{BIE}	Operation supply current			3		mA
V_{SS}	Supply Voltage			0		V
When connecting to the external VBIE power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.						

6.10. Build-In EPROM(BIE) Low voltage control circuit

TA = 25℃,VDD = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		2.75		5.5	V
V_{SS}	Supply Voltage			0		V
When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external VBIE power source.						

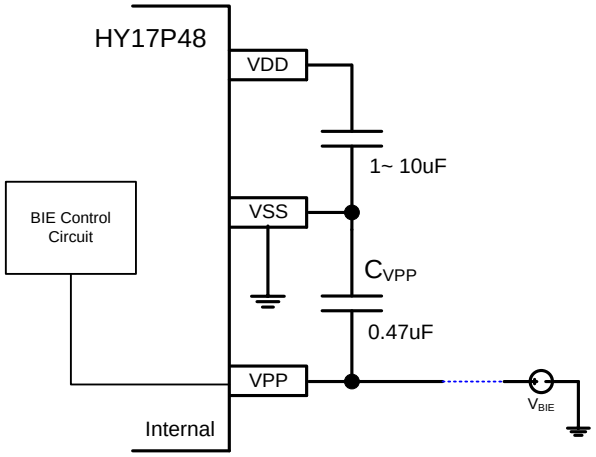


Figure 6.10-1 BIE typical application circuit

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY17P48-D000	Die	-	D	000	000	Tray	250	Green[4]	-
HY17P48-NS32	QFN	32	N	S32	000	Tape & Reel	5000	Green[4]	MSL-3
HY17P48-ES28	SSOP	28	E	S28	000	Tube	50	Green[4]	MSL-3
HY17P48-ES28	SSOP	28	E	S28	000	Tape & Reel	3000	Green[4]	MSL-3
HY17P48-ES20	SSOP	20	E	S20	000	Tube	58	Green[4]	MSL-3
HY17P48-ES20	SSOP	20	E	S20	000	Tape & Reel	3000	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code (Blank Code/ Standard/Customized Programming Code)**

Ex: You request blank code in Die package. The device No. will be HY17P48-D000.
Ex: Your customized programming code is 007 and you require products in Die package. The device No. will be HY17P48-D000-007. and please clearly indicate the shipment packing type when placing orders.
Ex: You request blank code in SSOP28 package. The device No. will be HY17P48-ES28. and please clearly indicate the shipment packing type when placing orders.
Ex: Your customized programming code is 005 and you require products in SSOP28 package. The device No. will be HY17P48-ES28-005. and please clearly indicate the shipment pack ing type when placing orders.
Ex: You request blank code in SSOP20 package. The device No. will be HY17P48-ES20. and please clearly indicate the shipment packing type when placing orders.
Ex: Your customized programming code is 009 and you require products in SSOP20 package. The device No. will be HY17P48-ES20-009. and please clearly indicate the shipment pack ing type when placing orders.
Ex: You request blank code in QFN32 package. The device No. will be HY17P48-NS32. and please clearly indicate the shipment packing type when placing orders.
Ex: Your customized programming code is 007 and you require products in QFN32 package. The device No. will be HY17P48-NS32-007. and please clearly indicate the shipment pack ing type when placing orders.

[2] Code

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] MSL:

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

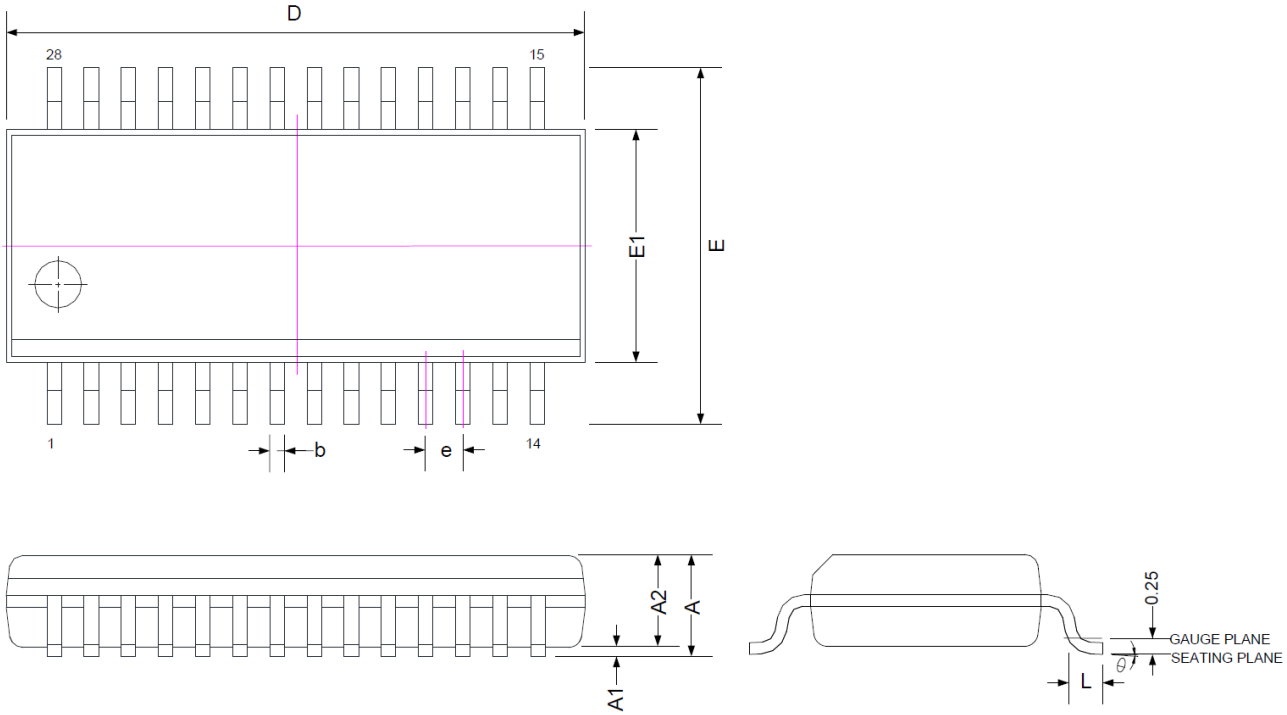
[4] Green (RoHS & no Cl/Br):

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

8. Package Information

8.1. SSOP28(ES28)

8.1.1. Package Dimensions SSOP28(150mil)



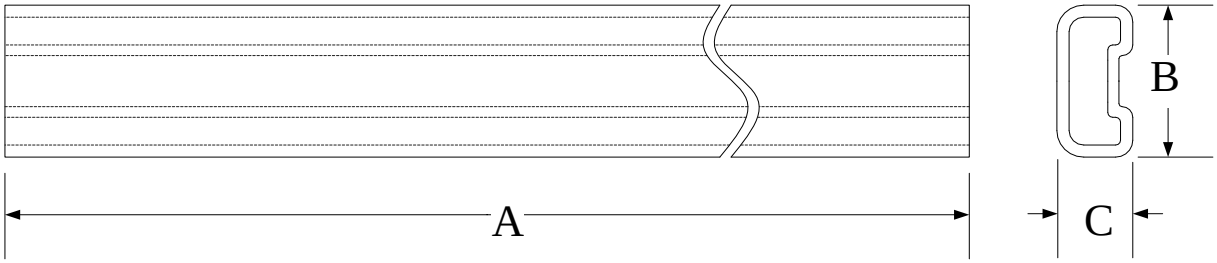
SYMBOLS	MIN	NOM	MAX
A	1.34	1.63	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	9.80	9.91	10.01
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	0.64	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.1.2. Tube Dimensions SSOP28(150mil) (ES28)

Unit : mm

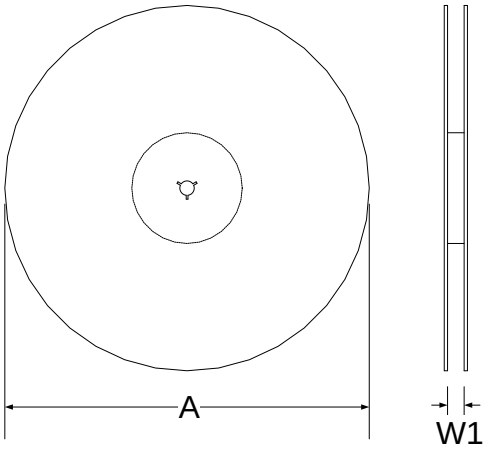


SYMBOLS	A	B	C
Spec.	529.6±1.0	8.001±0.127	3.937±0.127

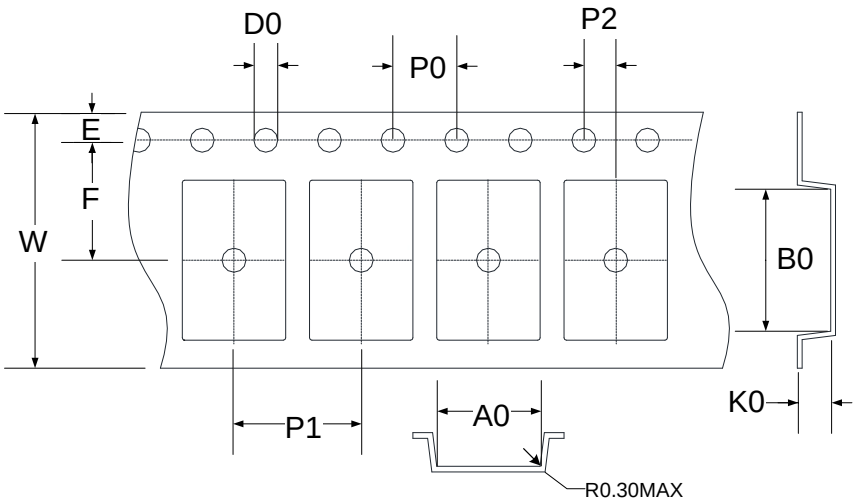
8.1.3. Tape & Reel Information

8.1.3.1. Reel Dimensions

Unit: mm



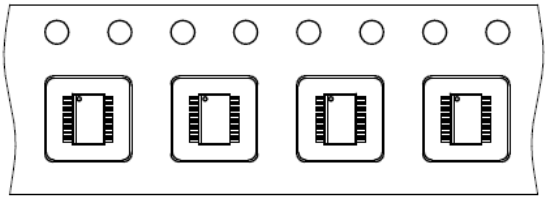
8.1.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	10.30	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

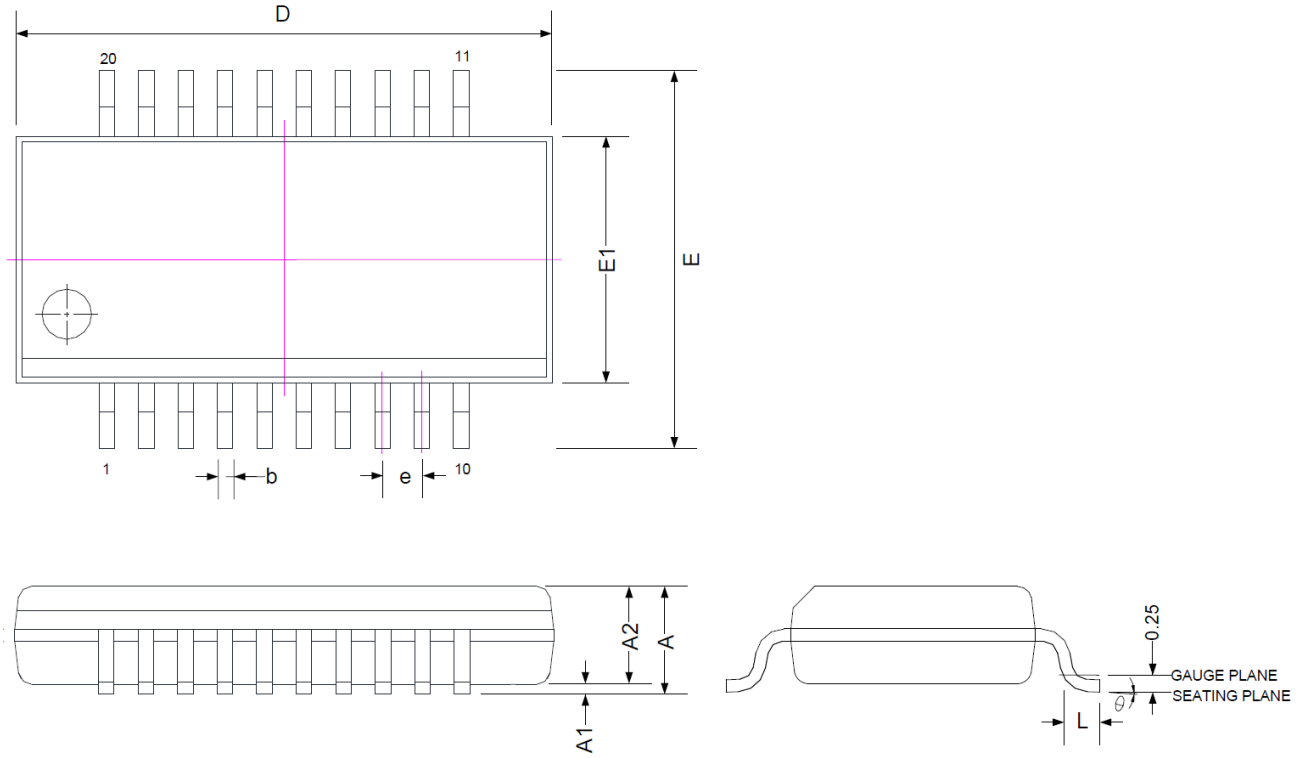
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.1.3.3. Pin1 direction



8.2. SSOP20(ES20)

8.2.1. Package Dimensions SSOP20(150mil)



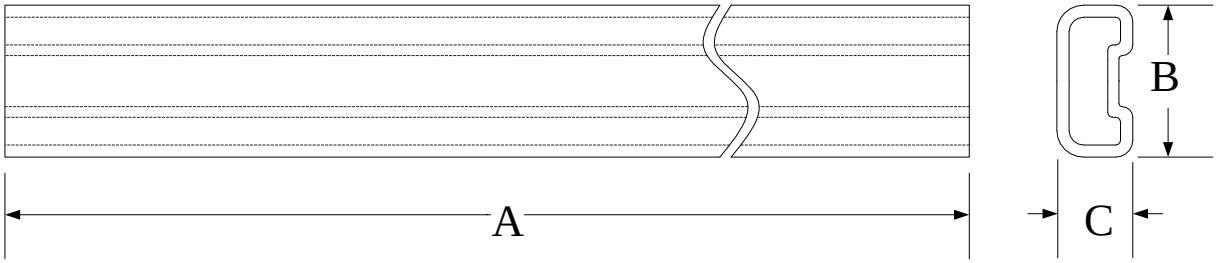
SYMBOLS	MIN	NOM	MAX
A	1.34	1.63	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	8.55	8.66	8.74
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	0.64	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MS-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2.2. Tube Dimensions SSOP20(150mil) (ES20)

Unit : mm

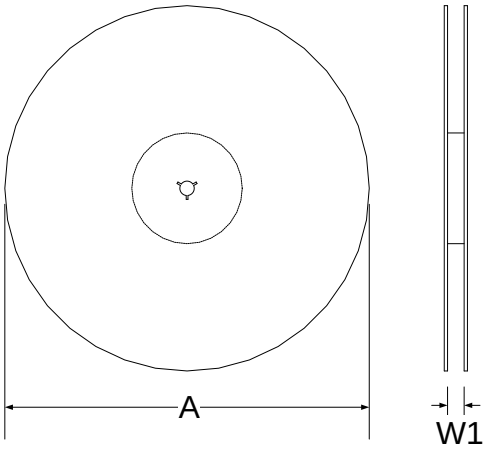


SYMBOLS	A	B	C
Spec.	529.6±1.0	8.001±0.127	3.937±0.127

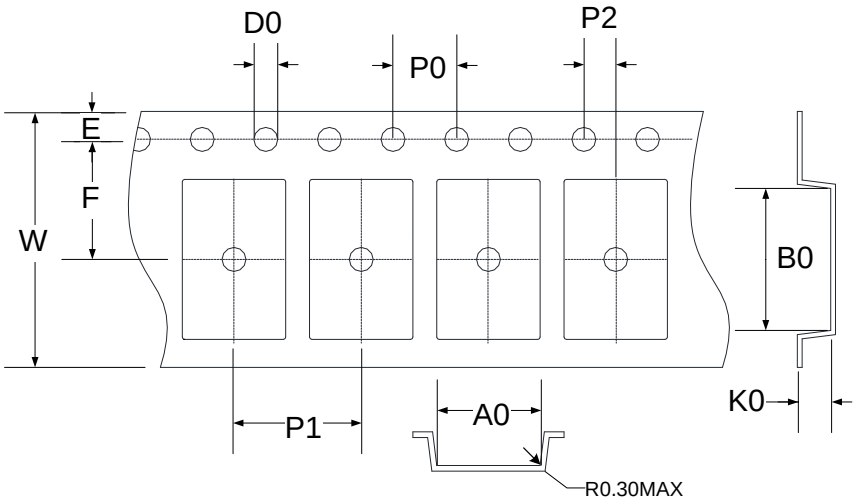
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions

Unit: mm



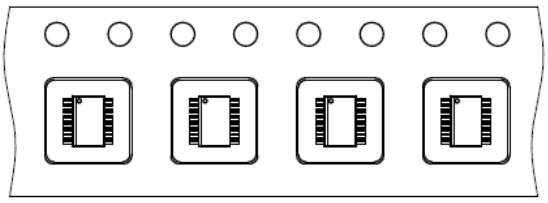
8.2.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	9.50	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

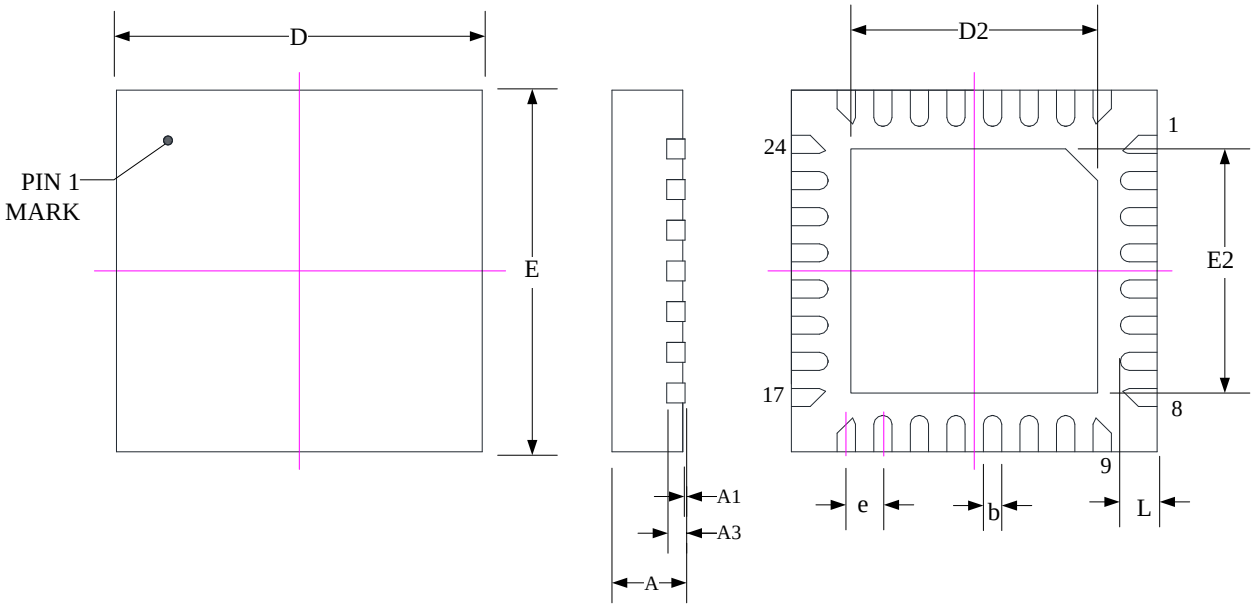
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.2.3.3. Pin1 direction



8.3. QFN32(NS32)

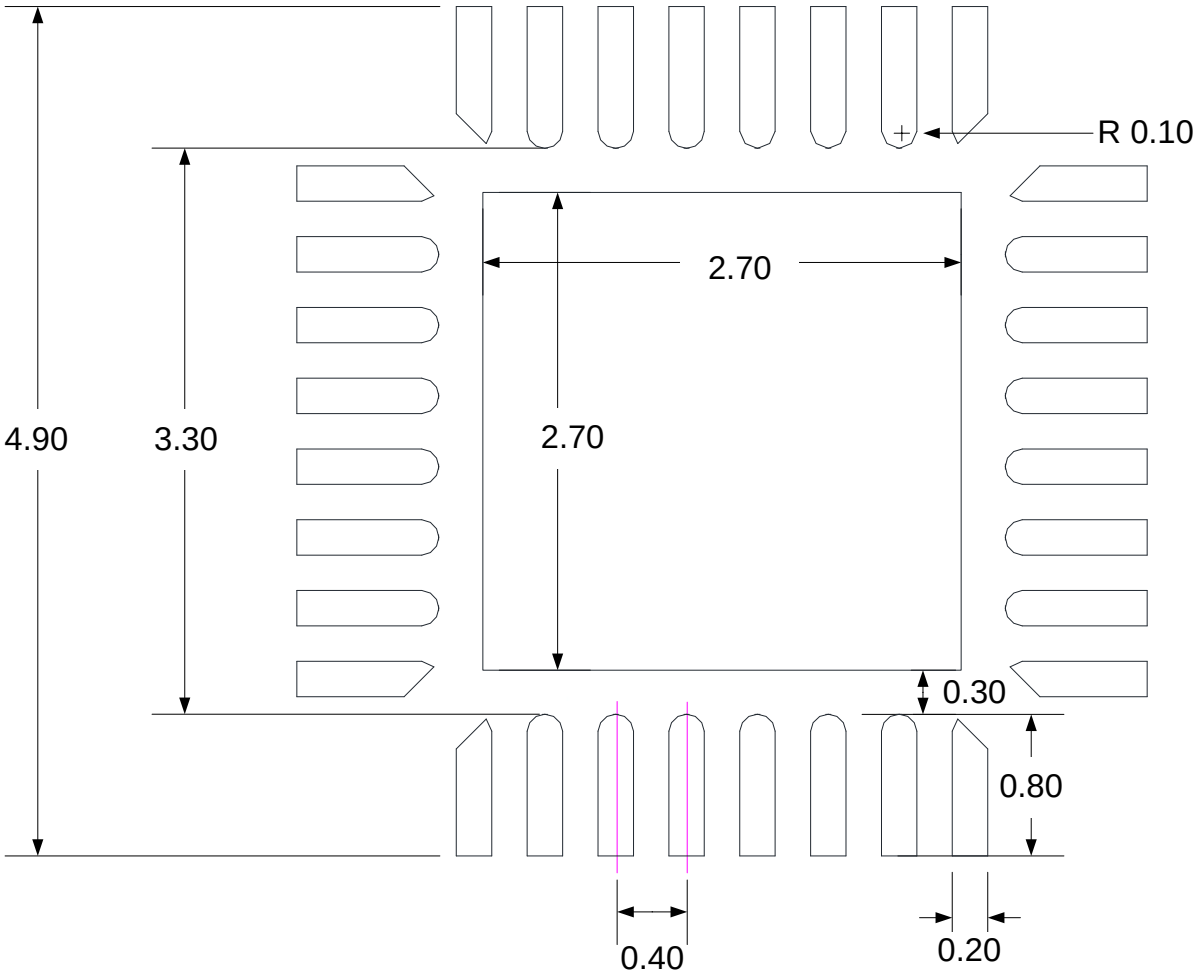
8.3.1. Package Dimensions QFN32(4x4x0.55)



SYMBOLS	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.15 REF.		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.25	0.30	0.35
e	0.40 BASIC		

Note:
1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf

8.3.2. Land Pattern Design Recommendations

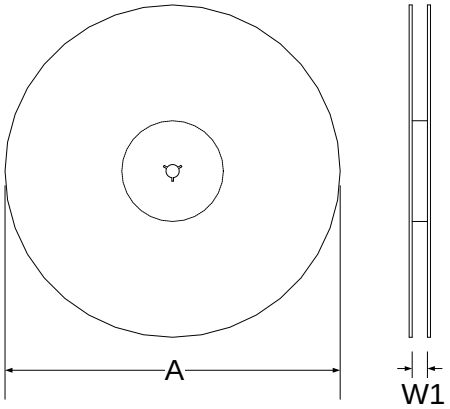


Note:
1. Publication IPC-7351 is recommended for alternate designs.
2. http://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf
3. Unit: mm.

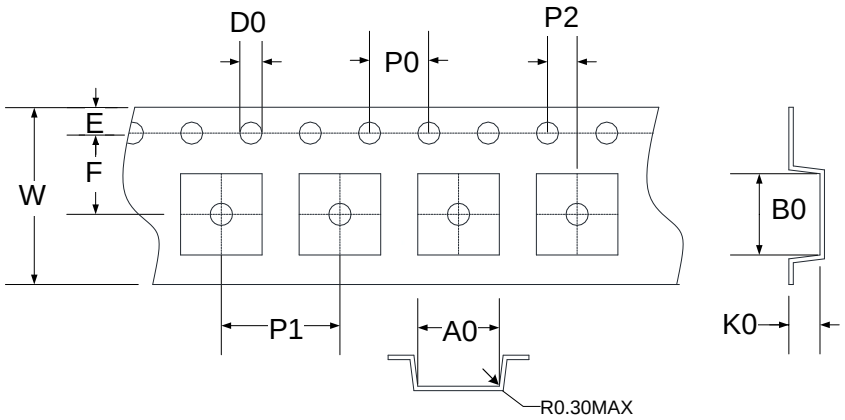
8.3.3. Tape & Reel Information

8.3.3.1. Reel Dimensions

Unit: mm



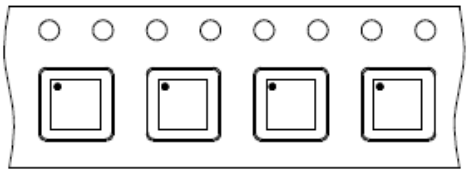
8.3.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	4.35	4.35	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

Pin1 direction



9. Revision Record

Major differences are stated thereinafter.

Version	Page	Date	Revision Summary
V03	All	2019/05/30	First edition
V05	22~23	2020/04/28	Update register table.
	6~9		Update I2C,UART pin. Remove AI14,AI15
	17,24		Update AIE register. Update GPIO block diagram
	27		Adding Oscillator=32768Hz current
	41		Update SSOP20 Unit Q'ty
V07	23	2021/09/11	Update register table.Add INIS1,VRIS,INIS
	31~32		Add BOR、Reset timing diagram
	14		Update Reset block diagram
V08	All	2023/01/9	Add HY17P48-NS32 (QFN32 4x4x0.55) product informations