# HY17P51
# Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x14 LCD Driver
Embedded High Resolution ΣΔADC

## Table of Contents

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# 1. Features

- 8-Bit RISC-like microcontrollers with 71 high-performance instruction set H08D (same as H08A),support C compiler
- Operating voltage and operating temperature range
  - VDD : 2.0V ~ 5.5V
  - VDDA : 2.4V ~ 5.0V
  - -40°C ~ 85°C
- Internal High Precision RC Oscillator, Many CPU clock rates enable users to have the most power-saving plan.
  - Active mode
  - Idle mode
  - Sleep mode
- Memory
  - 4K words OTP program memory
  - 256 bytes data memory
  - Support 8 stack level
- Reset
  - Power On Reset
  - Brown Out Reset
  - Watch Dog Reset
  - Stack Over Reset
- 4 X 14 LCD Driver
  - 1/4 Duty 1/3 Bias
  - Built-in charge pump regulated circuit providing 8 LCD bias voltage
  - 2 SEG ports can set as digital input and output
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function
- VDDA has 10mA regulated voltage source output, wtuh fast start function to provide sensor driving voltage.
- 24-Bit ΣΔADC
  - Built-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x
  - Zero point bias translation controller
  - Sampling frequency 921KHz
  - Settable over-sampling rate is 64~65536
  - Diverse data output rate. Max. 7.1Ksps
  - Built-in absolute temperature sensor
- Timer
  - Watch Dog
    - Reset event
    - Interrupt event
  - 1 channels 8-bit Timer A1
    - Interrupt event
    - Compare events
- 64 words Built-In EPROM (BIE), 2.75V low voltage programming control circuit
- Interface
  - 1 channels serial communication EUART module
- Package
  - QFN16
  - QFN32

**Function List**

| Model No. | VDD (V) | Internal Clock (Hz) | System Clock (Hz) | Program Memory (word) | SRAM (byte) | BIE (byte) | ADC ENOB (bit x ch) | Sample Rate (sps) | LCD (com x seg) | I/O | Timer (bit x ch) | PWM (bit x ch) | Serial Interface (I/F x ch) | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HY17P51 | 2.0~ 5.5 | 14.5K 1.843M 3.686M 7.834M | 14.5K ~ 8M | 4K | 256 | 64LV | 20-bit x4 | 8~7.1K | - | 8 | 8-bit x 1 | - | EUART | QFN16 |
| | | | | | | | | | 4 x 14 | | | | | QFN32 |

# 2. Pin Definition

## 2.1. QFN32 Pin Diagram

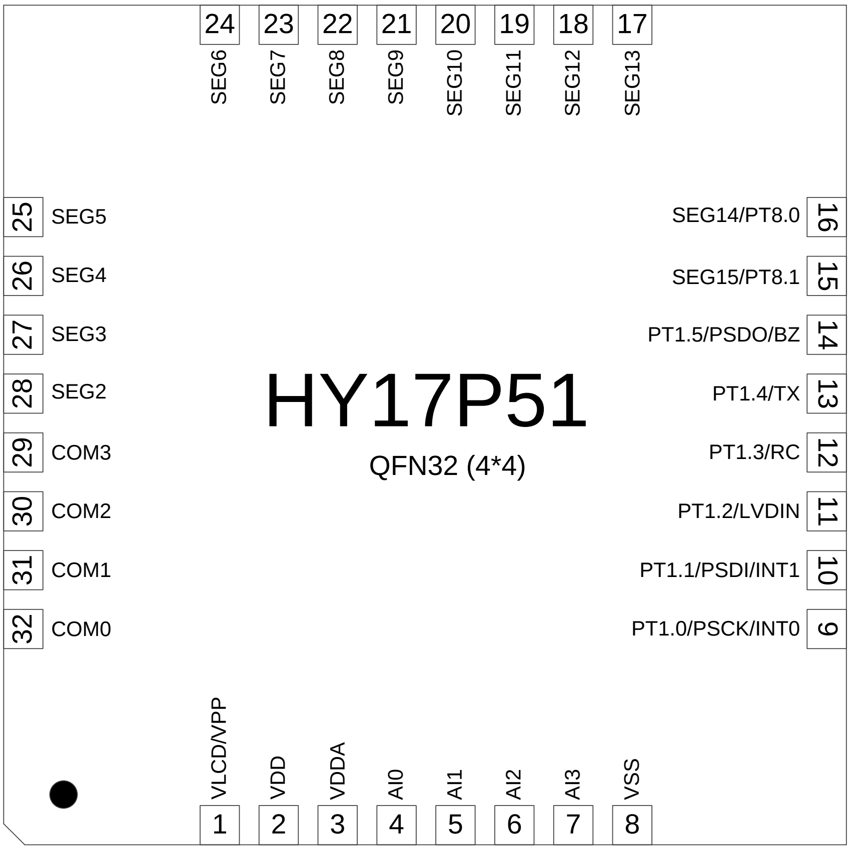



Figure 2-1 QFN32 Pin Diagram

Note: VPP and VLCD reuse the same PIN, input of high voltage is prohibited when OTP is not burned

## 2.2. QFN16 Pin Diagram

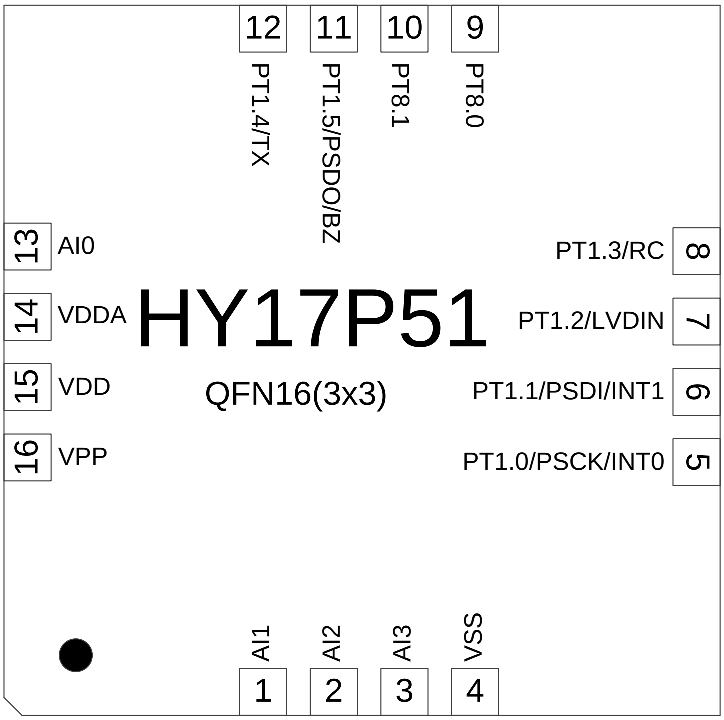



Figure 2-2 QFN16 Pin Diagram

Note: VPP and VLCD reuse the same PIN, input of high voltage is prohibited when OTP is not burned

## 2.3. Pinout I/O Description

"I/O"Inout/Output,"I"Input,"O"Output,"S"Smith triggers,"C"CMOS,"P"Power Source,"A"Analog channel

| Package / Pin No. | | Pin Name | Characteristic | | Description |
|---|---|---|---|---|---|
| QFN32 (4x4) | QFN16 (3x3) | | Type | Buffer | |
| 1 | 16 | VLCD/VPP | | | |
| | | VLCD | P | P | Power Source of LCD |
| | | VPP | P | P | OTP burning voltage source input pin |
| 2 | 15 | VDD | P | P | Chip Power Voltage Input, an external 1~10uF capacitor is required. |
| 3 | 14 | VDDA | P | P | LDO output, Analog circuit voltage source, an external 1~10uF capacitor is required. (source: VDD) |
| 4 | 13 | AI0 | A | A | Analog input channel 0 |
| 5 | 1 | AI1 | A | A | Analog input channel 1 |
| 6 | 2 | AI2 | A | A | Analog input channel 2 |
| 7 | 3 | AI3 | A | A | Analog input channel 3 |
| 8 | 4 | VSS | P | P | System Power Ground |
| 9 | 5 | PT1.0/INT1.0/PSCK | | | |
| | | PT1.0 | I/O | S/C | Digital input / Output pin |
| | | INT1.0 | I | S | External interrupt source input pin |
| | | PSCK | I | S | OTP read / write interface pin, PSCK |
| 10 | 6 | PT1.1/INT1.1/PSDI | | | |
| | | PT1.1 | I/O | S/C | Digital input / Output pin |
| | | INT1.1 | I | S | External interrupt source input pin |
| | | PSDI | I | S | OTP read / write interface pin, PSDI |
| 11 | 7 | PT1.2/LVDIN | | | |
| | | PT1.2 | I/O | S/C | Digital input / Output pin |
| | | LVDIN | A | A | LVD external signal input port |
| 12 | 8 | PT1.3/RC | | | |
| | | PT1.3 | I/O | S/C | Digital input / Output pin |
| | | RC | I | S | RC pin of EUART interface |
| 13 | 12 | PT1.4/TX | | | |
| | | PT1.4 | I/O | S/C | Digital input / Output pin |
| | | TX | O | C | TX pin of EUART interface |
| 14 | 11 | PT1.5/PSDO/BZ | | | |
| | | PT1.5 | I/O | S/C | Digital input / Output pin |
| | | PSDO | O | C | OTP read / write interface pin, PSDO |
| | | BZ | O | C | Buzzer Signal Output pin |

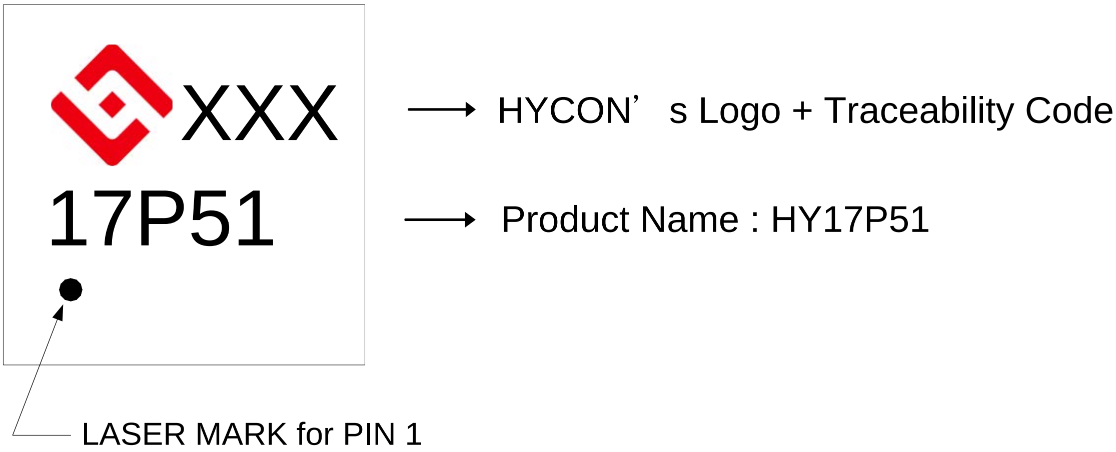
| Package / Pin No. | | Pin Name | Characteristic | | Description |
|---|---|---|---|---|---|
| QFN32 (4x4) | QFN16 (3x3) | | Type | Buffer | |
| 15 | 10 | PT8.1/SEG15 | | | |
| | | PT8.1 | I/O | S/C | Digital input / Output pin |
| | | SEG15 | O | A | LCD Segment Output pin |
| 16 | 9 | PT8.0/SEG14 | | | |
| | | PT8.0 | I/O | S/C | Digital input / Output pin |
| | | SEG14 | O | A | LCD Segment Output pin |
| 17 | - | SEG13 | | | |
| | | SEG13 | O | A | LCD Segment Output pin |
| 18 | - | SEG12 | | | |
| | | SEG12 | O | A | LCD Segment Output pin |
| 19 | - | SEG11 | | | |
| | | SEG11 | O | A | LCD Segment Output pin |
| 20 | - | SEG10 | | | |
| | | SEG10 | O | A | LCD Segment Output pin |
| 21 | - | SEG9 | | | |
| | | SEG9 | O | A | LCD Segment Output pin |
| 22 | - | SEG8 | | | |
| | | SEG8 | O | A | LCD Segment Output pin |
| 23 | - | SEG7 | | | |
| | | SEG7 | O | A | LCD Segment Output pin |
| 24 | - | SEG6 | | | |
| | | SEG6 | O | A | LCD Segment Output pin |
| 25 | - | SEG5 | | | |
| | | SEG5 | O | A | LCD Segment Output pin |
| 26 | - | SEG4 | | | |
| | | SEG4 | O | A | LCD Segment Output pin |
| 27 | - | SEG3 | | | |
| | | SEG3 | O | A | LCD Segment Output pin |
| 28 | - | SEG2 | | | |
| | | SEG2 | O | A | LCD Segment Output pin |
| 29 | - | COM3 | | | |
| | | COM3 | O | A | LCD COM Output pin |
| 30 | - | COM2 | | | |
| | | COM2 | O | A | LCD COM Output pin |

| Package / Pin No. | | Pin Name | Characteristic | | Description |
|---|---|---|---|---|---|
| QFN32 (4x4) | QFN16 (3x3) | | Type | Buffer | |
| 31 | - | COM1<br>COM1 | O | A | LCD COM Output pin |
| 32 | - | COM0<br>COM0 | O | A | LCD COM Output pin |

Table 2-1 Pin Definition and Function Description

### 2.4. Package marking information

#### 2.4.1. QFN Package marking information



# 3. Application Circuit

## 3.1. Bridge Sensor with LCD display

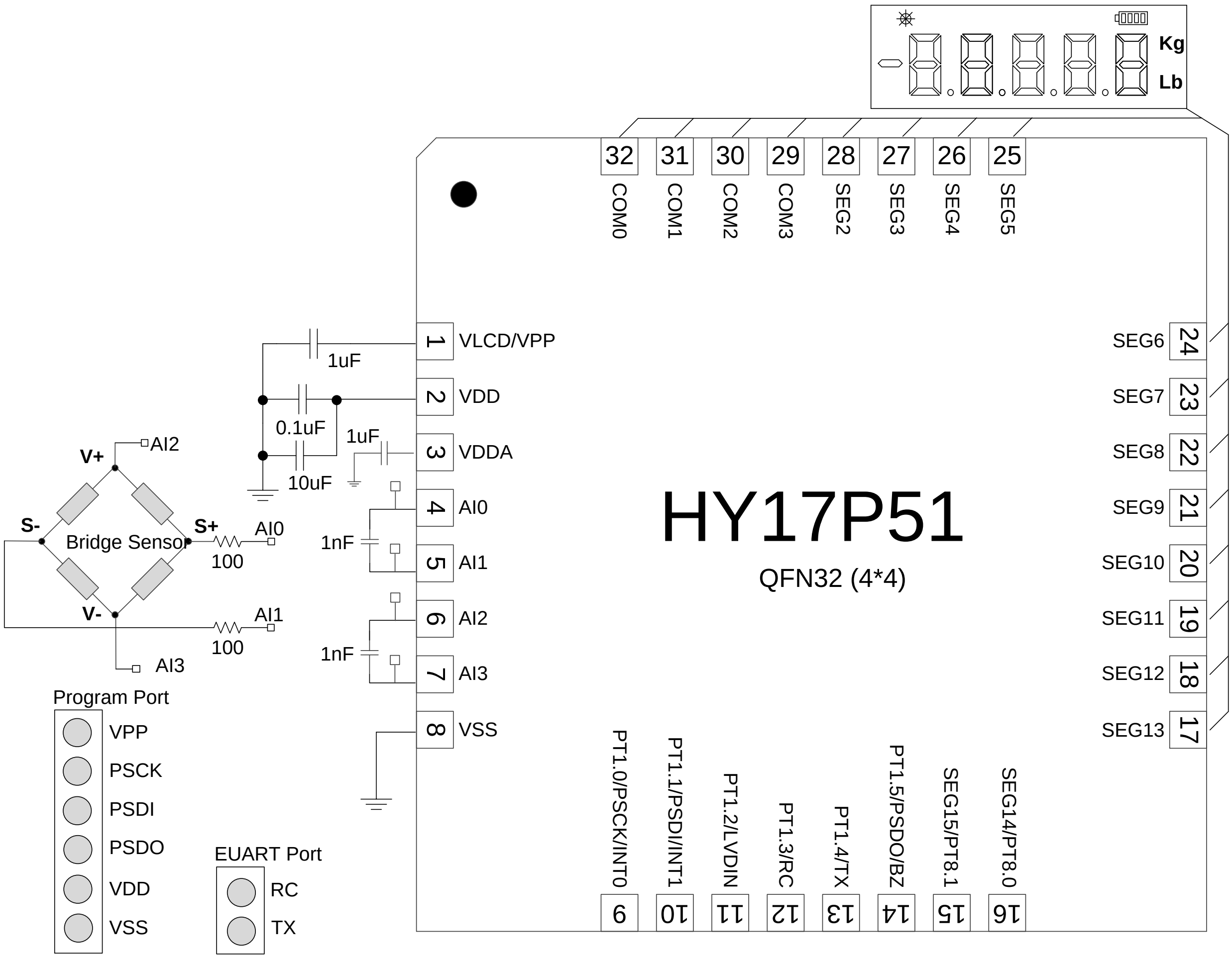



Figure 3-1 Bridge Sensor application reference circuit

## 3.2. Digital Thermometer with LCD display

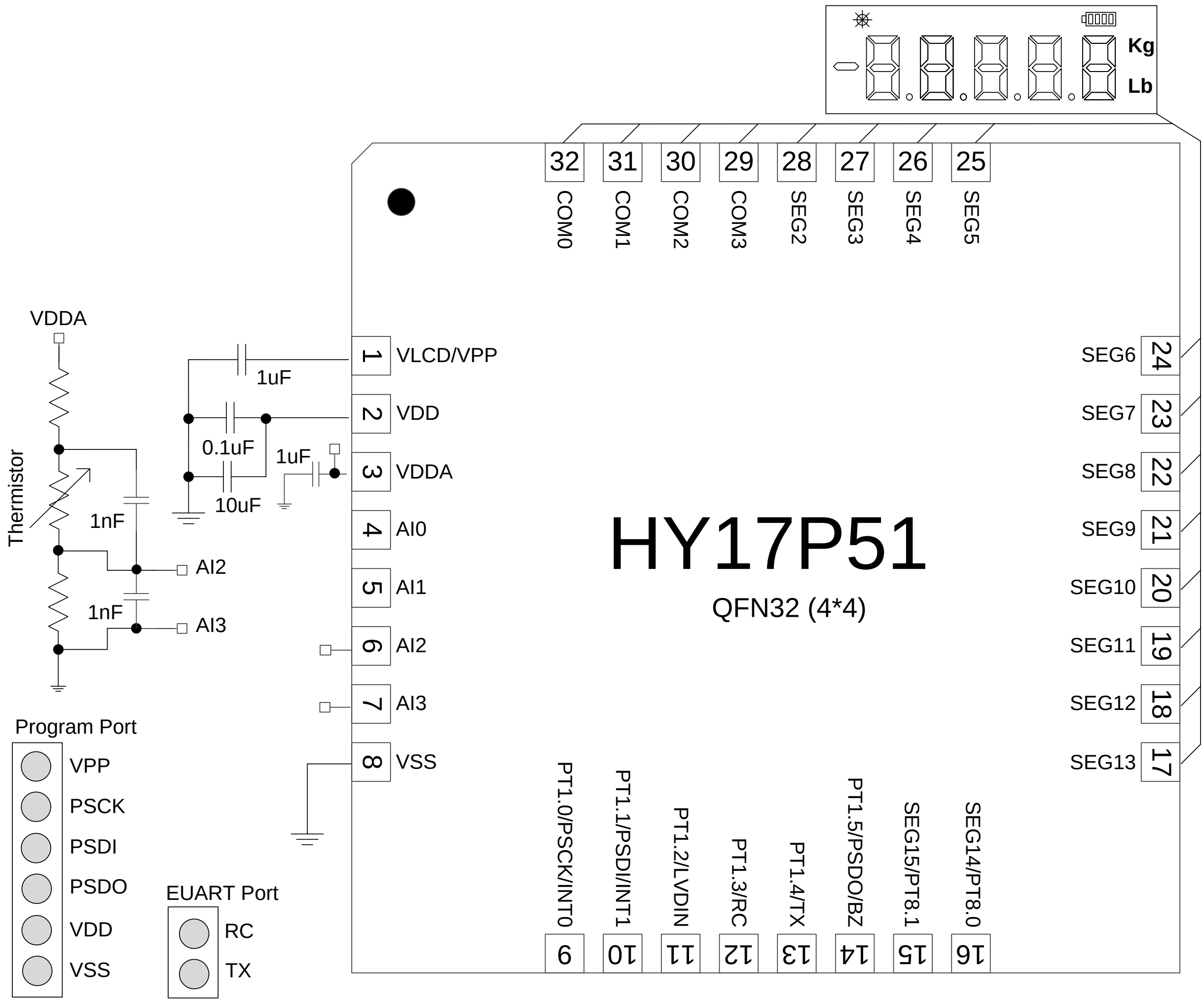



Figure 3-2 Digital Thermometer application reference circuit

# 4. Function Outline

## 4.1. Internal Block Diagram

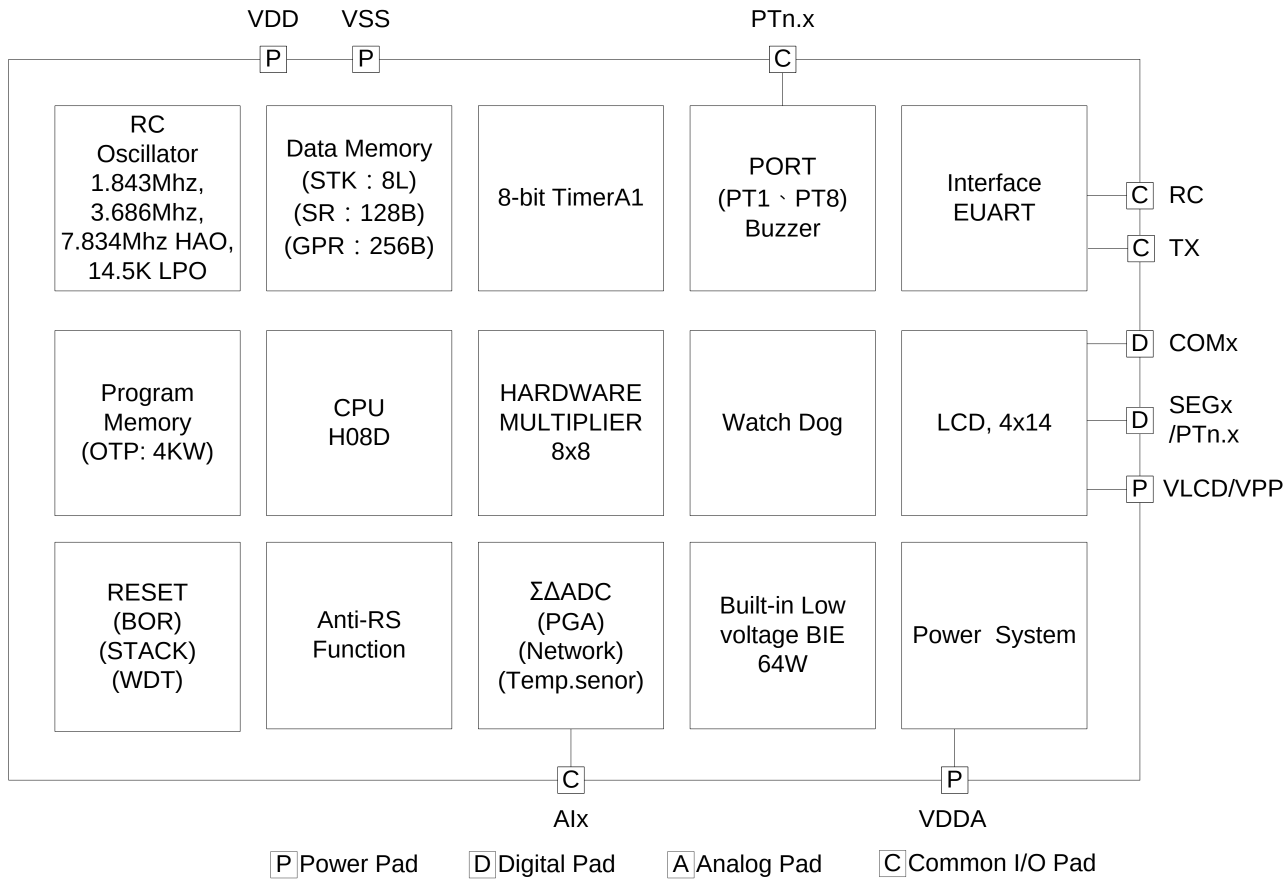



Figure 4-1 Internal Block Diagram

## 4.2. Related Description and Supporting Document

| File Name | Description |
|---|---|
| DS-HY17P51 | HY17P51 Datasheet |
| UG-HY17S58 | HY17S58 chip User's Manual |
| APD-CORE002 | H08A, H08C, H08D Instruction Set User's Manual |
| APD-HY17PIDE001 | HY17P Series development tool software User's Manual |
| APD-HY17PIDE002 | HY17P Series development tool hardware User's Manual |
| APD-HYIDE016 | H08 C IDE software User's Manual |
| APD-HY17PIDE003 | HY17P4x/5x Series Peripheral Driver C Library User's Manual |
| APD-HY17PIDE004 | HY17P Series HexLoader User's Manual |
| APD-HYIDE014 | HY10000-WK08D Integrated Writer software User's Manual |
| APD-HYIDE013 | HY10000-WK08D Integrated Writer hardware User's Manual |

## 4.3. Clock System

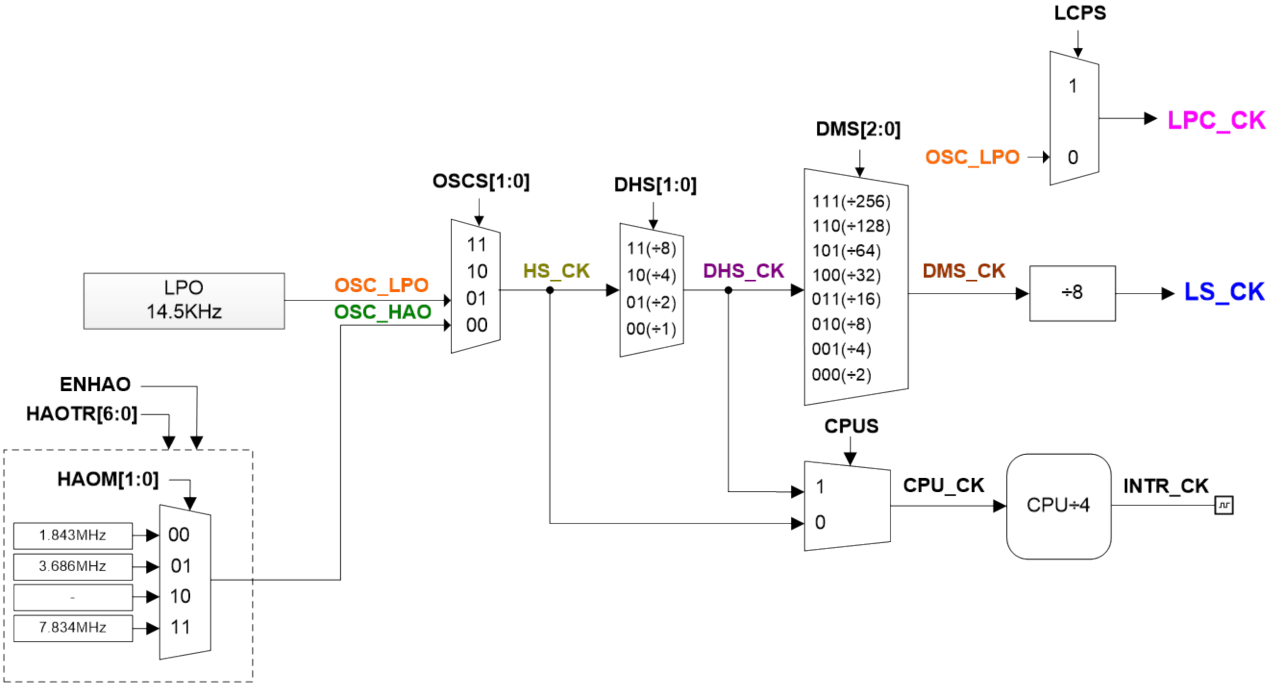



Figure 4-2 Clock System block diagram (1)

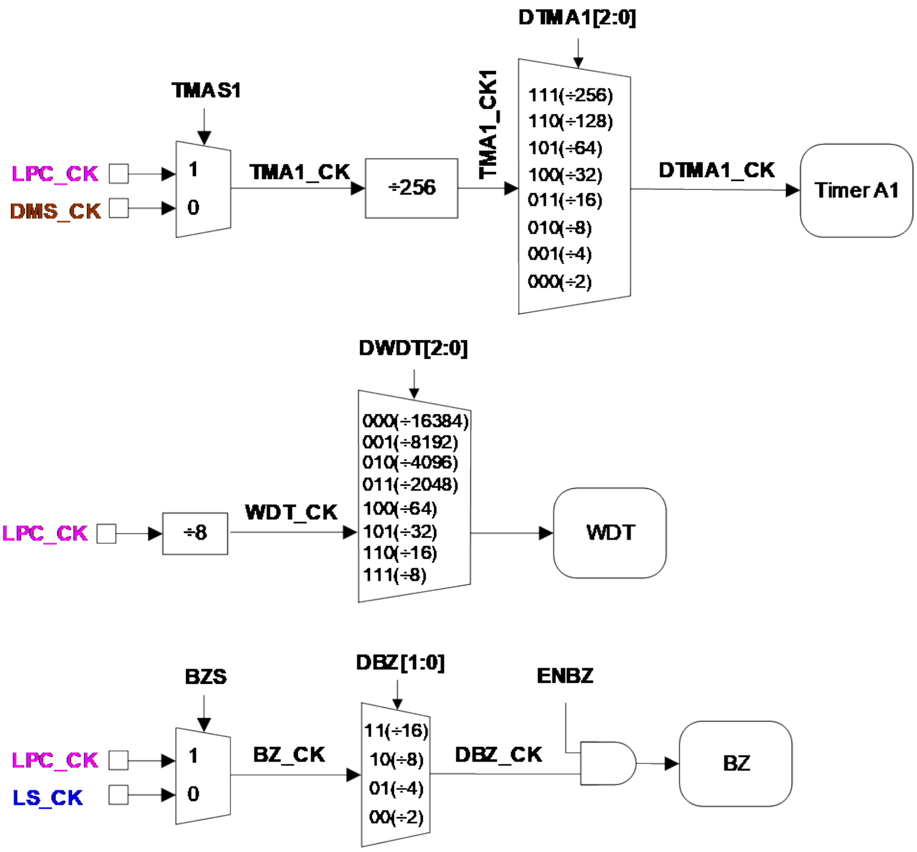



Figure 4-3 Clock System block diagram (2)

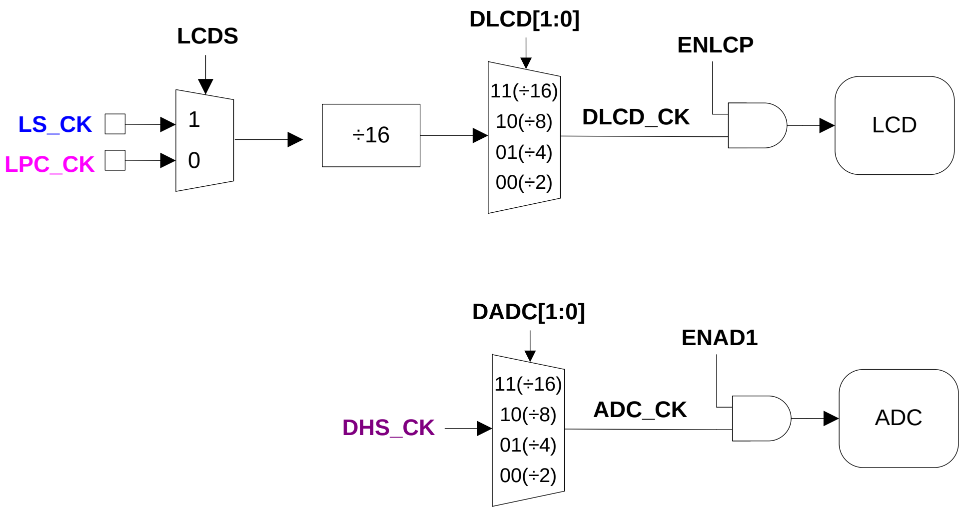



Figure 4-4 Clock System block diagram (3)

## 4.4. Low Voltage Detect(LVD)

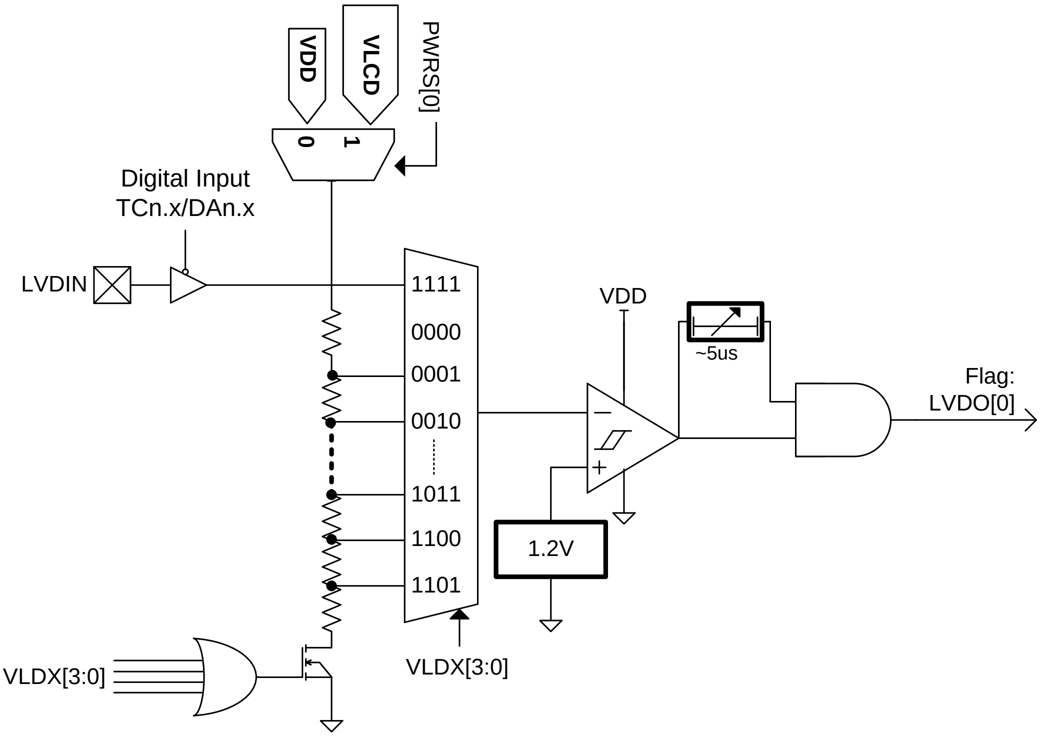



Figure 4-5 Low Voltage Detect block diagram

## 4.5. Reset

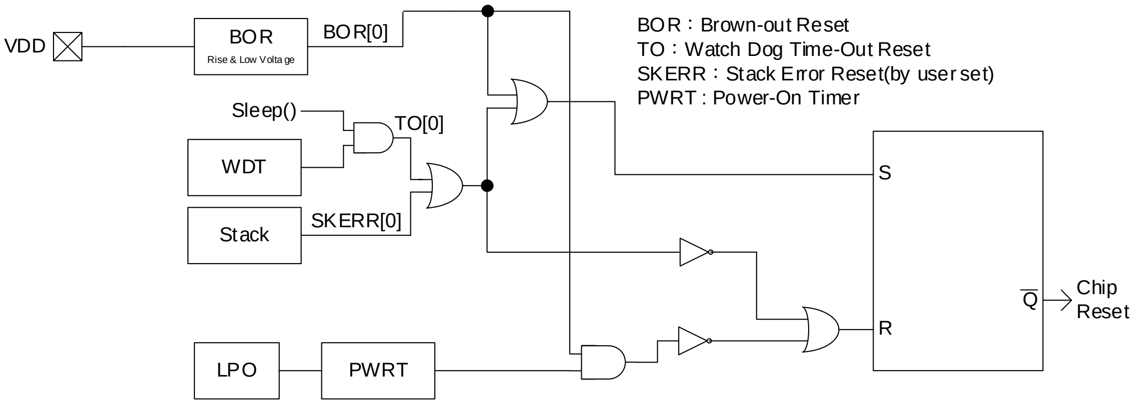



Figure 4-6 Reset block diagram

## 4.6. Power System

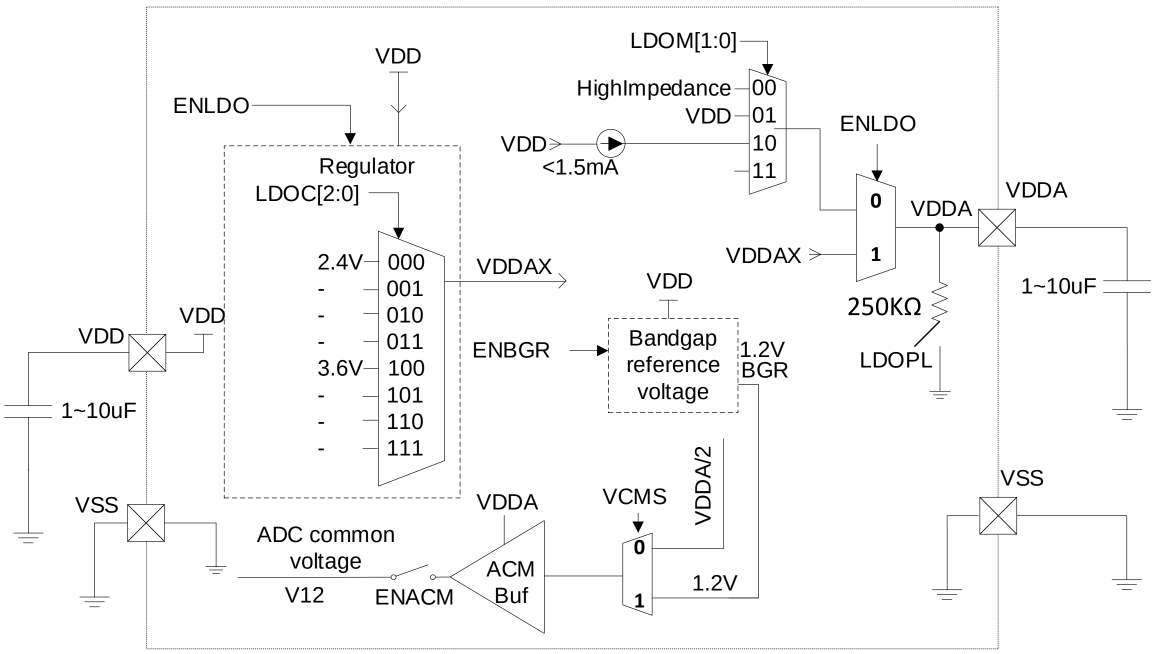
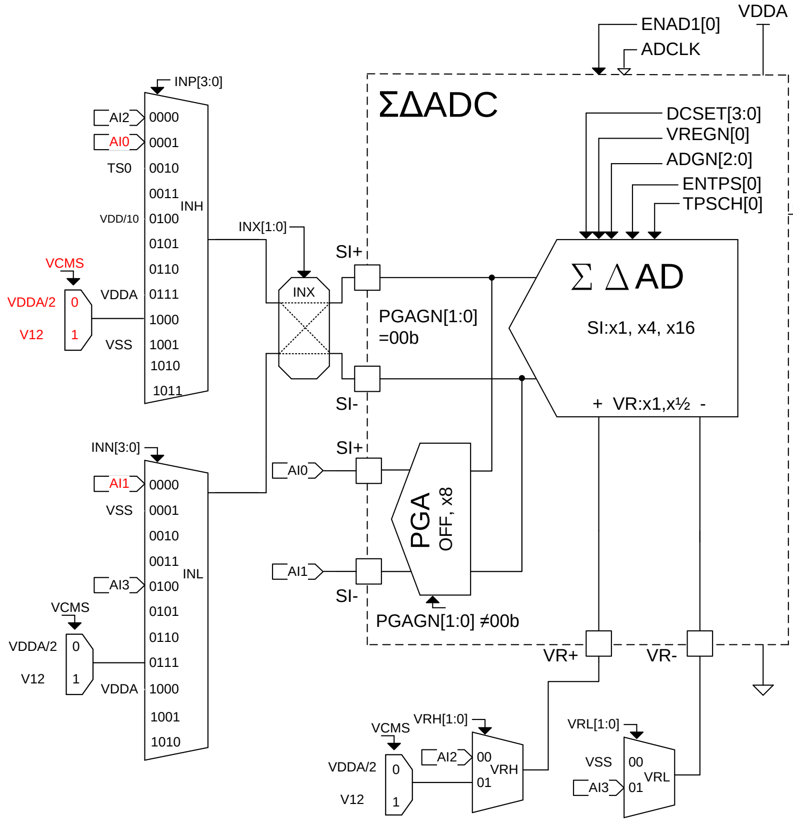



Figure 4-7 Power System block diagram

## 4.7. ΣΔADC Network




| OSR | Comb filter Order |
|---|---|
| 65536 | 2nd |
| 32768 | 2nd |
| 16384 | 2nd |
| 8192 | 2nd |
| 4096 | 2nd |
| 2048 | 2nd |
| 1024 | 3rd |
| 512 | 3rd |
| 256 | 3rd |
| 128 | 3rd |
| 64 | 3rd |

Figure 4-8 ΣΔADC Network

## 4.8. GPIO PT1

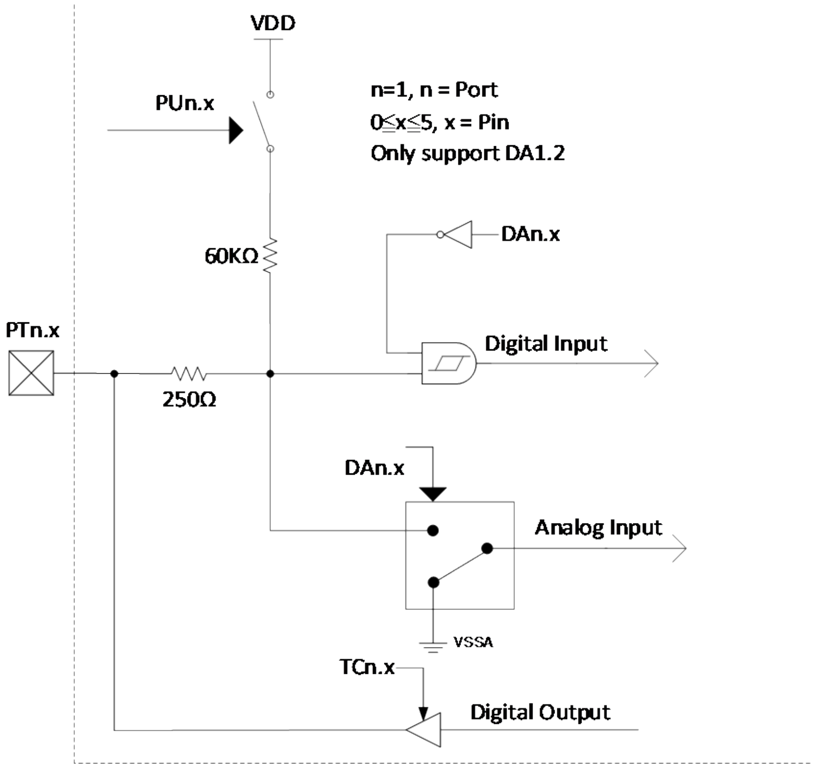



Figure 4-9 GPIO PT1 block diagram

## 4.9. GPIO PT8/SEG14~SEG15

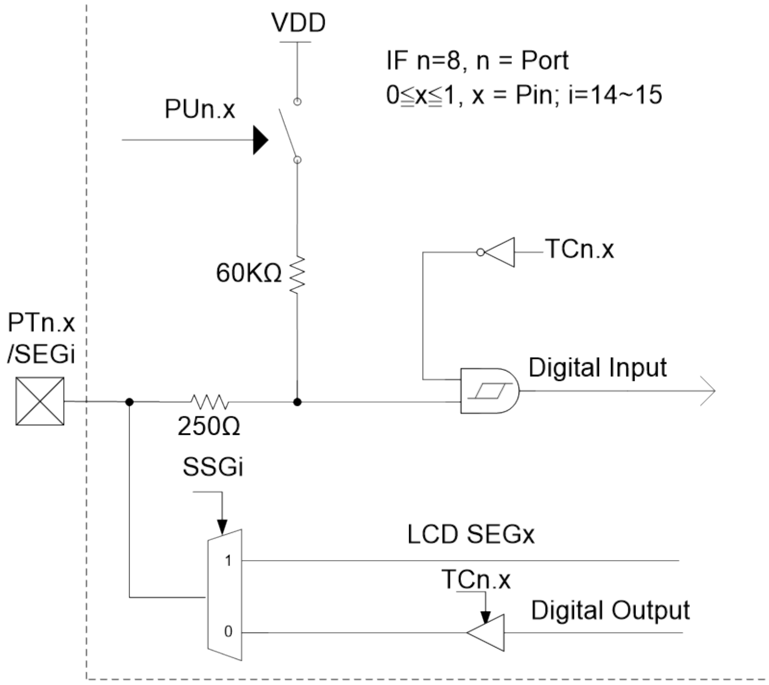



Figure 4-10 GPIO PT8/SEG14~SEG15 block diagram

## 4.10. Watch Dog

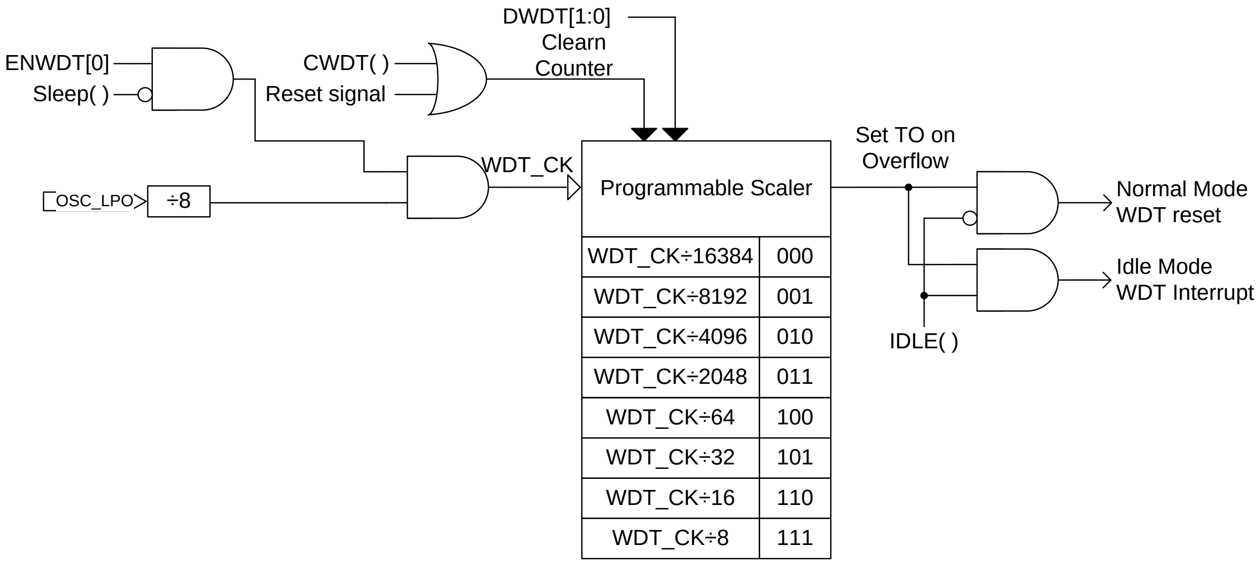



Figure 4-11 Watch Dog block diagram

## 4.11. 8-bit Timer A1

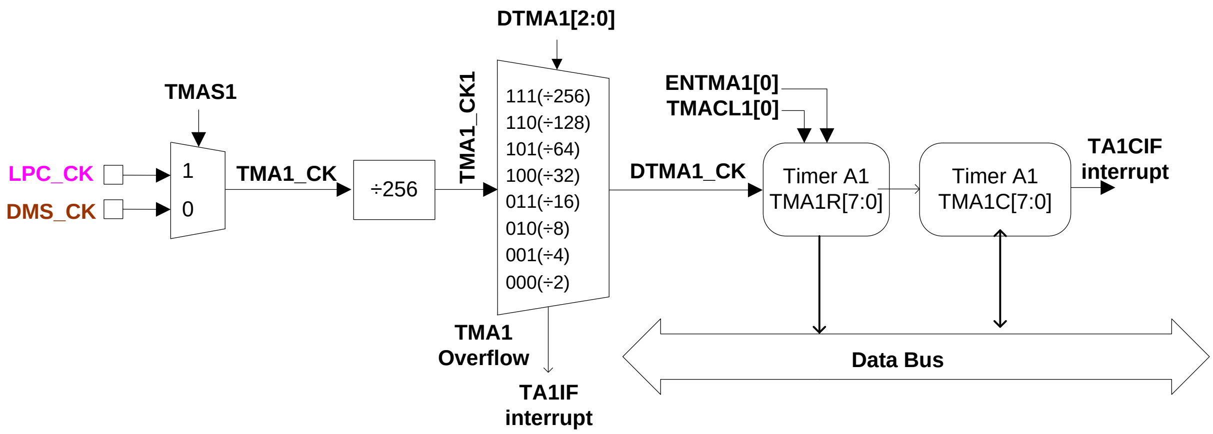



Figure 4-12 8-bit Timer A1 block diagram

### 4.12. LCD

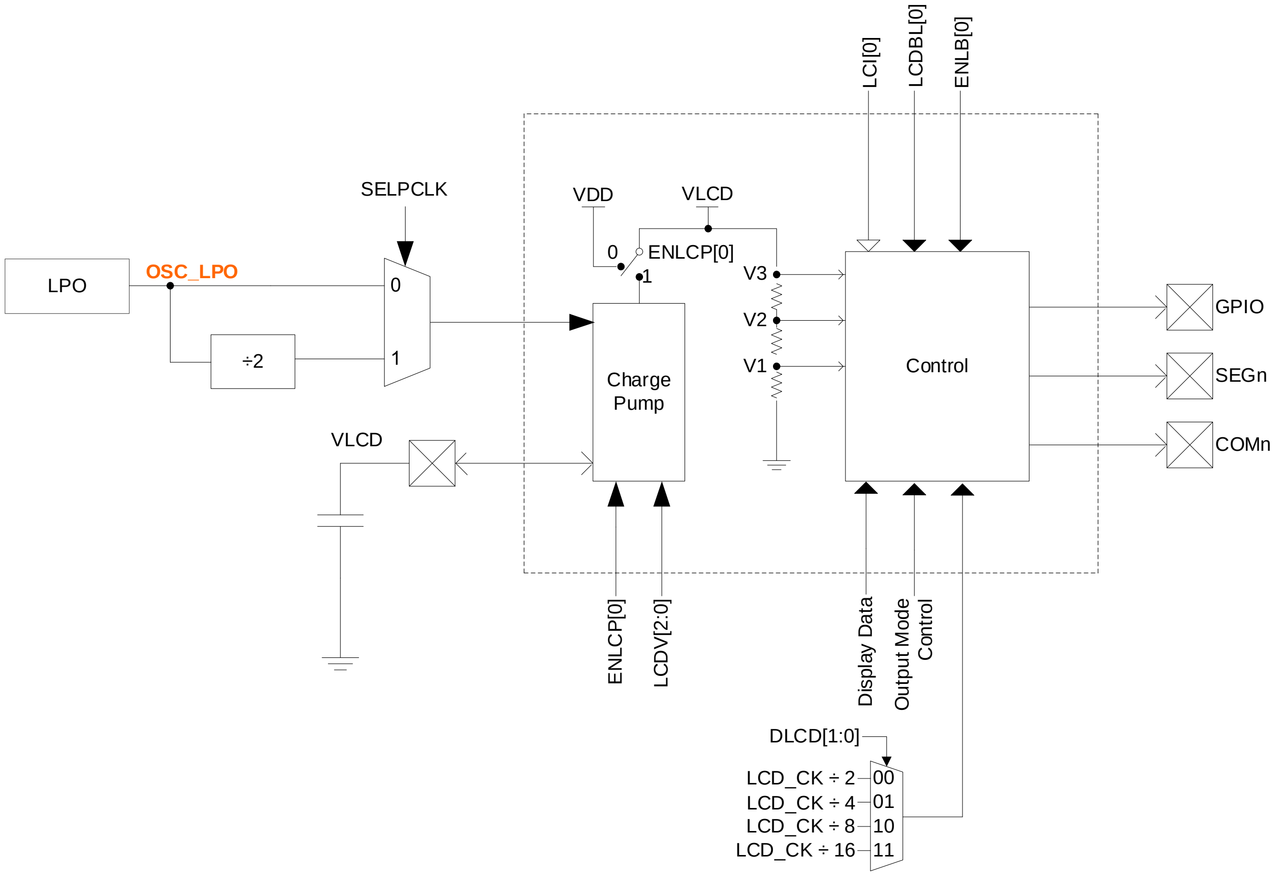



Figure 4-13 LCD block diagram

## 4.13. EUART

### EUART TRANSMIT BLOCK DIAGRAM

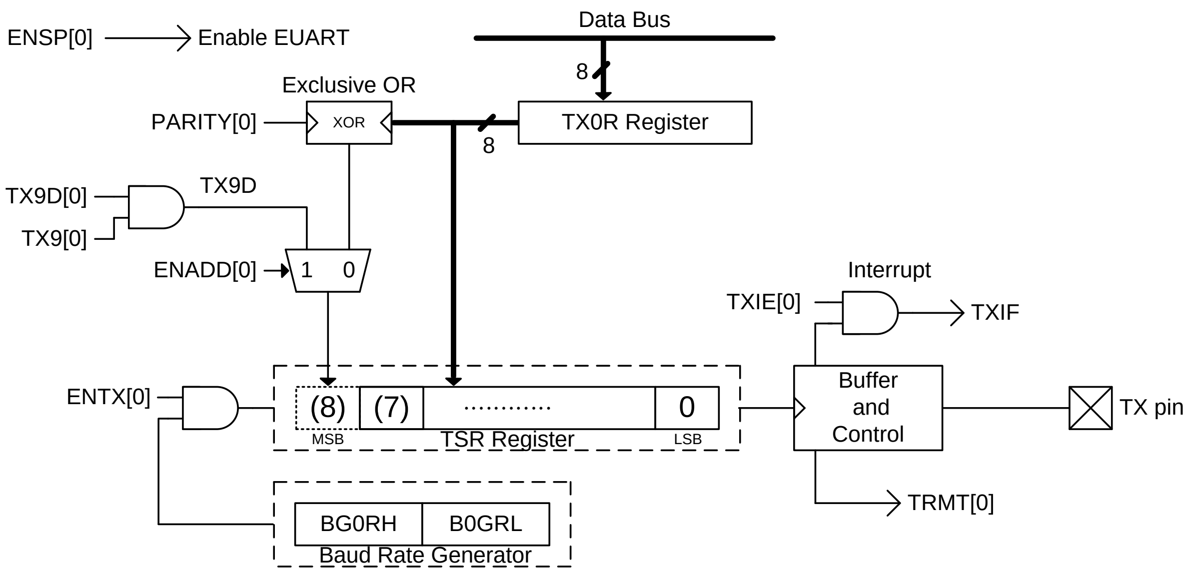
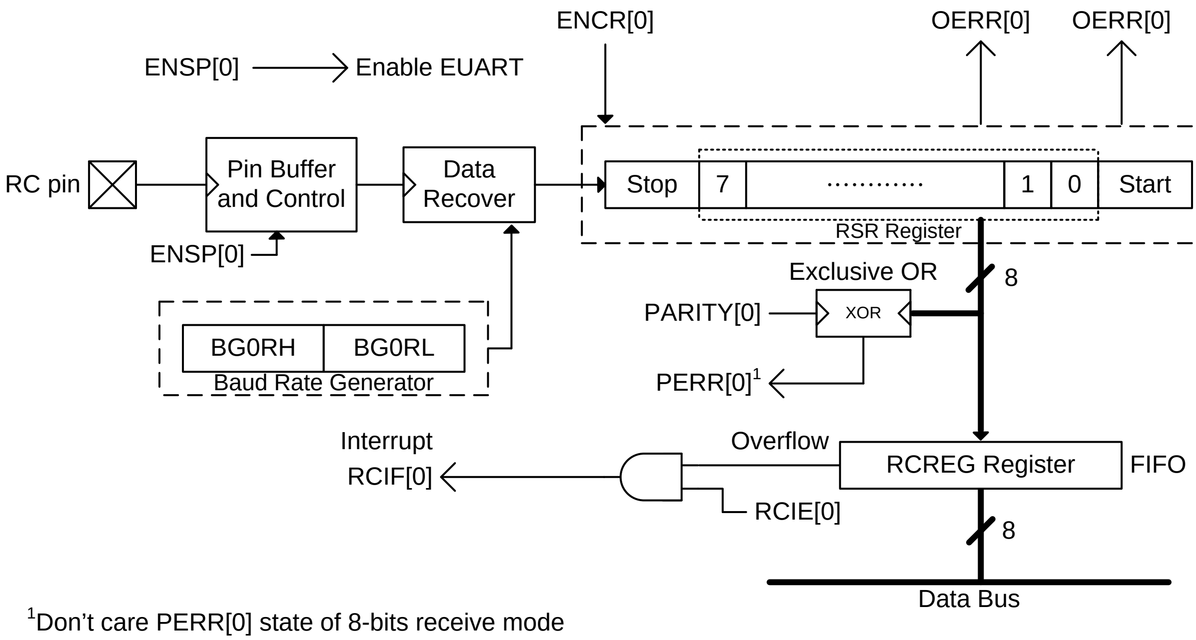



Figure 4-14 EUART transmit block diagram

### EUART 8-BITs RECEIVE BLOCK DIAGRAM




[1]Don't care PERR[0] state of 8-bits receive mode

Figure 4-15 EUART 8-bits receive block diagram

# 5. Register list

"-"no use,"*"read/write,"w"write,"r"read,"r0"onlyread 0,"r1"onlyread 1,"w0"onlywrite 0,"w1"omlywrite 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | ARST | IRST | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000h | INDF0 | Contents of FSR0 to address data memoryvalue of FSR0 not changed | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 001h | POINC0 | Contents of FSR0 to address data memoryvalue of FSR0 post-incremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 002h | PODEC0 | Contents of FSR0 to address data memoryvalue of FSR0 post-decremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 003h | PRINC0 | Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 004h | PLUSW0 | Contents of FSR0 to address data memoryvalue of FSR0 offset by W | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 005h | INDF1 | Contents of FSR1 to address data memoryvalue of FSR1 not changed | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 006h | POINC1 | Contents of FSR1 to address data memoryvalue of FSR1 post-incremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 007h | PODEC1 | Contents of FSR1 to address data memoryvalue of FSR1 post-decremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 008h | PRINC1 | Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 009h | PLUSW1 | Contents of FSR1 to address data memoryvalue of FSR1 offset by W | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 00Ah | INDF2 | Contents of FSR2 to address data memoryvalue of FSR2 not changed | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 00Bh | POINC2 | Contents of FSR2 to address data memoryvalue of FSR2 post-incremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 00Ch | PODEC2 | Contents of FSR2 to address data memoryvalue of FSR2 post-decremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 00Dh | PRINC2 | Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 00Eh | PLUSW2 | Contents of FSR2 to address data memoryvalue of FSR2 offset by W | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 00Fh | FSR0H | - | - | - | - | - | - | - | FSR0[8] | .... ...x | .... ...u | -,-,-,- -,-,-,* |
| 010h | FSR0L | Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0] | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 011h | FSR1H | - | - | - | - | - | - | - | FSR1[8] | .... ...x | .... ...u | -,-,-,- -,-,-,* |
| 012h | FSR1L | Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0] | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 016h | TOSH | - | - | - | - | TOS[11:8] | | | | .... xxxx | .... uuuu | -,-,-,- *,*,*,* |
| 017h | TOSL | Top-of-Stack Low Byte (TOS<7:0>) | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 018h | SKCN | SKFL | SKUN | SKOV | - | SKPRT[3:0] | | | | 000. 0000 | u$$. $$$$ | rw 0,rw 0,rw 0,- *,*,*,* |
| 01Ah | PCLATH | - | - | - | - | PC[11:8] | | | | .... 0000 | .... 0000 | -,-,-,- *,*,*,* |
| 01Bh | PCLATL | PC Low Byte for PC<7:0> | | | | | | | | 0000 0000 | 0000 0000 | *,*,*,* *,*,*,* |
| 01Dh | TBLPTRH | - | - | - | - | TBLPTR11:8] | | | | .... xxxx | .... uuuu | -,-,-,- *,*,*,* |
| 01Eh | TBLPTRL | Program Memory Table Pointer Low Byte (TBLPTR<7:0>) | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 01Fh | TBLDH | Program Memory Table Latch High Byte | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 020h | TBLDL | Program Memory Table Latch Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 021h | PRODH | Product Register of Multiply High Byte | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 022h | PRODL | Product Register of Multiply Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 023h | INTE0 | GIE | TA1CIE | ADIE | WDTIE | - | - | E1IE | E0IE | 0000 0000 | 0uuu uuuu | *,*,*,* *,*,*,* |
| 024h | INTE1 | TA1IE | - | TXIE | RCIE | - | - | - | - | 0000 0000 | uuuu uuuu | *,*,*,* *,*,*,* |
| 026h | INTF0 | - | TA1CIF | ADIF | WDTIF | - | - | E1IF | E0IF | .000 0000 | .uuu uuuu | *,*,*,* *,*,*,* |
| 027h | INTF1 | TA1IF | - | TXIF | RCIF | - | - | - | - | 0000 0000 | uuuu uuuu | *,*,*,* r,r,*,* |
| 029h | WREG | Working Register | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 02Ah | BSRCN | - | - | - | - | - | - | - | BSR[0] | .... ...x | .... ...u | -,-,-,- -,-,-,* |
| 02Bh | MSTAT | - | - | - | C | DC | N | OV | Z | ...x xxxx | ...u uuuu | -,-,-,* *,*,*,* |
| 02Ch | PSTAT | BOR | PD | TO | IDL | RST | SKERR | - | - | $000 $0.. | uu$u u$.. | rw0,rw0,rw0,rw0 rw0,rw0,-,- |
| 02Eh | BIECN | 1 | - | - | ENBVD | VPPHV | ENBCP | BIEWR | BIERD | 1.00 $000 | 1.00 $uuu | r1,*,-,* r,*,*,* |
| 02Fh | BIEARH | - | - | 1 | 1 | 1 | 1 | 1 | 1 | 0.xx xxxx | u.uu uuuu | *,-,*,* *,*,*,* |
| 030h | BIEARL | | | BIE Address Register as BIEAL[5:0] | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 031h | BIEDRH | BIE High Byte Data Register | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 032h | BIEDRL | BIE Low Byte Data Register | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,* *,*,*,* |
| 033h | PWRCN | ENBGR | LDOC[2:0] | | | LDOM[1:0] | | ENLDO | CSFON | 1000 0000 | uuuu uu0u | *,*,*,* *,*,*,* |
| 034h | OSCCN0 | - | OSCS[0] | DHS[1:0] | | DMS[2:0] | | | CUPS | 0000 0000 | uuuu uuuu | *,*,*,* *,*,*,* |
| 035h | OSCCN1 | CCOPT | - | DADC[1:0] | | - | - | - | LCDS | 0000 0000 | uuuu uuuu | *,*,*,* *,*,*,* |
| 036h | OSCCN2 | DLCD[1:0] | | - | - | - | HAOM[1:0] | | ENHAO | 0000 0011 | uuuu uu11 | *,*,*,* *,*,*,* |
| 037h | CSFCN0 | SKRST | HAOTR[6:0] | | | | | | | .1.. .... | .... .... | -,-,-,- -,-,-,- |
| 038h | CSFCN1 | ENSDRV | - | - | - | - | - | - | - | .... .... | uuuu uuuu | *,*,*,* *,*,*,* |
| 039h | WDTCN | ENBZ | BZS | BZ[1:0] | | ENWDT | DWDT[2:0] | | | 0000 0000 | uuuu $000 | -,*,*,* rw 1,*,*,* |
| 03Ah | AD1H | ADC1 conversion high byte data register | | | | | | | | ..00 0000 | ..uu uuuu | -,-,*,* *,*,*,* |
| 03Bh | AD1M | ADC1 conversion middle byte data register | | | | | | | | 0000 0000 | uuuu uuuu | *,*,*,* *,*,*,* |
| 03Ch | AD1L | ADC1 conversion low byte data register | | | | | | | | 0000 0000 | uuuu uuuu | *,*,*,* *,*,*,* |

Table 5-1 Data memory list (1)

“-”no use,“*”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”omly write 1
“$”for event status,“.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | ARST | IRST | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 03Dh | AD1CN0 | ENAD1 | - | | OSR[3:0] | | | | CMFR | 0000 0000 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 03Eh | AD1CN1 | INIS1 | - | VREGN | PGAGN[1:0] | | ADGN[2:0] | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 03Fh | AD1CN2 | - | - | - | - | DCSET[3:0] | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 040h | AD1CN3 | INP[3:0] | | | | INN[3:0] | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 041h | AD1CN4 | VRH[1:0] | | VRL[1:0] | | INX[1:0] | | VRIS | INIS | 0000 0000 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 042h | AD1CN5 | ENACM | - | VCMS | LDOPL | - | - | ENTPS | TPSCH | 0000 0000 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 043h | LVDCN | - | - | PWRS | LVDS[3:0] | | | | LVDO | 0000 0000 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 044h | TMA1CN | ENTMA1 | TMACL1 | TMAS1 | DTMA1[2:0] | | | - | | 0000 0000 | u0uu uuuu | *,rw 1,*,*,*,*,*,* |
| 045h | TMA1R | TMA1 counter Register | | | | | | | | 0000 0000 | uuuu uuuu | rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0 |
| 046h | TMA1C | TMA1C counter Register | | | | | | | | 0000 0000 | uuuu uuuu | rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0 |
| 047h | PT1 | - | - | PT1.5 | PT1.4 | PT1.3 | PT1.2 | PT1.1 | PT1.0 | xxxx xxxx | xxxx xxxx | *,*,*,*,*,*,*,* |
| 048h | TRISC1 | - | - | TC1.5 | TC1.4 | TC1.3 | TC1.2 | TC1.1 | TC1.0 | xx00 0000 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 049h | PT1DA | - | - | - | - | - | DA1.2 | - | - | xxxx x0xx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 04Ah | PT1PU | - | - | PU1.5 | PU1.4 | PU1.3 | PU1.2 | PU1.1 | PU1.0 | xx11 1111 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 04Bh | PT1M1 | - | - | - | - | INTEG1[1:0] | | INTEG0[1:0] | | 0000 0000 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 04Ch | PT8 | - | - | - | - | - | - | PT8.1 | PT8.0 | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 04Dh | TRISC8 | - | - | - | - | - | - | TC8.1 | TC8.0 | xxxx xx00 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 04Eh | PT8DA | - | - | - | - | - | - | DA8.1 | DA8.0 | xxxx xx00 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 04Fh | PT8PU | - | - | - | - | - | - | PU8.1 | PU8.0 | xxxx xx11 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 050h | UR0CN | ENSP | ENTX | TX9 | TX9D | PARITY | - | - | WUE | 0000 0..0 | uuuu u..u | *,*,*,*,*,-,-,* |
| 051h | UR0STA | - | RC9D | PERR | FERR | OERR | RCIDL | TRMT | ABDOVF | .000 0010 | .uuu uuuu | -,r,r,r r,r,r,rw 0 |
| 052h | BA0CN | - | - | - | - | ENCR | RC9 | ENADD | ENABD | .... 0000 | .... uuuu | -,-,-,- *,*,*,* |
| 053h | BG0RH | - | - | - | Baud Rate Generator Register High Byte | | | | | ...x xxxx | ...u uuuu | -,-,-,*,*,*,*,* |
| 054h | BG0RL | Baud Rate Generator Register Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 055h | TX0R | UART Transmit Register | | | | | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 056h | RC0REG | UART Receive Register | | | | | | | | xxxx xxxx | uuuu uuuu | r,r,r,r r,r,r,r |
| 057h | LCDCN1 | ENLCP | LCDV[2:0] | | | ENLB | SELPCLK | - | - | 0000 0000 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 058h | LCDCN2 | | - | - | - | - | - | LCDBL | LCI | .... ..00 | .... ..uu | *,*,*,*,*,*,*,* |
| 059h | LCDCN3 | SCM3[1:0] | | SCM2[1:0] | | SCM1[1:0] | | SCM0[1:0] | | 1111 1111 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 05Ah | LCDCN4 | - | - | - | - | - | - | SSG15 | SSG14 | 0000 0000 | uuuu uuuu | *,*,*,*,*,*,*,* |
| 05Bh | LCD0 | LCD SEG3[4:7] data | | | | LCD SEG2[3:0] data | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 05Ch | LCD1 | LCD SEG5[4:7] data | | | | LCD SEG4[3:0] data | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 05Dh | LCD2 | LCD SEG7[4:7] data | | | | LCD SEG6[3:0] data | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 05Eh | LCD3 | LCD SEG9[4:7] data | | | | LCD SEG8[3:0] data | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 05Fh | LCD4 | LCD SEG11[4:7] data | | | | LCD SEG10[3:0] data | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 060h | LCD5 | LCD SEG13[4:7] data | | | | LCD SEG12[3:0] data | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 061h | LCD6 | LCD SEG15[4:7] data | | | | LCD SEG14[3:0] data | | | | xxxx xxxx | uuuu uuuu | *,*,*,*,*,*,*,* |
| 080h ~ 17Fh | | SRAM as 256Byte | | | | | | | | uuuu uuuu | uuuu uuuu | *,*,*,*,*,*,*,* |

Table 5-2 Data memory list (2)

# 6. Electrical Characteristics

**Absolute Maximum Ratings :**

**Absolute maximum ratings over operating free-air temperature (unless otherwise noted)**

**Voltage applied at VDD to VSS . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.2 V to 6.0 V**

**Voltage applied to any pin . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.2 V to VDD + 0.3 V**

**Voltage applied to VLCD/VPP pin . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −0.2 V to 8.0 V**

**Diode current at any device terminal . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±2 mA**

**Storage temperature, Tstg: (unprogrammed device) . . . . . . . . . . . . . . . . . . . . . .. . . . . . . . . −55℃ to 125℃**

**(programmed device) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −40℃ to 85℃**

**Total power dissipation. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.5w**

**Maximum output current sink by any I/O pin. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .20mA**

## 6.1. Recommended operating conditions

A = -40℃ ~ 85℃,unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD | Supply Voltage | All digital peripherals and CPU | 2.0 | | 5.5 | V |
| VDDA | Supply Voltage | Analog peripherals | 2.4 | | 5.0 | |
| VSS | Supply Voltage | | 0 | | 0 | |

## 6.2. Internal RC Oscillator

TA = 25℃,VDD = 3.0V,unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| HAO | High Speed Oscillator frequency | ENHAO[0]=1, HAOM[1:0]=00 | -20% | 1.843 | +20% | MHz |
| | | ENHAO[0]=1, HAOM[1:0]=01 | -20% | 3.686 | +20% | MHz |
| | | ENHAO[0]=1, HAOM[1:0]=11 | -20% | 7.834 | +20% | MHz |
| | | After Frequency Trim by Writer | -2% | | +2% | MHz |
| LPO | Low Power Oscillator frequency | VDD supply voltage be enable LPO | -20% | 14.5 | +20% | KHz |

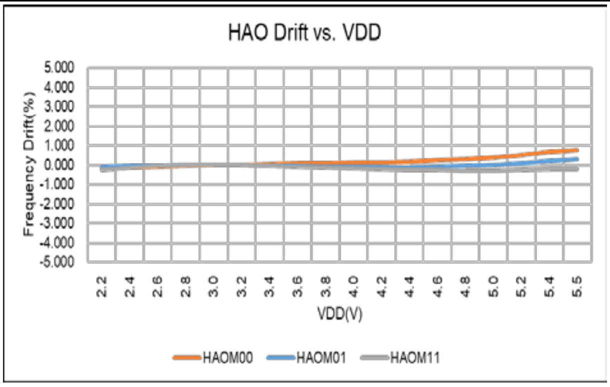



Figure 6.2-1 HAO vs. VDD

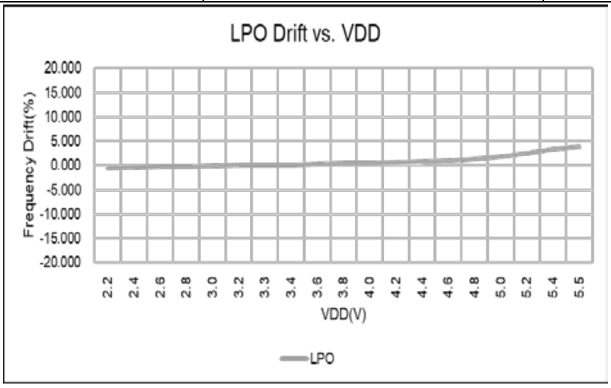



Figure 6.2-2 LPO vs. VDD

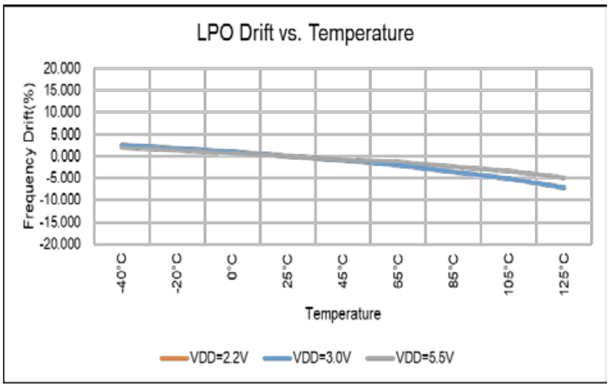



Figure 6.2-3 LPO vs. Temperature

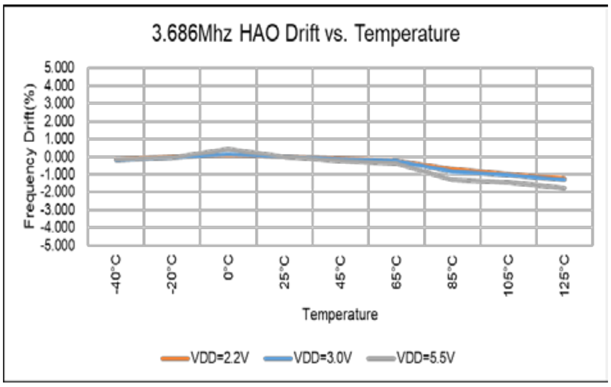



Figure 6.2-4 HAO(3.686MHz) vs. Temperature

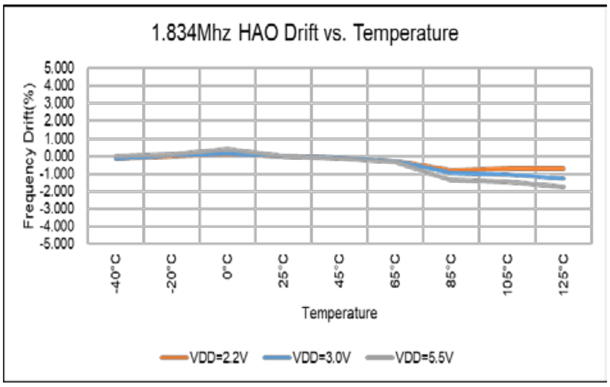



Figure 6.2-4 HAO(1.843MHz) vs. Temperature

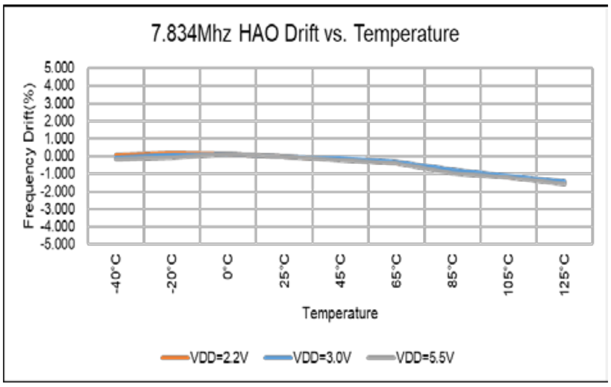



Figure 6.2-6 HAO(7.834MHz) vs. Temperature

## 6.3. Supply current into VDD excluding peripherals current

TA = 25℃,VDD = 3.0V,OSC_LPO = 14.5KHz, , unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit |
|---|---|---|---|---|---|---|
| $I_{AM2}$ | Active mode 2 | OSC_CY = off, OSC_HAO =3.686MHz, CPU_CK = 3.686MHz | | 320 | 650 | uA |
| $I_{AM5}$ | Active mode 5 | OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz/2 | | 250 | 500 | uA |
| $I_{LP1}$ | Low Power 1 | OSC_CY = off, OSC_HAO=off, CPU_CK = LPO | | 2 | 5 | uA |
| $I_{LP2}$ | Low Power 2 | OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state | | 1.1 | 2.5 | uA |
| $I_{LP3}$ | Low Power 3 | OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state | | 0.4 | 1.0 | uA |
| OSC_HAO：Internal High Accuracy Oscillator frequency.<br>CPU_CK：CPU core work frequency. | | | | | | |

TA = 25℃,VDD = 5.5V,OSC_LPO = 14.5KHz, , unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit |
|---|---|---|---|---|---|---|
| $I_{AM2}$ | Active mode 2 | OSC_CY = off, OSC_HAO =3.686MHz, CPU_CK = 3.686MHz | | 720 | 1200 | uA |
| $I_{AM5}$ | Active mode 5 | OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz/2 | | 600 | 900 | uA |
| $I_{LP1}$ | Low Power 1 | OSC_CY = off, OSC_HAO=off, CPU_CK = LPO | | 4 | 10 | uA |
| $I_{LP2}$ | Low Power 2 | OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state | | 2.5 | 5 | uA |
| $I_{LP3}$ | Low Power 3 | OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state | | 0.4 | 2 | uA |
| OSC_HAO：Internal High Accuracy Oscillator frequency. | | | | | | |

CPU_CK：CPU core work frequency.

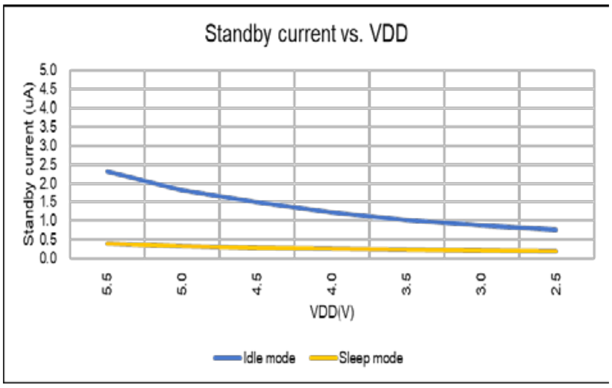



Figure 6.3-1 Standby current vs. VDD

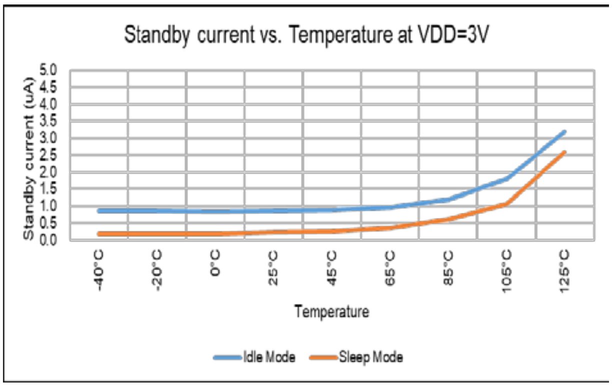



Figure 6.3-2 Standby current vs. Temperature VDD=3V

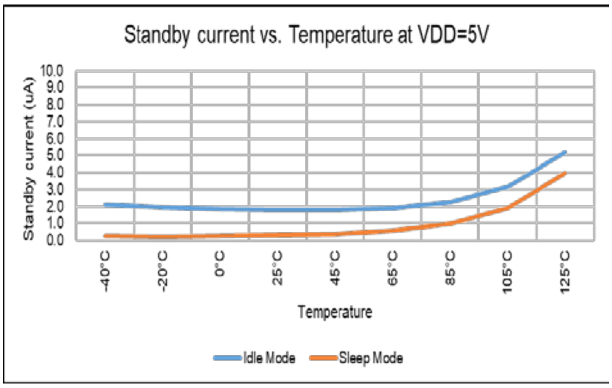



Figure 6.3-3 Standby current vs. Temperature at VDD=5V

## 6.4. Port 1 & 8

TA = 25℃,VDD = 3.0V,unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input voltage and Schmitt trigger and leakage current and timing | | | | | | |
| $V_{IH}$ | High-Level input voltage | | | | 0.7*VDD | V |
| $V_{IL}$ | Low-Level input voltage | | 0.3*VDD | | | V |
| $V_{hys}$ | Input Voltage hysteresis($V_{IH}$ - $V_{IL}$ ) | | | 0.3*VDD | | V |
| $I_{LKG}$ | Leakage Current | | | | 0.1 | uA |
| $R_{PU}$ | Port pull high resistance(PT1、PT2) | | | 60 | | kΩ |
| | Port pull high resistance(PT8) | | | 60 | | kΩ |
| Output voltage and current and frequency | | | | | | |
| $V_{OH}$ | High-level output voltage | VDD<4V, $I_{OH}$=3mA, | VDD -0.3 | | | V |
| | | VDD>=4V, $I_{OH}$=5mA, | VDD -0.3 | | | V |
| $V_{OL}$ | Low-level output voltage | VDD<4V, $I_{OL}$=-3mA | | | VSS +0.3 | V |
| | | VDD>=4V, $I_{OL}$=-5mA | | | VSS +0.3 | V |

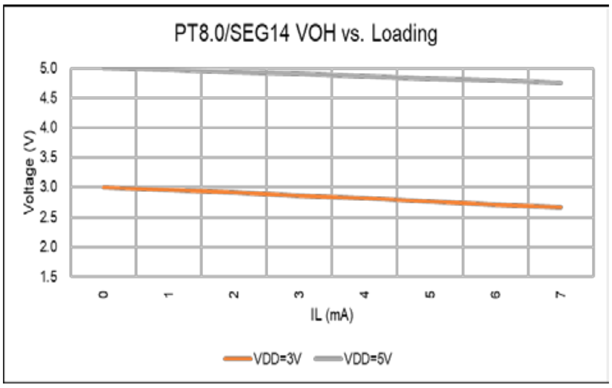



Figure 6.4-1 PT8.0/SEG14 VOH vs. Loading

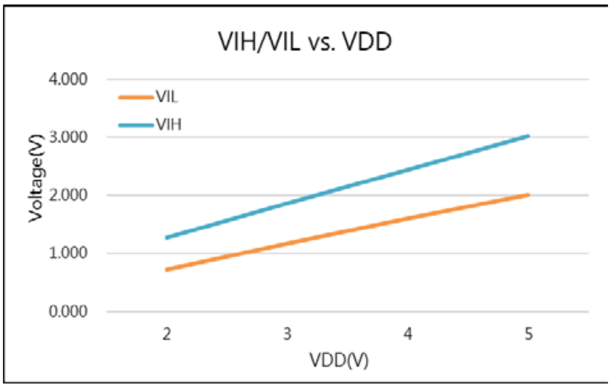



Figure 6.4-2 $V_{IH}/V_{IL}$ vs. VDD

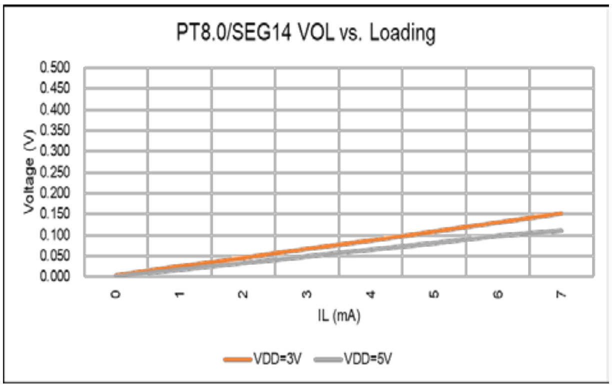



Figure 6.4-3 PT8.0/SEG14 VOL vs. Loading

## 6.5. Port1.4~Port1.5

TA = 25℃,VDD = 3.0V,unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input voltage and Schmitt trigger and leakage current and timing | | | | | | |
| $V_{IH}$ | High-Level input voltage | | | | 0.7*VDD | V |
| $V_{IL}$ | Low-Level input voltage | | 0.3*VDD | | | V |
| $V_{hys}$ | Input Voltage hysteresis($V_{IH}$ - $V_{IL}$ ) | | | 0.3*VDD | | V |
| $I_{LKG}$ | Leakage Current | | | | 0.1 | uA |
| $R_{PU}$ | Port pull high resistance | | | 60 | | kΩ |
| Output voltage and current and frequency | | | | | | |
| $V_{OH}$ | High-level output voltage | VDD=3V, $I_{OH}$=10mA, | VDD -0.4 | | | V |
| | | VDD=5V, $I_{OH}$=15mA, | VDD -0.4 | | | |
| $V_{OL}$ | Low-level output voltage | VDD=3V, $I_{OL}$=-10mA | | | VSS +0.4 | |
| | | VDD=5V, $I_{OL}$=-15mA | | | VSS +0.4 | |

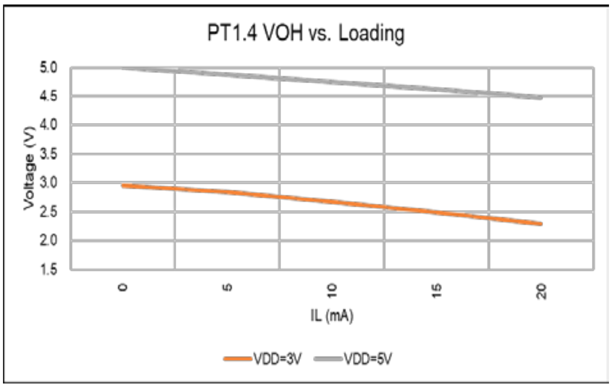



Figure 6.5-1 PT1.4 VOH vs. Loading

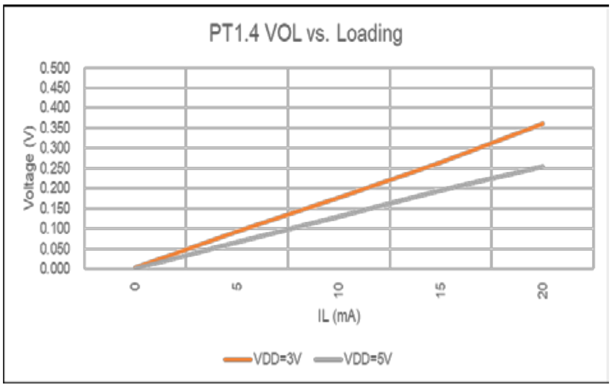



Figure 6.5-2 PT1.4 VOL vs. Loading

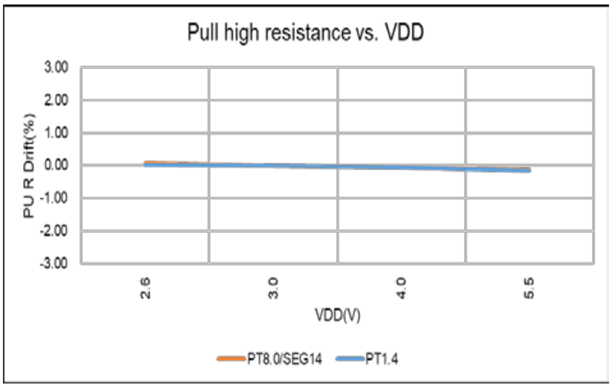



Figure 6.5-3 Pull high resistance vs. VDD

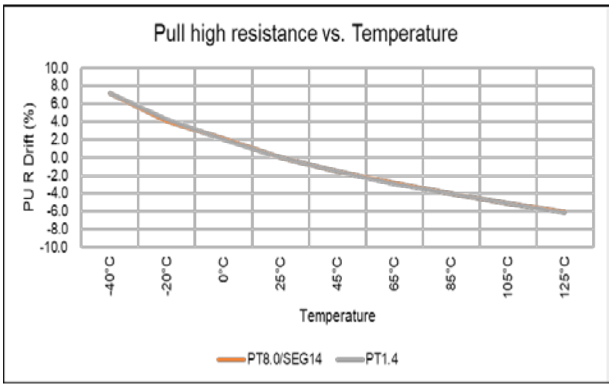



Figure 6.5-4 Pull high resistance vs. Temperature

## 6.6. Reset(Brownout, Low Voltage Detect)

TA = 25℃,VDD = 3.0V,unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit |
|---|---|---|---|---|---|---|
| BOR1 | Pulse length needed to accepted reset internally, $t_{d\text{-}LVR1}$ | | 2 | | | uS |
| | VDD Start Voltage to accepted reset internally (L➔H),$V_{HYS1}$ | | 1.6 | 1.8 | 2.0 | V |
| | BOR1 current, $I_{BOR1}$ | | | 0.4 | | uA |
| | Temperature Drift | | | 5 | | % |
| LVD | Operation current, $I_{LVD}$ | | | 10 | | uA |
| | External input voltage to compare reference voltage | | 1.15 | 1.2 | 1.25 | V |
| | Compare reference voltage temperature drift | TA = -40℃ ~ 85 ℃ | | 50 | | ppm/℃ |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1110b | | -0.1 | 4.0 | +0.1 | V |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1101b | | | 3.6 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1100b | | | 3.3 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1011b | | | 3.0 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1010b | | | 2.9 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1001b | | | 2.8 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1000b | | | 2.7 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0111b | | | 2.6 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0110b | | | 2.5 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0101b | | | 2.4 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0100b | | | 2.3 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0011b | | | 2.2 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0010b | | | 2.1 | | |
| | Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0001b | | | 2.0 | | |
| BOR1：Brownout Reset 1<br>LVD：Low Voltage Detect | | | | | | |

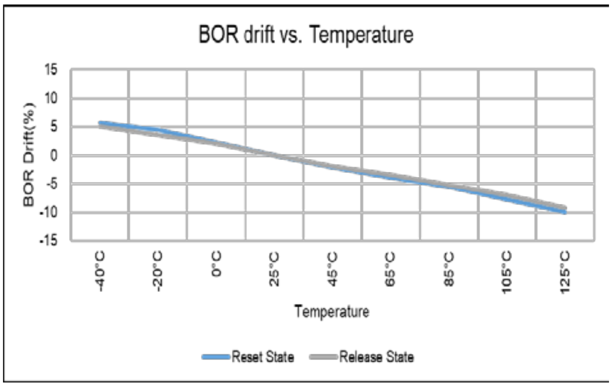



Figure 6.6-1 BOR vs. Temperature

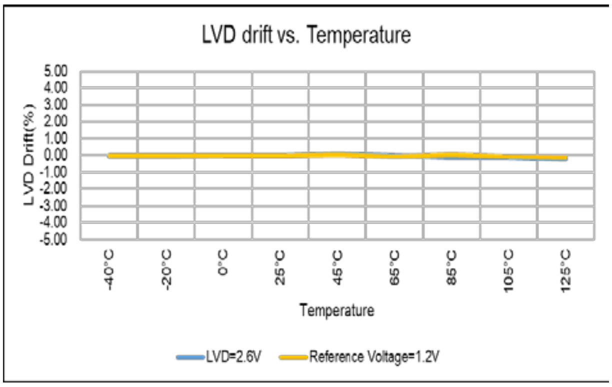



Figure 6.6-2 LVD drift vs. Temperature

## 6.7. Power System

TA = 25℃,VDD = 3.0V,unless otherwise noted

| Sym. | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VDDA | VDDA operation current, $I_{VDDA}$ | $I_L$ = 0mA | LDOC[2:0]=000b | | 20 | | uA |
| | Select VDDA output voltage | $I_L$ = 0.1mA, VDD≧VDDA+0.25V | LDOC [2:0]=000b | -5% | 2.4 | +5% | V |
| | | | LDOC [2:0]=100b | | 3.6 | | V |
| | Dropout voltage | $I_L$ = 10mA | LDOC [2:0]=000b | | 500 | | mV |
| | Temperature drift | LDOC [2:0]=000b<br>$I_L$ = 0.1mA | TA=-40℃~85℃ | | 50 | | PPM/℃ |
| | VDD Voltage drift | LDOC [2:0]=000b | VDD=2.2V~5.5V | | ±0.2 | | %/V |
| VDDA/2 | operation current, $I_{ACM}$ | ENADC[0]=1b, | ENACM [0]=1b | | 50 | | uA |
| | Internal Analog Common Mode Voltage ,$V_{ACM}$=VDDA/2 | | $I_L$ = 0uA | | VDDA/2 | | V |
| | Temperature drift | ENADC[0]=1b, | TA=-40℃~85℃,<br>ENACM [0]=1b | | 50 | | PPM/℃ |
| V12 | operation current, $I_{V12}$ | ENADC[0]=1b, | ENV12 [0]=1b | | 50 | | uA |
| | Internal Analog Common Mode Voltage ,$V_{ACM}$=V12 | | $I_L$ = 0uA | 1.1 | 1.2 | 1.3 | V |

| | | | | | |
|---|---|---|---|---|---|
| | Temperature drift | ENADC[0]=1b, | TA=-40℃~85℃,<br>ENV12 [0]=1b | 50 | PPM/℃ |
| VDDA：Adjust Voltage Regulator,<br>ACM：Internal Analog Common Mode Voltage VDDA/2 (No voltage output) | | | | | |

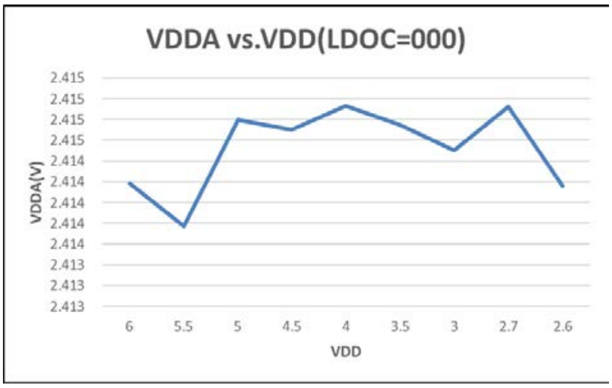



Figure 6.7-1 VDDA Drift vs. VDD

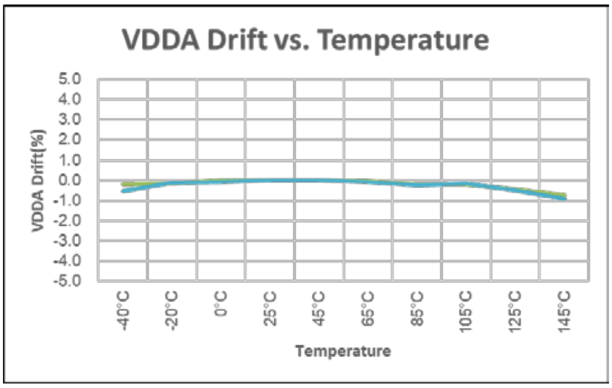



Figure 6.7-2 VDDA Drift vs. Temperature

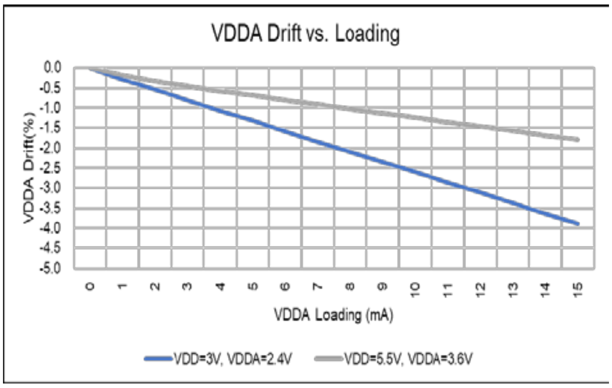



Figure 6.7-3 VDDA Drift vs. Loading

## 6.8. LCD

TA = 25℃,VDD = 3.3V, CVLCD =4.7uF,unless otherwise noted.

| Sym. | Parameter | Test Conditions | | Min. | Typ. | Max. | unit |
|---|---|---|---|---|---|---|---|
| $I_{LCD}$ | Operation supply current with output buffer.(all segment turn on, No load) | ENLCP[0]=1 | VDD = 3.0V | | 5 | | uA |
| VLCD | Supply Voltage at VLCD pin | ENLCP [0]=0 | | 2.4 | | 5 | V |
| | Embedded Charge Pump output voltage at VLCD pin | VDD = 3.3V,<br>ENLCP [0]=1<br>CVLCD<br>=4.7uF | LCDV[2:0]=111b | -10% | 2.45 | +10% | V |
| | | | LCDV[2:0]=110b | -10% | 2.70 | +10% | |
| | | | LCDV[2:0]=101b | -10% | 2.85 | +10% | |
| | | | LCDV[2:0]=100b | -10% | 3.10 | +10% | |
| | | | LCDV[2:0]=011b | -10% | 3.30 | +10% | |
| | | | LCDV[2:0]=010b | -10% | 4.10 | +10% | |
| | | | LCDV[2:0]=001b | -10% | 4.55 | +10% | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | (VDD>2.4V mode) | | | | |
| | | | LCDV[2:0]=000b (VDD>2.75V) | -10% | 5.1 | +10% | |
| | VDD Voltage drift | ENLCP [0]=1, CVLCD =4.7uF, LCDV[2:0]>010b,VDD=2.2V~ 5.5V; LCDV[2:0]=001b,VDD>2.4V; LCDV[2:0]=000b,VDD>2.75V; | | | 4 | | %/V |
| $Z_{LCD}$ | Output impedance with LCD buffer | $f_{LCD}$ =128Hz,VLCD=3.05V | | | 10 | | kΩ |

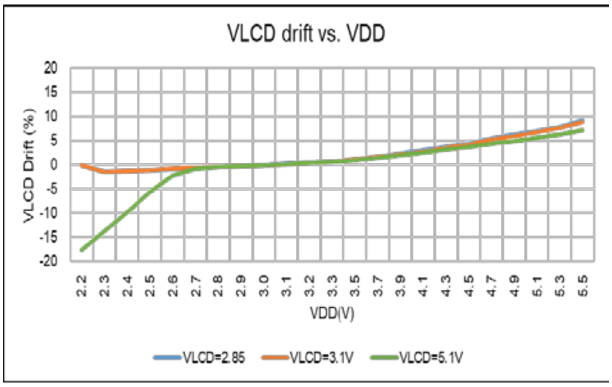



Figure6.8-1 VLCD drift vs. VDD

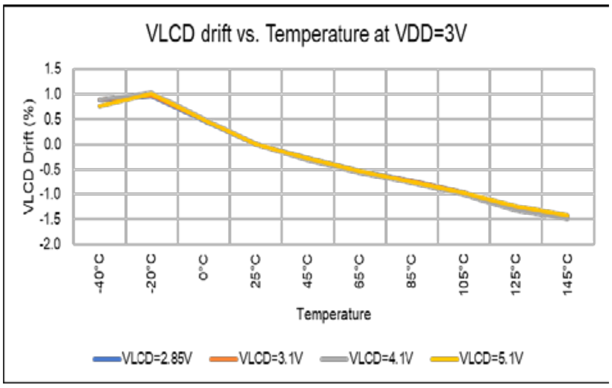



Figure6.8-2 VLCD drift vs. Temperature at VDD=3V

## 6.9. ΣΔADC, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

| Sym. | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{SD18}$ | Supply Voltage at VDDA | ENLDO[0]=0 | | 2.4 | | 5.5 | V |
| $f_{SD18}$ | Modulator sample frequency, ADC_CK | | | 230 | 921 | | KHz |
| | Over Sample Ratio, OSR | | | 64 | | 65536 | |
| $I_{SD18}$ | Operation supply current without PGA | ENAD1 [0]=1 | GAIN =16, ADC_CK=921KHz | | 300 | | uA |

### 6.9.1. PGA, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

| Sym. | Parameter | Test Conditions | | Min | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{PGA}$ | Supply Voltage at VDDA | ENLDO [0]=0 | | 2.4 | | 5.5 | V |
| $I_{PGA}$ | Operation supply current | PGAGN[1:0]=<11> | | | 450 | | uA |
| $G_{PGA}$ | Gain temperature drift | TA = -40℃~ 85℃ | GAIN=128 | | 14 | | ppm/℃ |

### 6.9.2. ΣΔADC,performance

TA = 25℃,VDD = 3.6V, VDDA=2.4V,$V_{VR}$= AI2(short to VDDA)/2

GAIN=16 with PGA=8,$f_{SD18}$=921KHz,unless otherwise noted

| Sym. | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| INL | Integral Nonlinearity(INL) | VDDA=2.4V,VVR= AI2/2, ΔSI=±450mV | | | ±0.003 | ±0.01 | %FSR |
| | No Missing Codes3 | ADC_CK=921KHz,OSR[3:0]=0000b | | 23 | | | Bits |
| $G_{SD18}$ | Temperature drift Gain x16 | TA = -40℃~ 85℃ | | | 10 | | ppm/℃ |
| $E_{OS}$ | Offset error of Full Scale Rang input voltage range with Chopper without PGA | ΔAI=0V<br>ΔVR=1.2V<br>DCSET[3:0]=<0000><br>*ΔAI is external short | Gain=2 | | | 1 | %FSR |
| | Offset temperature drift with chopper without PGA | | GAIN=1 | | 2 | | uV/℃ |
| | | | GAIN=2 | | 1 | | uV/℃ |
| | | | GAIN=4 | | 0.5 | | uV/℃ |
| | | | GAIN=16 | | 0.15 | | uV/℃ |
| | Offset temperature drift with chopper | | GAIN=128 | | 0.02 | | uV/℃ |
| $CM_{SD18}$ | Common-mode rejection | $V_{CM}$=0.7V to 1.7V, $V_{VR}$= 1.0V,without PGA | $V_{SI}$=0V, GAIN=1 | | 90 | | dB |
| | | | $V_{SI}$=0V, GAIN=16 | | 75 | | dB |
| PSRR | DC power supply rejection | VDDA=3.0V<br>$\Delta_{VDDA}$=±100mV,<br>$V_{VR}$=1.0V,<br>$V_{SI}$=1.2V,$V_{SI}$-=1.2V, | GAIN=1 PGA=off | | 75 | | dB |
| | | | GAIN=16 PGA=8 | | | | dB |

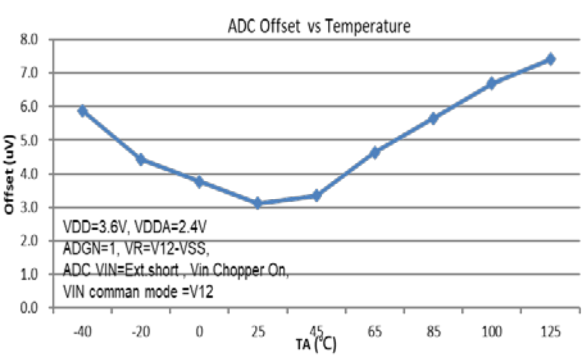



Figure 6.9-1 ADC Offset drift with Temperature (Gain=1)

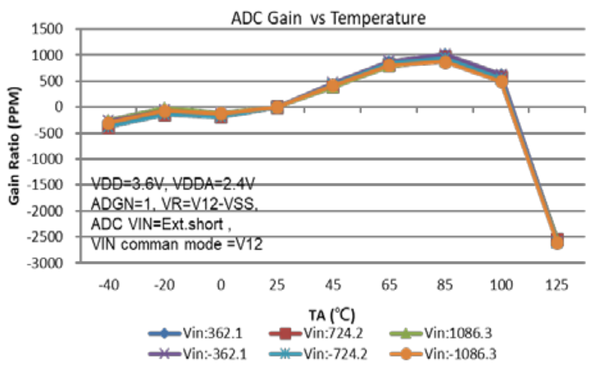



Figure 6.9-2 ADC Gain drift with Temperature (Gain=1)

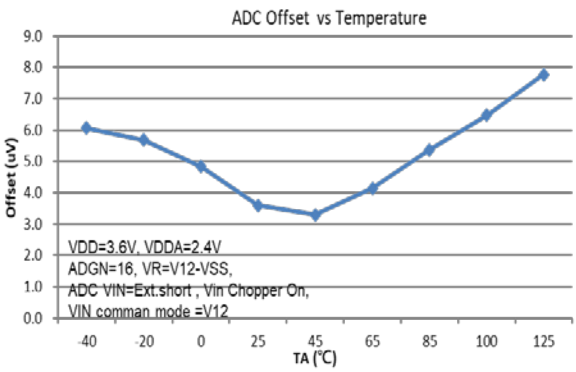



Figure 6.9-3 ADC Offset drift with Temperature (Gain=16)

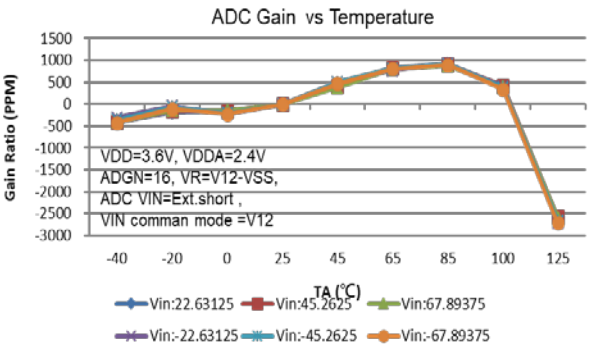



Figure 6.9-4 ADC Gain drift with Temperature (Gain=16)

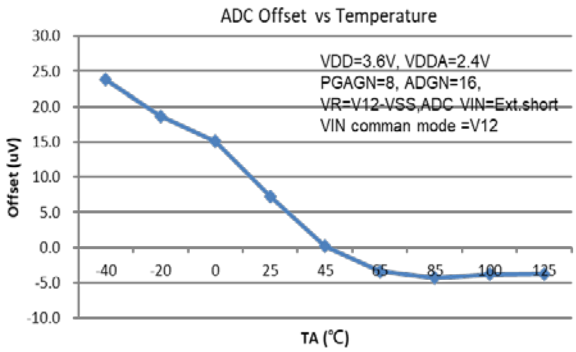



Figure 6.9-5 Offset drift with Temperature (Gain=128)

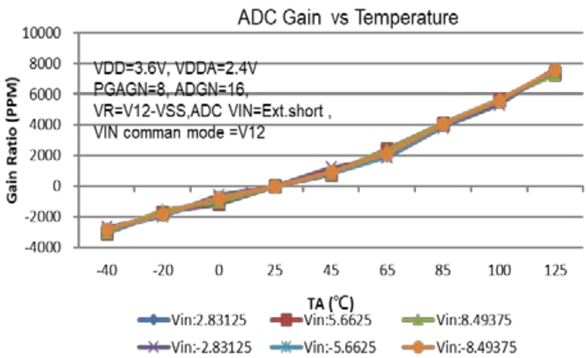



Figure 6.9-6 ADC Gain drift with Temperature (Gain=128)

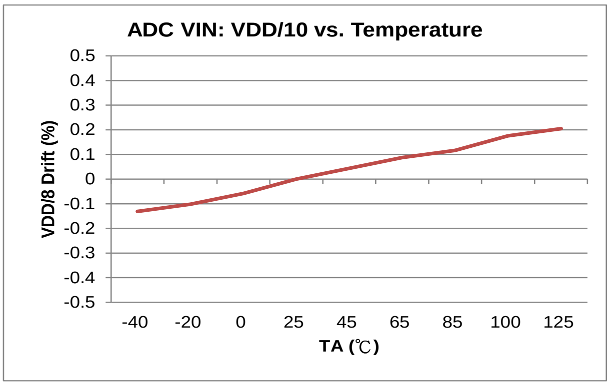



Figure 6.9-7 VDD/10 drift with Temperature

### 6.9.3. ΣΔADC Noise Performance

Provide important input noise specifications for the ΣΔ ADC. Table 6.9-1 below shows the typical noise specification table and the relationship between Gain, Output rate, and differential maximum input voltage., sampling 1024 datas.

| *ENOB(RMS) with OSR/GAIN at A/D Clock=921KHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V* | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Max. Vin(mV) =0.9VREF(1) | OSR | | | | | 64 | 128 | 256 | 512 | 1024 | 2048 | 4096 | 8196 | 16384 | 32768 | 65536 |
| | Output rate(Hz) | | | | | 15625 | 7813 | 3906 | 1953 | 977 | 488 | 244 | 122 | 61 | 28 | 14 |
| | Gain | = | PGAGN | x | ADGN | | | | | | | | | | | |
| ±1080 | 1 | = | off | x | 1 | 14.05 | 15.24 | 15.8 | 16.24 | 16.65 | 17.03 | 17.52 | 18.09 | 18.56 | 18.98 | 19.52 |
| ±270 | 4 | = | off | x | 4 | 14.09 | 15.14 | 15.59 | 16.02 | 16.6 | 16.87 | 17.31 | 17.82 | 18.29 | 18.74 | 19.1 |
| ±68 | 16 | = | off | x | 16 | 11.95 | 14.88 | 15.39 | 15.94 | 16.47 | 16.81 | 17.21 | 17.73 | 18.13 | 18.6 | 19.02 |
| ±135 | 8 | = | 8 | x | 1 | 13.67 | 15.14 | 15.6 | 16.04 | 16.47 | 16.88 | 17.35 | 17.87 | 18.42 | 18.87 | 19.34 |
| ±8.5 | 128 | = | 8 | x | 16 | 11.61 | 12.63 | 13.13 | 13.55 | 14.11 | 14.47 | 14.92 | 15.36 | 15.96 | 16.46 | 16.92 |

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

| *RMS(uV) with OSR/GAIN at A/D Clock=921KHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V* | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Max. Vin(mV) =0.9VREF(1) | OSR | | | | | 64 | 128 | 256 | 512 | 1024 | 2048 | 4096 | 8196 | 16384 | 32768 | 65536 |
| | Output rate(Hz) | | | | | 15625 | 7813 | 3906 | 1953 | 977 | 488 | 244 | 122 | 61 | 28 | 14 |
| | Gain | = | PGAGN | x | ADGN | | | | | | | | | | | |
| ±1080 | 1 | = | off | x | 1 | 142.74 | 62.37 | 42.43 | 31.17 | 23.40 | 18.04 | 12.83 | 8.65 | 6.22 | 4.65 | 3.20 |
| ±270 | 4 | = | off | x | 4 | 34.62 | 16.74 | 12.22 | 9.06 | 6.06 | 5.03 | 3.71 | 2.61 | 1.88 | 1.38 | 1.08 |
| ±68 | 16 | = | off | x | 16 | 38.02 | 4.99 | 3.52 | 2.41 | 1.66 | 1.32 | 0.99 | 0.69 | 0.53 | 0.38 | 0.28 |
| ±135 | 8 | = | 8 | x | 1 | 23.17 | 8.36 | 6.06 | 4.47 | 3.33 | 2.50 | 1.80 | 1.26 | 0.86 | 0.63 | 0.46 |
| ±8.5 | 128 | = | 8 | x | 16 | 6.05 | 2.97 | 2.11 | 1.58 | 1.07 | 0.83 | 0.61 | 0.45 | 0.30 | 0.21 | 0.15 |

Table 6.9-1(a) ΣΔADC ENOB and RMS Noise Table at VDDA=2.4V

| *ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V at High Accuracy Mode* | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Max. Vin(mV) =0.9VREF(1) | OSR | | | | | 64 | 128 | 256 | 512 | 1024 | 2048 | 4096 | 8196 | 16384 | 32768 | 65536 |
| | Output rate(Hz) | | | | | 7813 | 3906 | 1953 | 977 | 488 | 244 | 122 | 61 | 31 | 14 | 7 |
| | Gain | = | PGAGN | x | ADGN | | | | | | | | | | | |
| ±1080 | 1 | = | off | x | 1 | 14.95 | 15.76 | 16.25 | 16.8 | 17.13 | 17.51 | 17.99 | 18.51 | 19 | 19.61 | 20.04 |
| ±270 | 4 | = | off | x | 4 | 14.94 | 15.64 | 16.07 | 16.52 | 17.02 | 17.34 | 17.83 | 18.43 | 18.92 | 19.39 | 19.82 |
| ±68 | 16 | = | off | x | 16 | 14.75 | 15.44 | 15.89 | 16.46 | 16.96 | 17.32 | 17.79 | 18.3 | 18.81 | 19.22 | 19.62 |
| ±135 | 8 | = | 8 | x | 1 | 14.94 | 15.59 | 16.1 | 16.59 | 17.06 | 17.37 | 17.89 | 18.31 | 18.92 | 19.37 | 19.81 |
| ±8.5 | 128 | = | 8 | x | 16 | 12.57 | 12.89 | 13.53 | 13.94 | 14.48 | 14.68 | 15.25 | 15.85 | 16.38 | 16.98 | 17.49 |

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

| *RMS Noise(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V at High Accuracy Mode* | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Max. Vin(mV) =0.9VREF(1) | OSR | | | | | 64 | 128 | 256 | 512 | 1024 | 2048 | 4096 | 8196 | 16384 | 32768 | 65536 |
| | Output rate(Hz) | | | | | 7813 | 3906 | 1953 | 977 | 488 | 244 | 122 | 61 | 31 | 14 | 7 |
| | Gain | = | PGAGN | x | ADGN | | | | | | | | | | | |
| ±1080 | 1 | = | off | x | 1 | 76.21 | 43.47 | 30.92 | 21.16 | 16.80 | 12.95 | 9.29 | 6.45 | 4.61 | 3.01 | 2.24 |
| ±270 | 4 | = | off | x | 4 | 19.21 | 11.84 | 8.76 | 6.40 | 4.53 | 3.63 | 2.59 | 1.71 | 1.22 | 0.88 | 0.65 |
| ±68 | 16 | = | off | x | 16 | 5.46 | 3.39 | 2.48 | 1.68 | 1.18 | 0.92 | 0.67 | 0.47 | 0.33 | 0.25 | 0.19 |
| ±135 | 8 | = | 8 | x | 1 | 9.62 | 6.11 | 4.30 | 3.06 | 2.20 | 1.78 | 1.24 | 0.93 | 0.61 | 0.44 | 0.33 |
| ±8.5 | 128 | = | 8 | x | 16 | 3.11 | 2.49 | 1.59 | 1.20 | 0.83 | 0.72 | 0.48 | 0.32 | 0.22 | 0.15 | 0.10 |

Table 6.9-1(b) High Accuracy Mode, ΣΔADC ENOB and RMS Noise Table at VDDA=2.4V

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\mathrm{ENOB(RMS)} = \ln\left(\frac{\mathrm{FSR}}{\mathrm{RMS\ Noise}}\right) \Big/ \ln(2)$$

$$\mathrm{RMS\ Noise} = \left(2 \times \mathrm{VREF} \times \sqrt{\sum_{k=1}^{1024}\left(\mathrm{ADO}[k] - \mathrm{Average}\right)^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full-Scale Range)} = 2 \times \mathrm{VREF/Gain}.$$

$$\mathrm{Average} = \frac{\sum_{k=1}^{1024}\left(\mathrm{ADO}[k]\right)}{1024}$$

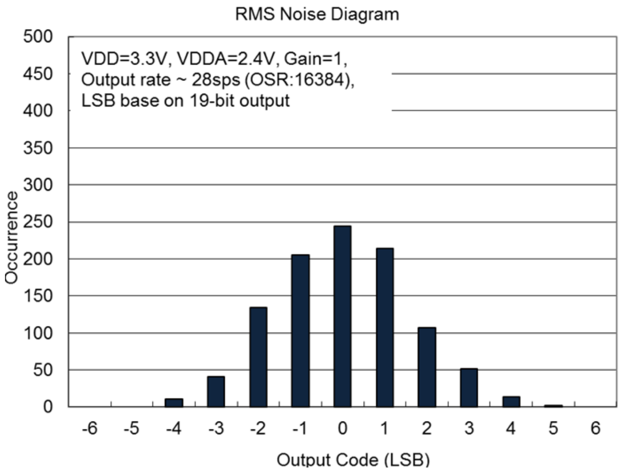



Figure 6.9-8 RMS Noise Diagram

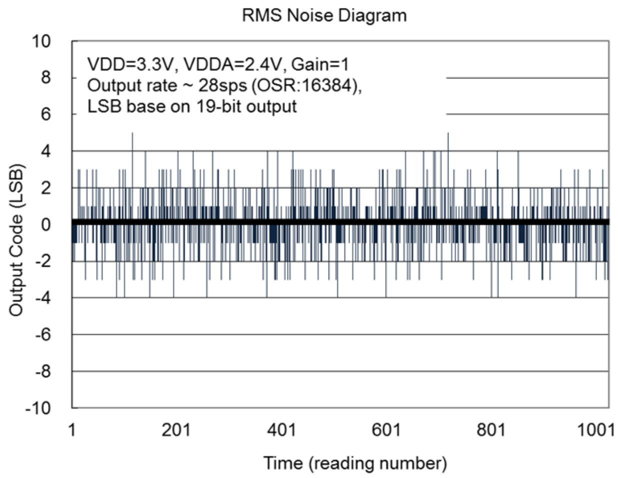



Figure 6.9-9 Output Code Diagram

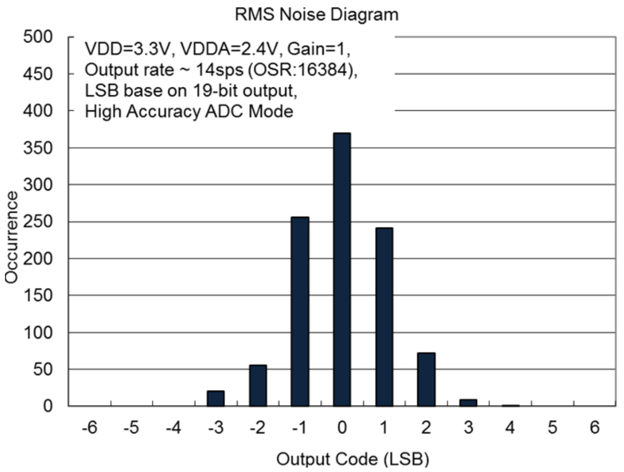



Figure 6.9-10 RMS Noise Diagram

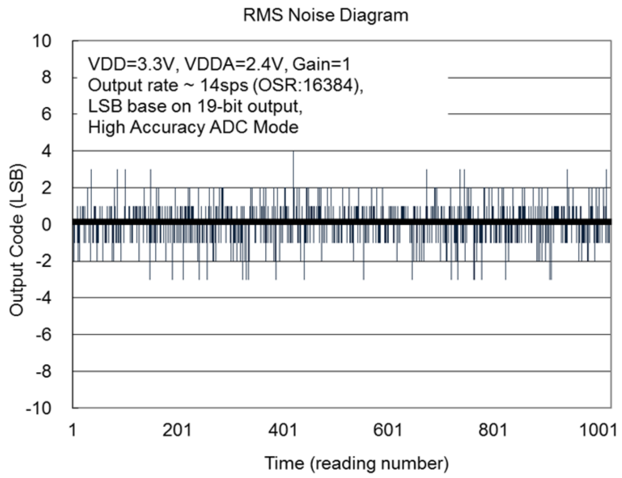



Figure 6.9-11 Output Code Diagram

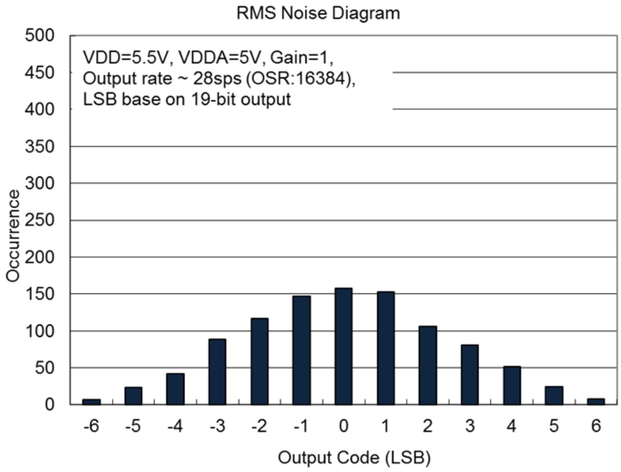



Figure 6.9-12 RMS Noise Diagram

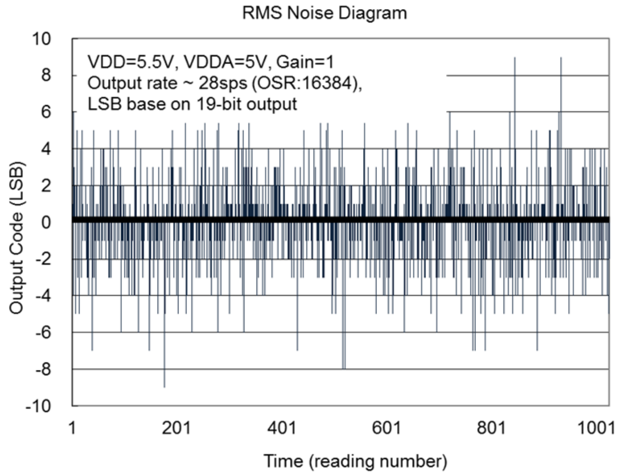



Figure 6.9-13 Output Code Diagram

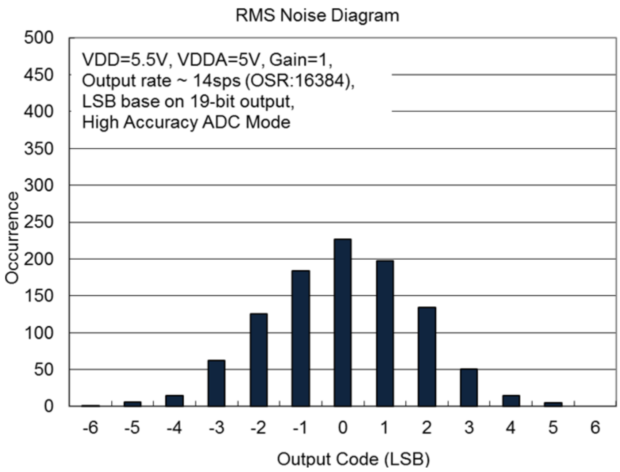



Figure 6.9-14 RMS Noise Diagram

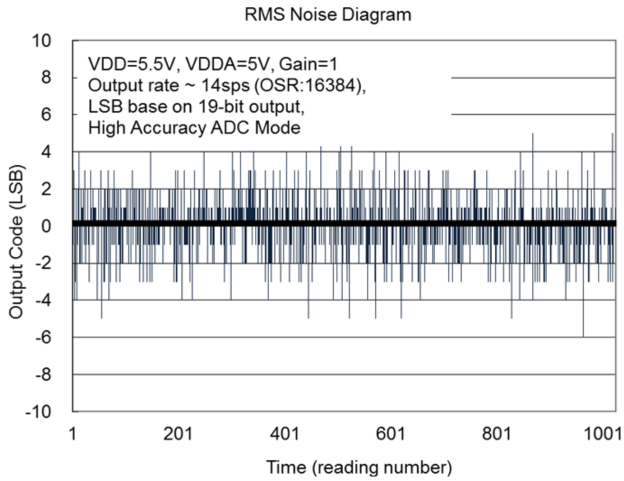



Figure 6.9-15 Output Code Diagram

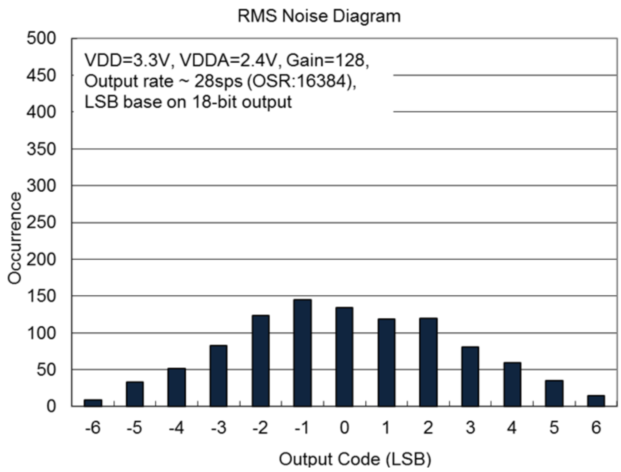



Figure 6.9-16 RMS Noise Diagram

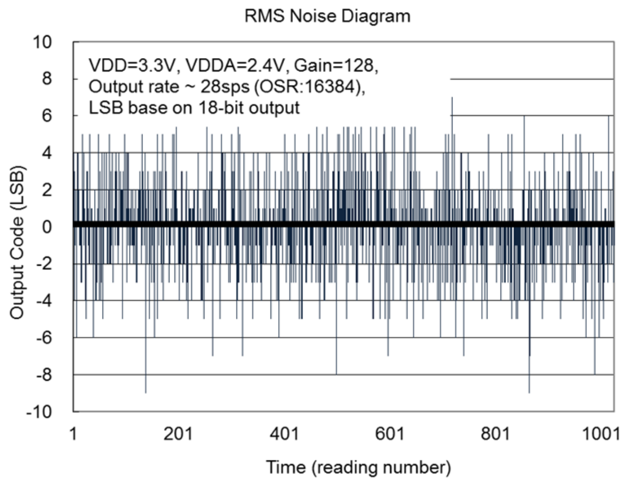



Figure 6.9-17 Output Code Diagram

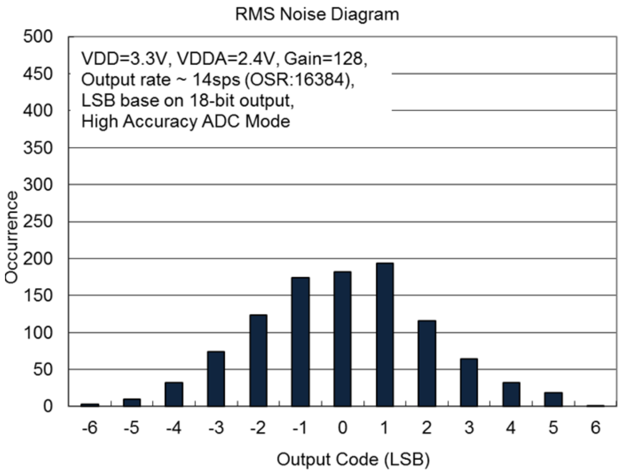



Figure 6.9-18 RMS Noise Diagram

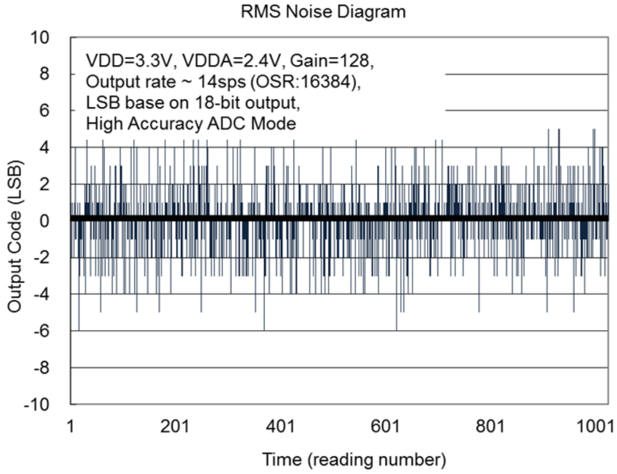



Figure 6.9-19 Output Code Diagram

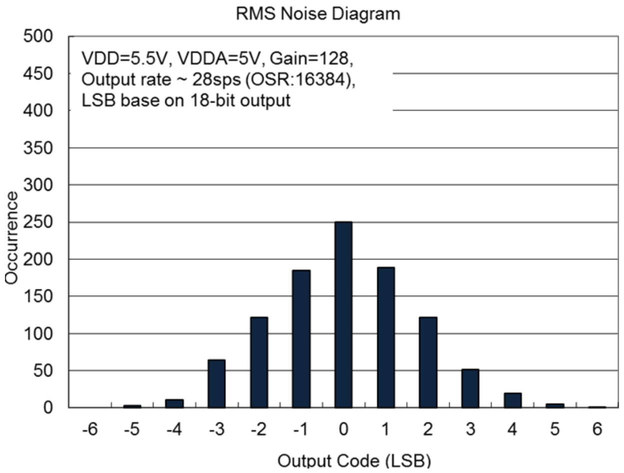



Figure 6.9-20 RMS Noise Diagram

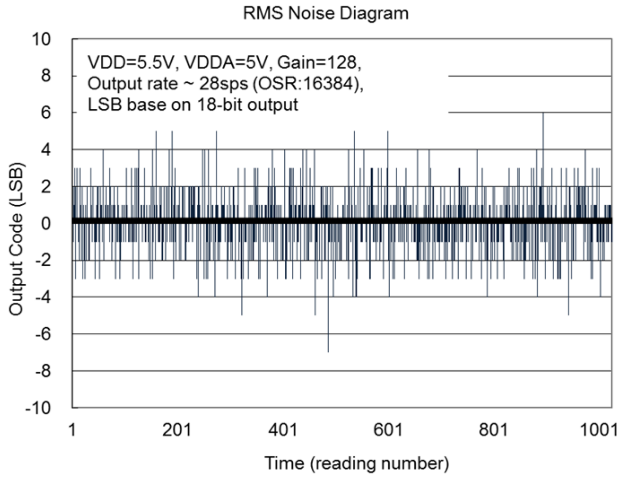



Figure 6.9-21 Output Code Diagram

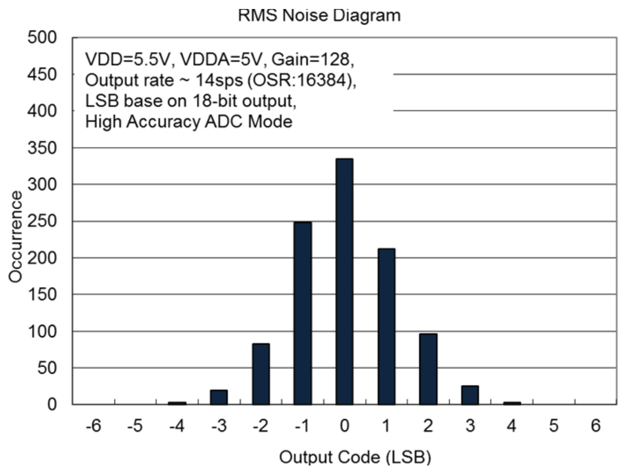



Figure 6.9-22 RMS Noise Diagram

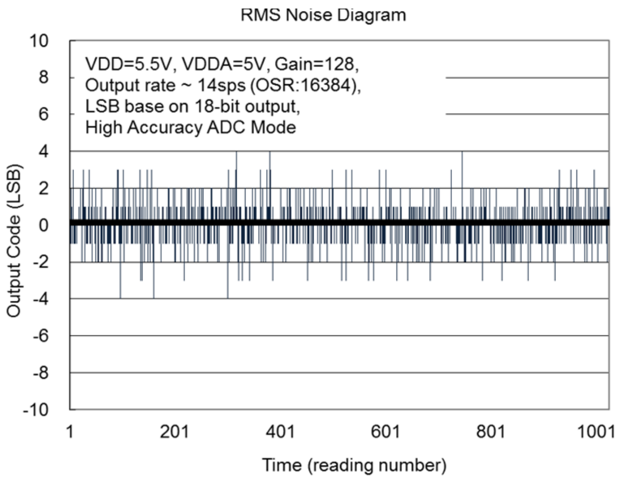



Figure 6.9-23 Output Code Diagram

### 6.9.4. ΣΔADC, Temperature Sensor

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $TC_S$ | Sensor temperature drift | | | 1.7 | | mV/℃ |
| $TC_{ERR}$ | One point calibrate error temperature | Calibration at 25℃ of -40℃~85℃ | | ±2 | | ℃ |

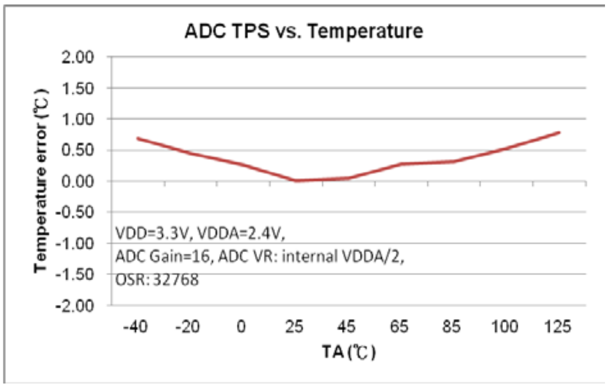



Figure 6.9-24 ADC Temperature Error

## 6.10. Build-In EPROM(BIE)

TA = 25℃,VDD = 3.0V, unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{BIE}$ | Supply Voltage at VPP PIN | | 7.5 | 7.75 | 8.0 | V |
| $I_{BIE}$ | Operation supply current | | | | 6.3 | mA |
| $V_{SS}$ | Supply Voltage | | | 0 | | V |
| When connecting to the external VBIE power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block. | | | | | | |

## 6.11. Build-In EPROM(BIE) Low voltage control circuit

TA = 25℃,VDD = 3.05V, unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_O$ | Operation temperature range | | 0 | 25 | 40 | ℃ |
| $V_{DD}$ | Operation supply Voltage | | 2.75 | | 5.5 | V |
| $V_{SS}$ | Supply Voltage | | | 0 | | V |
| When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external VBIE power source. | | | | | | |

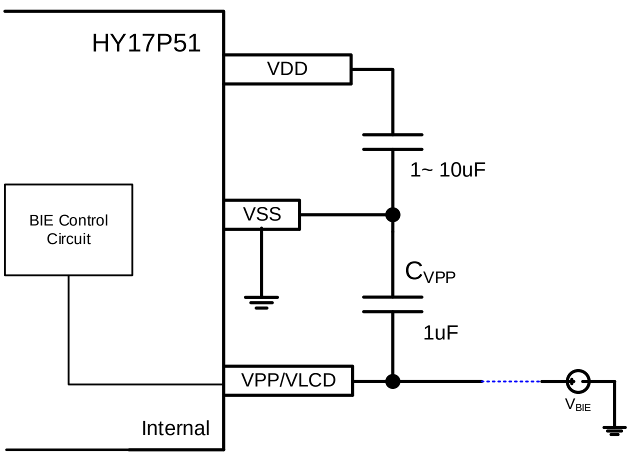



Figure 6.11-1 BIE typical application circuit

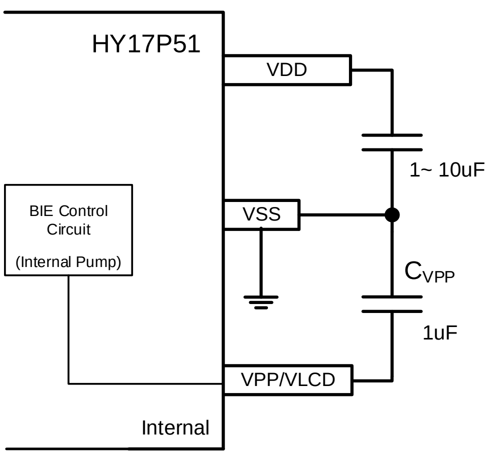



Figure 6.11-2 Use low voltage control circuit

## 7. Ordering Information

| Device No.[1] | Package Type | Pins | Package Drawing | | Code[2] | Shipment Packing Type | Unit Q'ty | Material Composition | MSL[3] |
|---|---|---|---|---|---|---|---|---|---|
| HY17P51-NS32 | QFN | 32 | N | S32 | 000 | Tape & Reel | 5000 | Green[4] | MSL-3 |
| HY17P51-N016 | QFN | 16 | N | 016 | 000 | Tape & Reel | 5000 | Green[4] | MSL-3 |

[1] **Device No.: Model No. – Package Type Description – Code (Blank Code/ Standard/Customized Programming Code)**

Ex: You request blank code in QFN32 package. The device No. will be HY17P51-NS32, and please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 008 and you require products in QFN32 package. The device No. will be HY17P51-NS32-008. and please clearly indicate the shipment packing type when placing orders.

Ex: You request blank code in QFN16 package. The device No. will be HY17P51-N016, and please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in QFN16 package. The device No. will be HY17P51-N016-009. and please clearly indicate the shipment packing type when placing orders.

[2] Code

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] MSL:

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

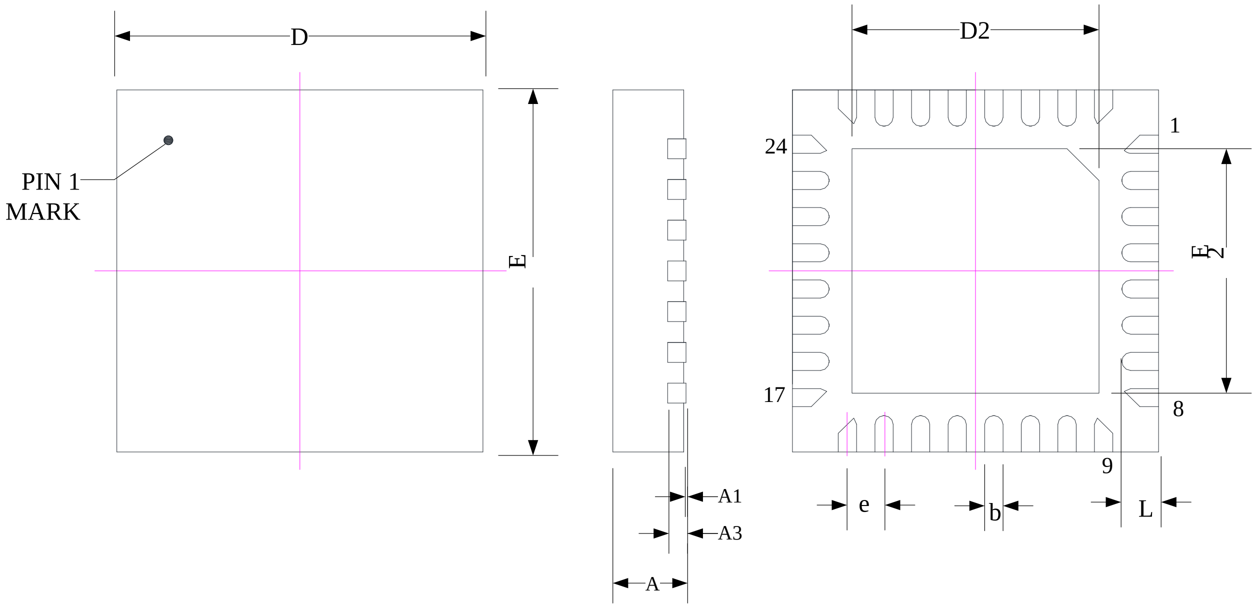
[4] Green (RoHS & no Cl/Br):

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

# 8. Package Information

## 8.1. QFN32(NS32)

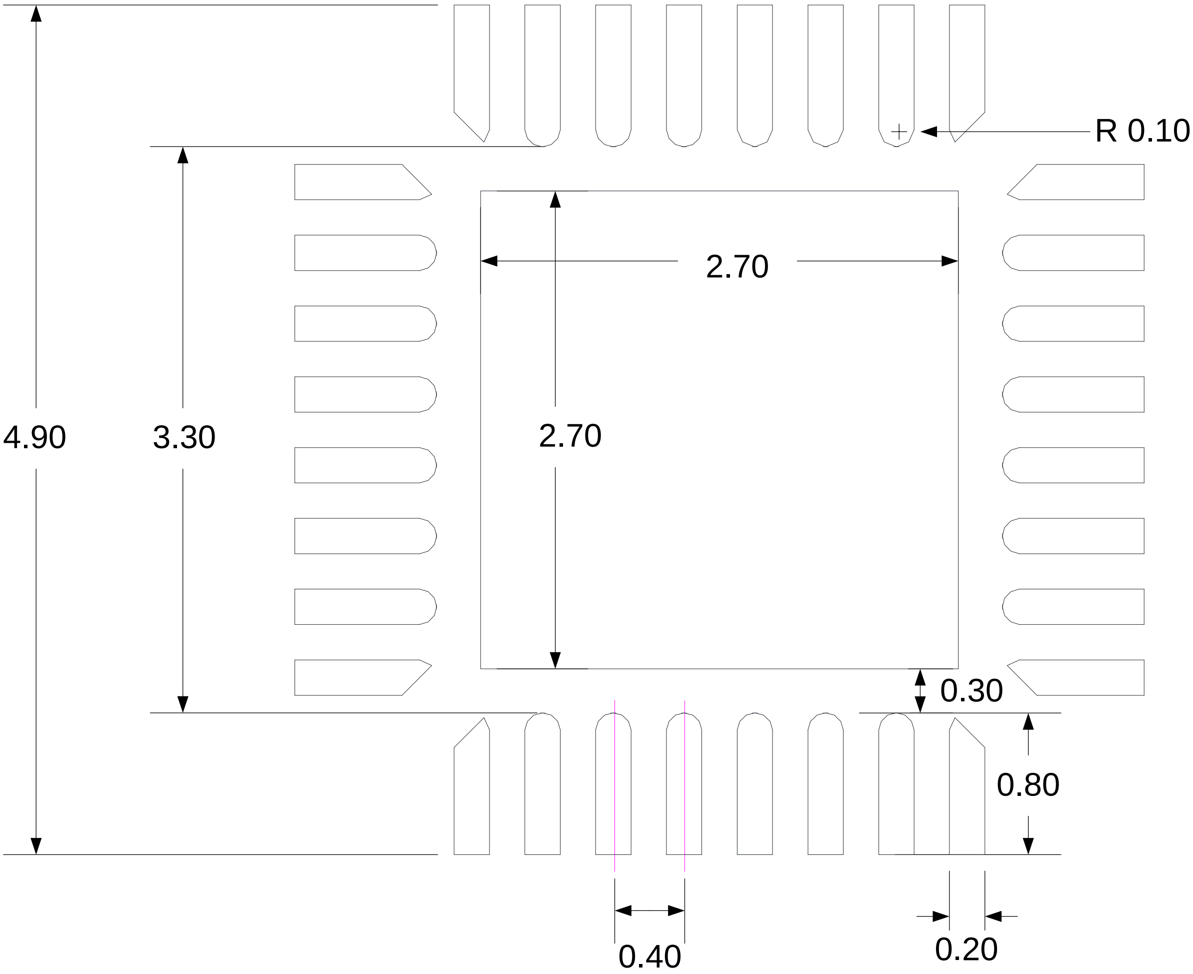
### 8.1.1. Package Dimensions QFN32(4x4x0.55)




| SYMBOLS | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.15 REF. | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 |
| D2 | 2.65 | 2.70 | 2.75 |
| E2 | 2.65 | 2.70 | 2.75 |
| L | 0.25 | 0.30 | 0.35 |
| e | 0.40 BASIC | | |

Note:
1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB_EN.pdf

### 8.1.2. Land Pattern Design Recommendations

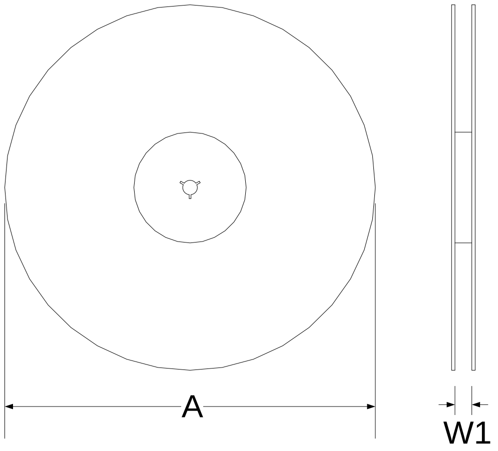



Note:
1. Publication IPC-7351 is recommended for alternate designs.
2. Unit: mm.
3. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB_EN.pdf

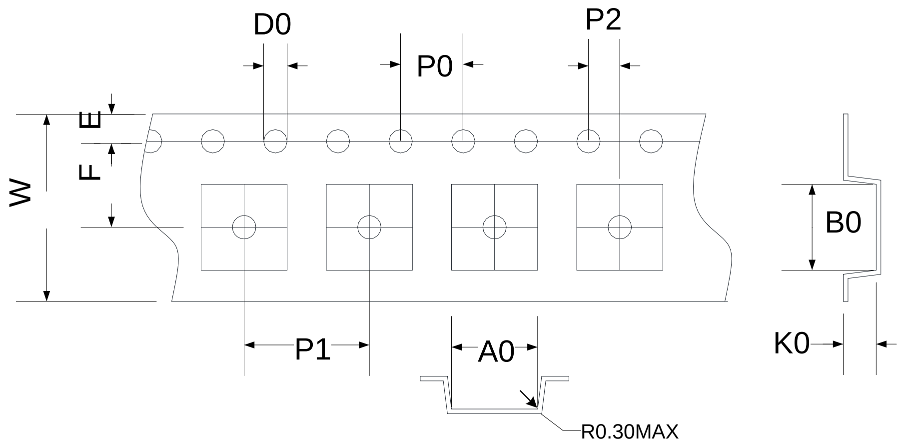
### 8.1.3. Tape & Reel Information

#### 8.1.3.1. Reel Dimensions

Unit: mm



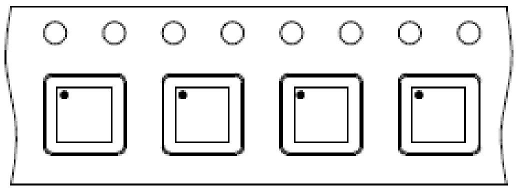

#### 8.1.3.2. Carrier Tape Dimensions




| SYMBOLS | Reel Dimensions | | Carrier Tape Dimensions | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | W1 | A0 | B0 | K0 | P0 | P1 | P2 | E | F | D0 | W |
| Spec. | 330 | 12.5 | 4.35 | 4.35 | 1.10 | 4.00 | 8.00 | 2.00 | 1.75 | 5.50 | 1.50 | 12.00 |
| Tolerance | +6/-3 | +1.5/-0 | ±0.10 | ±0.10 | ±0.10 | ±0.10 | ±0.10 | ±0.05 | ±0.10 | ±0.05 | +0.1/-0 | ±0.30 |

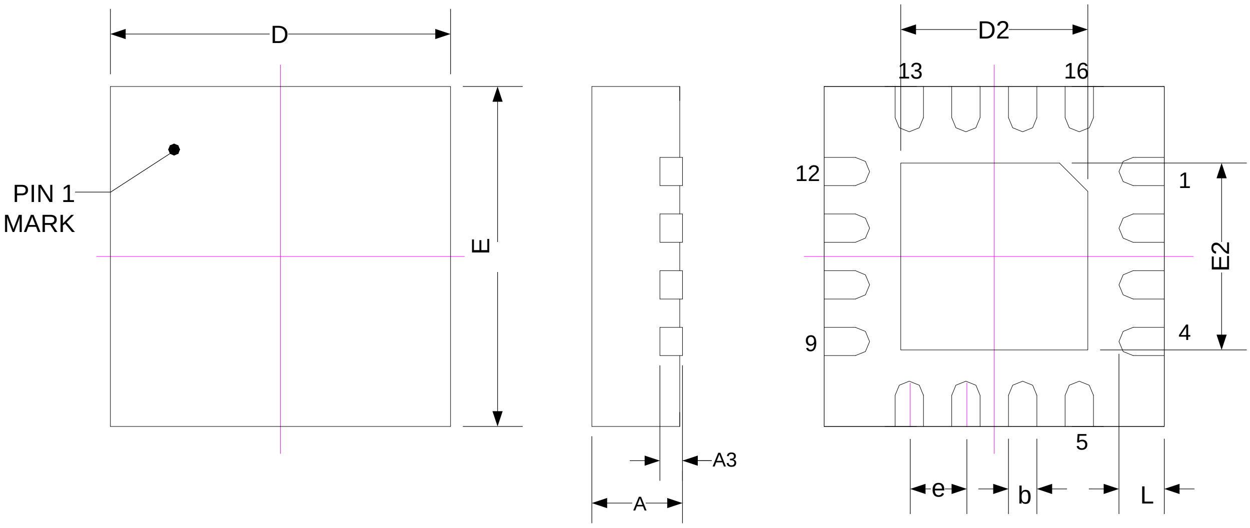
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

#### 8.1.3.3. Pin1 direction



### 8.2. QFN16(N016)

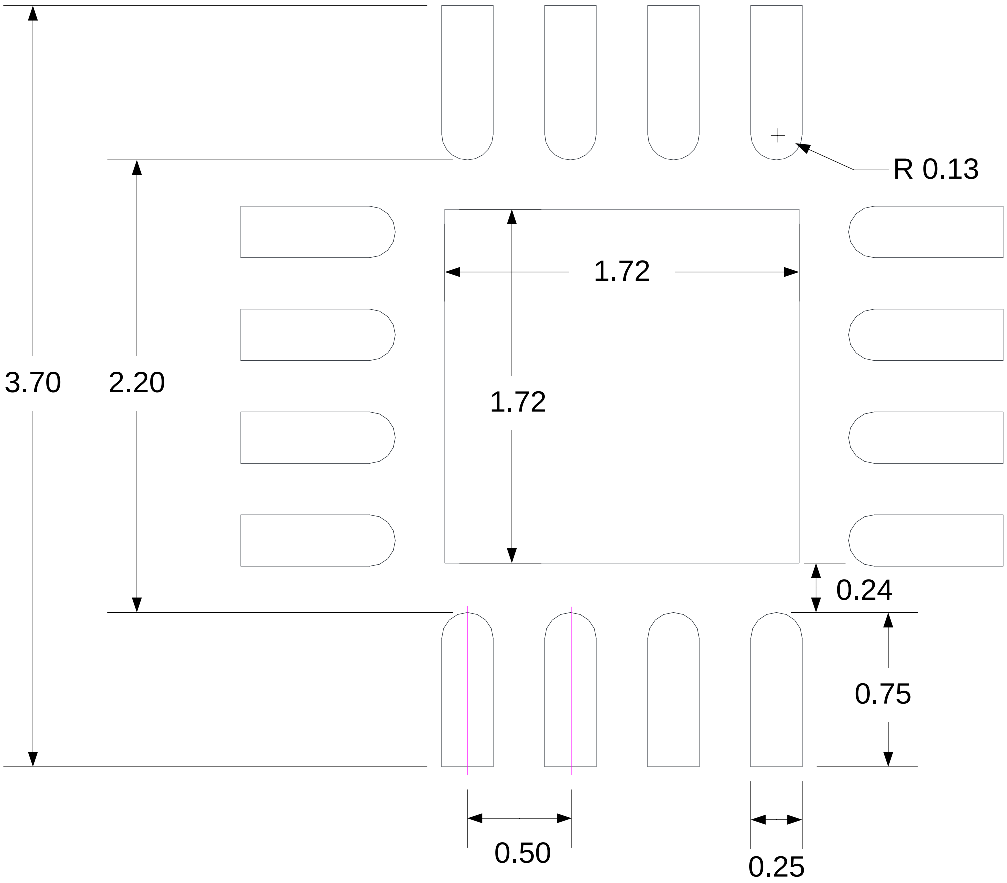
#### 8.2.1. Package Dimensions QFN16(3x3x0.75)




| SYMBOLS | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A3 | 0.203 REF. | | |
| b | 0.20 | 0.25 | 0.30 |
| D | 2.925 | 3.000 | 3.075 |
| E | 2.925 | 3.000 | 3.075 |
| D2 | 1.625 | 1.725 | 1.825 |
| E2 | 1.625 | 1.725 | 1.825 |
| L | 0.30 | 0.35 | 0.40 |
| e | 0.50 BASIC | | |

Note:
1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB_EN.pdf

### 8.2.2. Land Pattern Design Recommendations

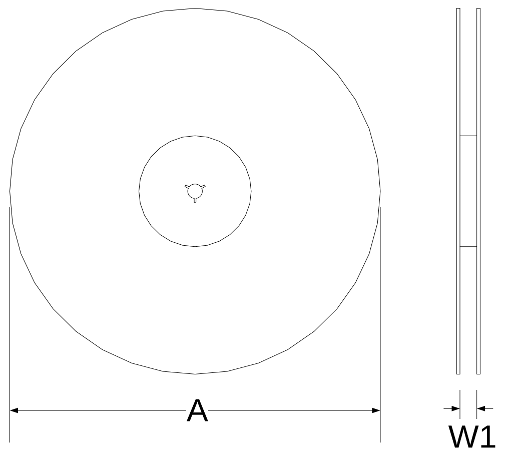



Note:
1. Publication IPC-7351 is recommended for alternate designs.
2. Unit: mm.
3. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB_EN.pdf

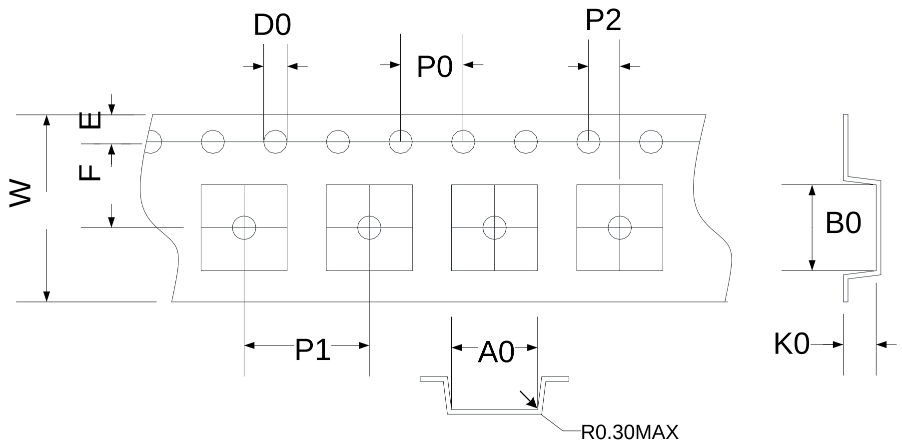
### 8.2.3. Tape & Reel Information

#### 8.2.3.1. Reel Dimensions

Unit: mm



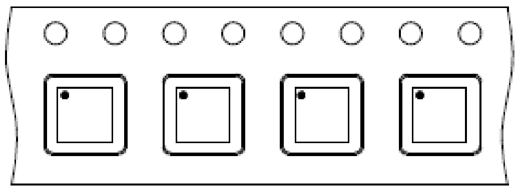

#### 8.2.3.2. Carrier Tape Dimensions




| SYMBOLS | Reel Dimensions | | Carrier Tape Dimensions | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | W1 | A0 | B0 | K0 | P0 | P1 | P2 | E | F | D0 | W |
| Spec. | 330 | 12.5 | 3.30 | 3.30 | 1.10 | 4.00 | 8.00 | 2.00 | 1.75 | 5.50 | 1.50 | 12.00 |
| Tolerance | +6/-3 | +1.5/-0 | ±0.10 | ±0.10 | ±0.10 | ±0.10 | ±0.10 | ±0.05 | ±0.10 | ±0.05 | +0.1/-0 | ±0.30 |

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

#### 8.2.3.3. Pin1 direction



# 9. Revision Record

Major differences are stated thereinafter.

| Version | Page | Date | Revision Summary |
|---|---|---|---|
| V02 | All | 2022/08/25 | First edition |
| | | | |