HY17P52
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x14 LCD Driver
Embedded High Resolution ΣΔADC

Table of Contents

Attention:

1、HYCON Technology Corp. reserves the right to change the content of this datasheet without further notice. For most up-to-date information, please constantly visit our website: http://www.hycontek.com .

2、HYCON Technology Corp. is not responsible for problems caused by figures or application circuits narrated herein whose related industrial properties belong to third parties.

3、Specifications of any HYCON Technology Corp. products detailed or contained herein stipulate the performance, characteristics, and functions of the specified products in the independent state. We does not guarantee of the performance, characteristics, and functions of the specified products as placed in the customer's products or equipment. Constant and sufficient verification and evaluation is highly advised.

4、Please note the operating conditions of input voltage, output voltage and load current and ensure the IC internal power consumption does not exceed that of package tolerance. HYCON Technology Corp. assumes no responsibility for equipment failures that resulted from using products at values that exceed, even momentarily, rated values listed in products specifications of HYCON products specified herein.

5、Notwithstanding this product has built-in ESD protection circuit, please do not exert excessive static electricity to protection circuit.

6、Products specified or contained herein cannot be employed in applications which require extremely high levels of reliability, such as device or equipment affecting the human body, health/medical equipments, security systems, or any apparatus installed in aircrafts and other vehicles.

7、Despite the fact that HYCON Technology Corp. endeavors to enhance product quality as well as reliability in every possible way, failure or malfunction of semiconductor products may happen. Hence, users are strongly recommended to comply with safety design including redundancy and fire-precaution equipments to prevent any accidents and fires that may follow.

8、Use of the information described herein for other purposes and/or reproduction or copying without the permission of HYCON Technology Corp. is strictly prohibited.

1. Features

- 8-Bit RISC-like microcontrollers with 71 high-performance instruction set H08D (same as H08A),support C compiler
- Operating voltage and operating temperature range
  - VDD：2.2V ~ 5.5V
  - VDDA：2.4V & 3.6V
  - -40°C ~ 85°C
- Internal High Precision RC Oscillator, Many CPU clock rates enable users to have the most power-saving plan.
  - Active mode
  - Idle mode
  - Sleep mode
- Memory
  - 4K words OTP program memory
  - 256 bytes data memory
  - Support 8 stack level
- Reset
  - Power On Reset
  - Brown Out Reset
  - Watch Dog Reset
  - Stack Over Reset
- 4 X 14 LCD Driver
  - 1/4 Duty 1/3 Bias
  - Built-in charge pump regulated circuit providing 8 LCD bias voltage
  - 2 SEG ports can set as digital output
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function
- VDDA has 10mA regulated voltage source output, with fast start function to provide sensor driving voltage.
- 24-Bit ΣΔADC
  - Built-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x
  - Zero point bias translation controller
  - Sampling frequency 921KHz
  - Settable over-sampling rate is 64~65536
  - Diverse data output rate. Max. 7.2Ksps
  - Built-in absolute temperature sensor
- Timer
  - Watch Dog
    - Reset event
    - Interrupt event
  - 1 channels 8-bit Timer A1
    - Interrupt event
    - Compare events
- 64 words Built-In EPROM (BIE), 2.75V low voltage programming control circuit
- Interface
  - 1 channels serial communication EUART module
- Package
  - LQFP48

Function List

Model No.	VDD (V)	Internal Clock (Hz)	System Clock (Hz)	Program Memory (word)	SRAM (byte)	BIE (byte)	ADC ENOB (bit x ch)	Sample Rate (sps)	LCD (com x seg)	I/O	Timer (bit x ch)	Serial Interface (I/F x ch)	Package
HY17P52	2.2~5.5	14.5K 1.843M 3.686M 7.834M	14.5K ~ 8M	4K	256	64LV	20-bit x4	8~7.2K	4 x 14	10xIO + 2xO	8-bit x 1	EUARTx1	LQFP48

2. Pin Definition

2.1. LQFP48 Pin Diagram

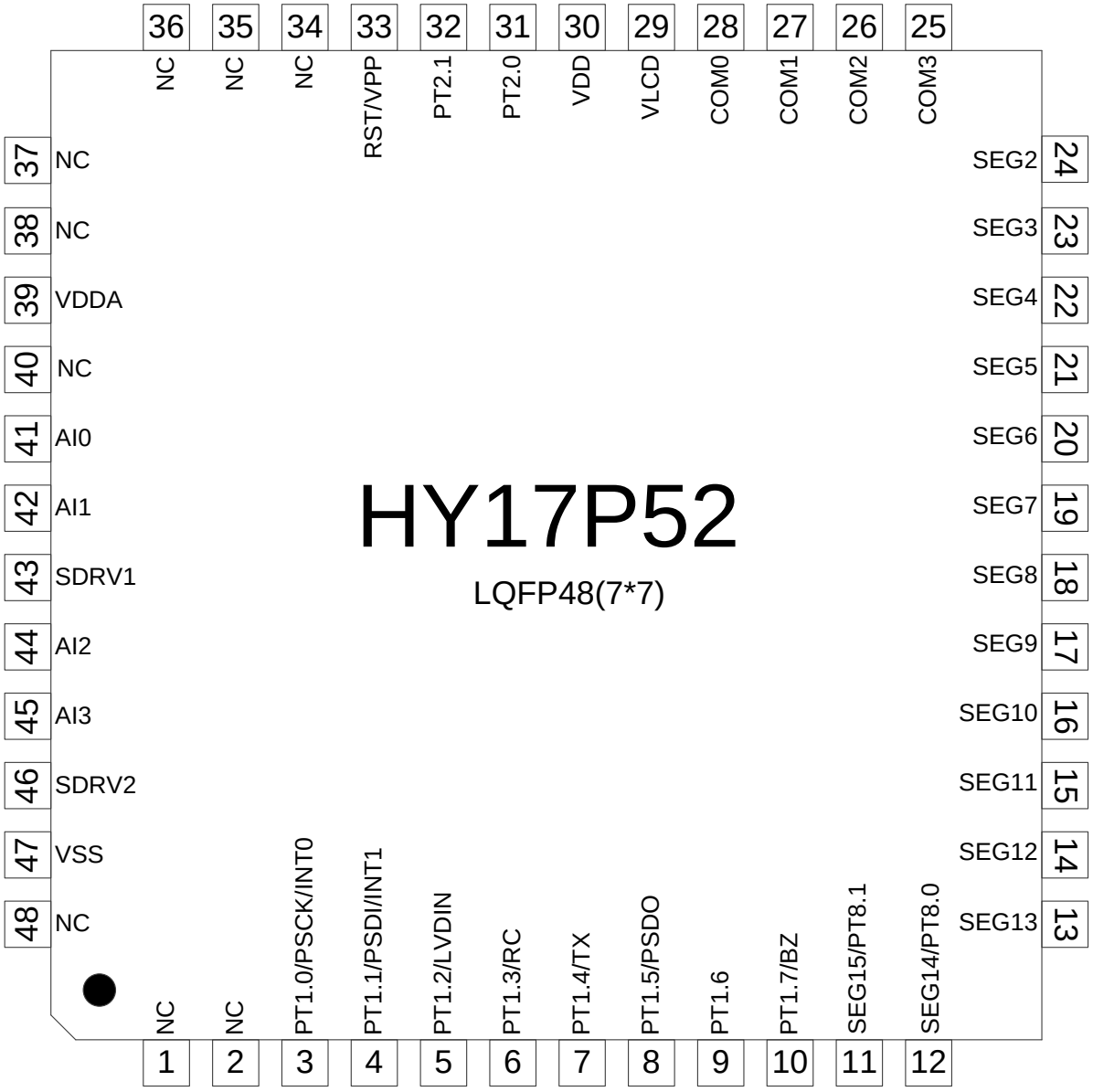


Figure 2-1 QFN32 Pin Diagram

Note: VPP and RST reuse the same PIN, input of high voltage is prohibited when OTP is not burned

2.2. Pinout I/O Description

"I/O"Inout/Output,"I"Input,"O"Output,"S"Smith triggers,"C"CMOS,"P"Power Source,"A"Analog channel

LQFP48 Pin No.	Pin Name	Characteristic		Description
		Type	Buffer	
3	PT1.0/INT1.0/PSCK			
	PT1.0	I/O	S/C	Digital input / output pin
	INT1.0	I	S	External interrupt source input pin
	PSCK	I	S	OTP read / write interface pin, PSCK
4	PT1.1/INT1.1/PSDI			
	PT1.1	I/O	S/C	Digital input / output pin
	INT1.1	I	S	External interrupt source input pin
	PSDI	I	S	OTP read / write interface pin, PSDI
5	PT1.2/LVDIN			
	PT1.2	I/O	S/C	Digital input / output pin
	LVDIN	A	A	LVD external signal input port
6	PT1.3/RC			
	PT1.3	I/O	S/C	Digital input / output pin
	RC	I	S	RC pin of EUART interface
7	PT1.4/TX			
	PT1.4	I/O	S/C	Digital input / output pin
	TX	O	C	TX pin of EUART interface
8	PT1.5/PSDO			
	PT1.5	I/O	S/C	Digital input / output pin
	PSDO	O	C	OTP read / write interface pin, PSDO
9	PT1.6			
	PT1.6	I/O	S/C	Digital input / output pin
10	PT1.7/BZ			
	PT1.7	I/O	S/C	Digital input / output pin
	BZ	O	C	Buzzer Signal Output pin
11	PT8.1/SEG15			
	PT8.1	O	C	Digital Output pin
	SEG15	O	A	LCD Segment output pin
12	PT8.0/SEG14			
	PT8.0	O	C	Digital output pin
	SEG14	O	A	LCD Segment output pin
13	SEG13			
	SEG13	O	A	LCD Segment output pin

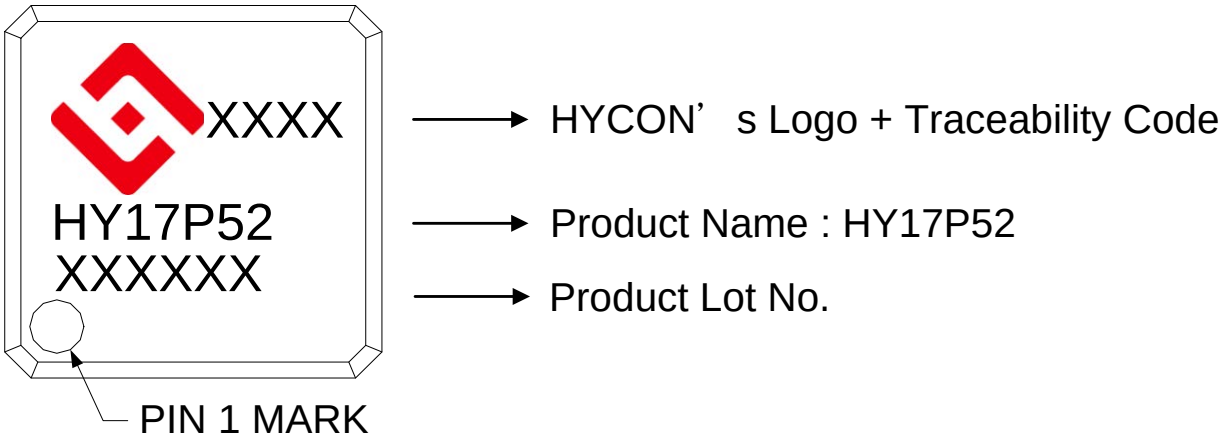
14	SEG12 SEG12	O	A	LCD Segment output pin
15	SEG11 SEG11	O	A	LCD Segment output pin
16	SEG10 SEG10	O	A	LCD Segment output pin
17	SEG9 SEG9	O	A	LCD Segment output pin
18	SEG8 SEG8	O	A	LCD Segment output pin
19	SEG7 SEG7	O	A	LCD Segment output pin
20	SEG6 SEG6	O	A	LCD Segment output pin
21	SEG5 SEG5	O	A	LCD Segment output pin
22	SEG4 SEG4	O	A	LCD Segment output pin
23	SEG3 SEG3	O	A	LCD Segment output pin
24	SEG2 SEG2	O	A	LCD Segment output pin
25	COM3 COM3	O	A	LCD COM output pin
26	COM2 COM2	O	A	LCD COM output pin
27	COM1 COM1	O	A	LCD COM output pin
28	COM0 COM0	O	A	LCD COM output pin
29	VLCD	P	P	Power Source of LCD
30	VDD	P	P	Chip Power Voltage Input, an external 1~10uF capacitor is required.
31	PT2.0 PT2.0	I/O	S/C	Digital input / output pin
32	PT2.1 PT2.1	I/O	S/C	Digital input / output pin

33	RST/VPP RST VPP	I P	S P	External Reset pin (Low active) OTP burning voltage source input pin
39	VDDA	P	P	LDO output, Analog circuit voltage source, an external 1~10uF capacitor is required.
41	AI0	A	A	Analog input channel 0
42	AI1	A	A	Analog input channel 1
43	SDRV1	O	P	Sensor Power
44	AI2	A	A	Analog input channel 2
45	AI3	A	A	Analog input channel 3
46	SDRV2	O	P	Sensor Power
47	VSS	P	P	System Power Ground
Others	NC	-	-	Not used (not connectable

Table 2-1 Pin Definition and Function Description

2.3. Package marking information

2.3.1. LQFP Package marking information



3. Application Circuit

3.1. Bridge Sensor with LCD

3.1.1. Standard Version

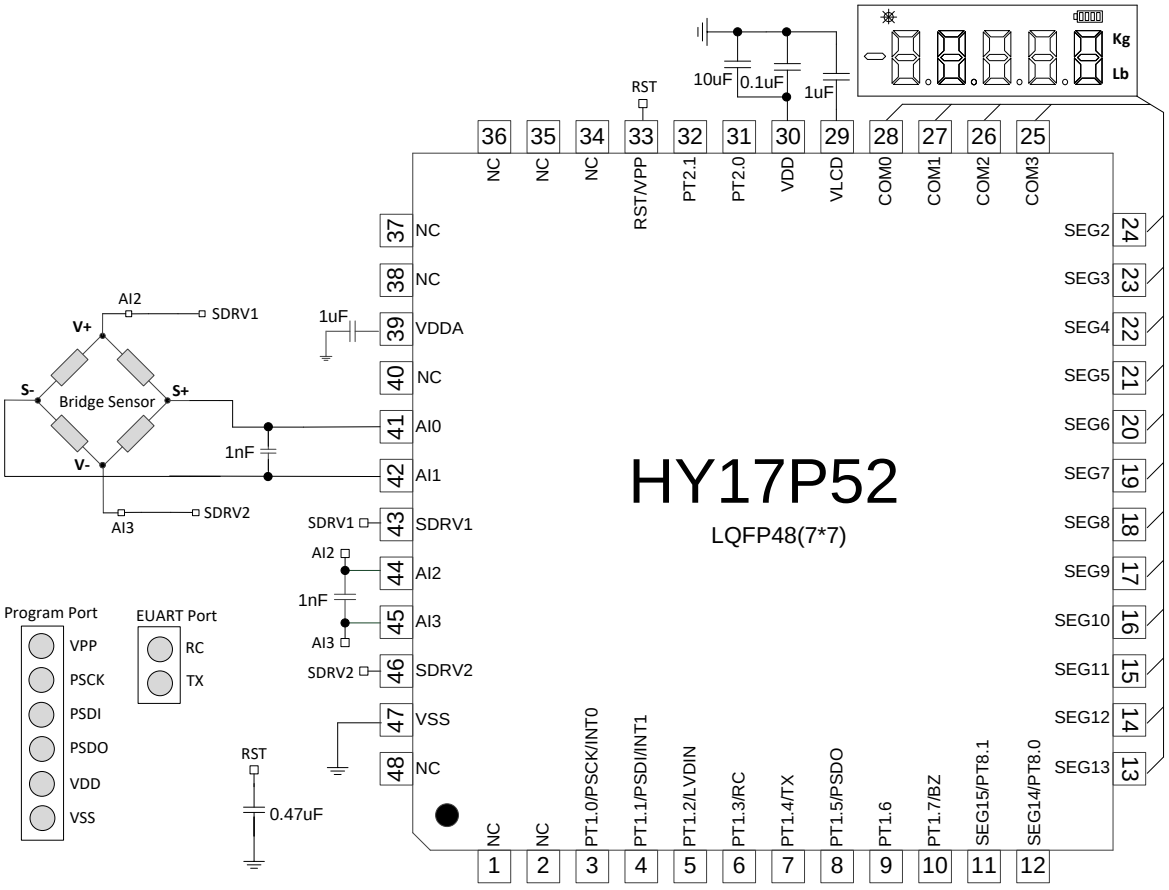


Figure 3-1 Bridge Sensor with LCD-Standard Version

3.1.2. Anti RS Interference Version

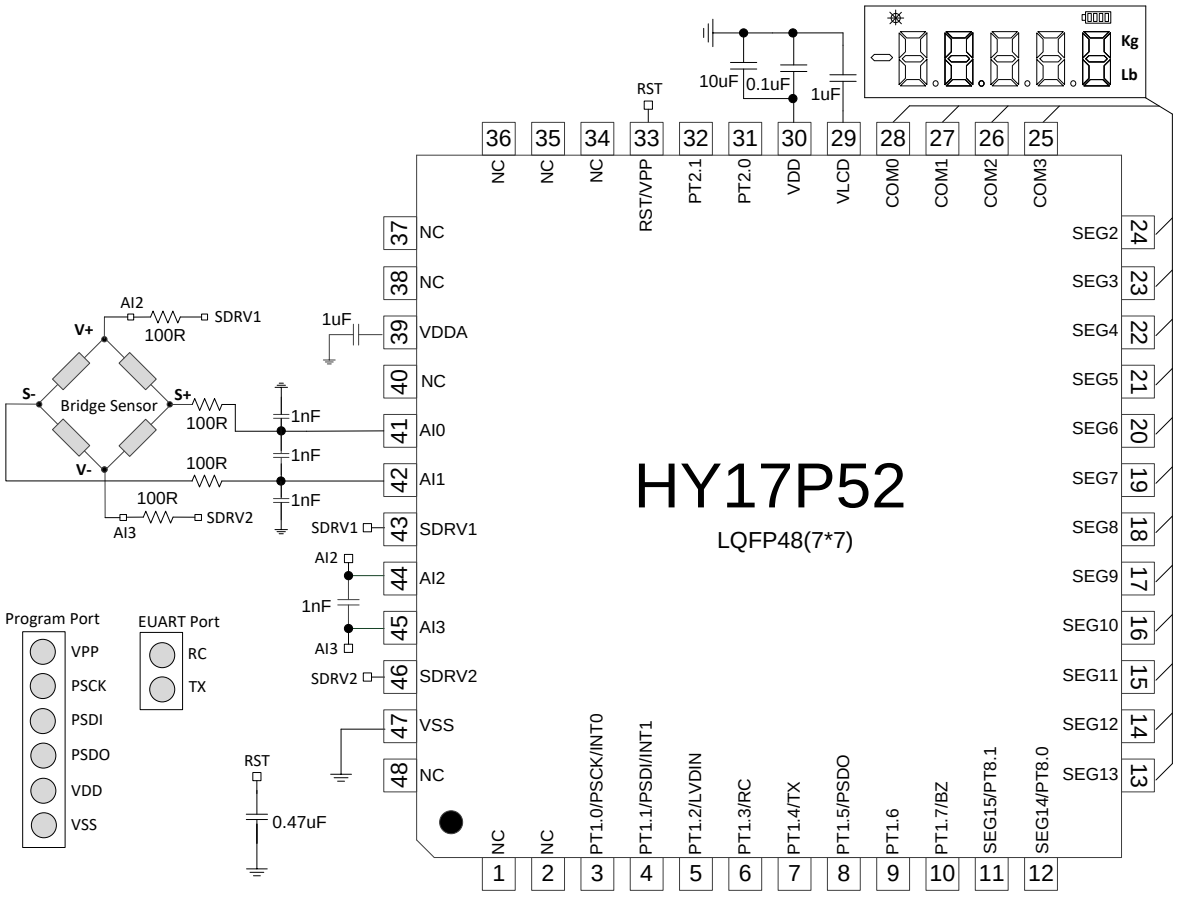
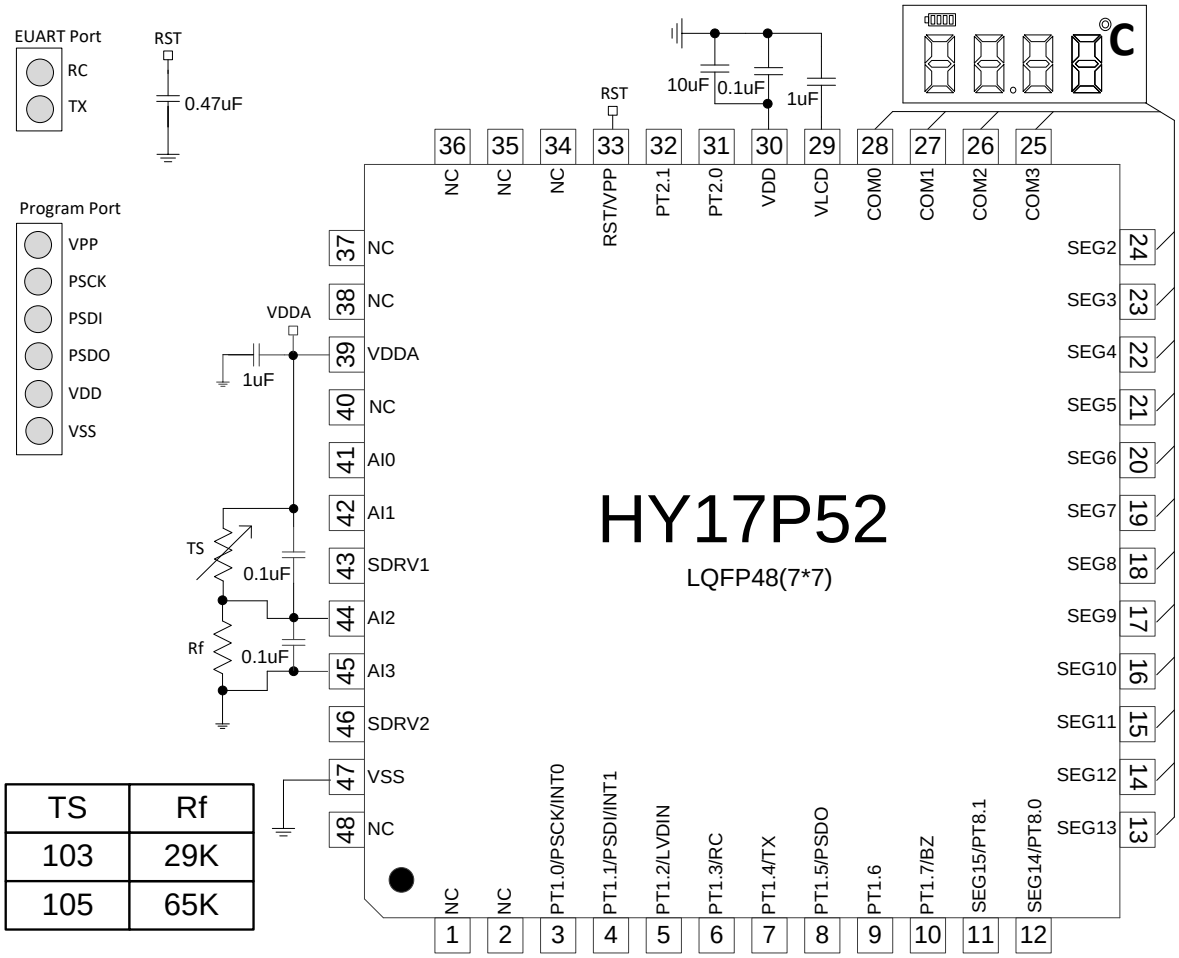


Figure 3-2 Bridge Sensor with LCD-Anti RS Interference Version

3.2. Digital Thermometer with LCD display



TS	Rf
103	29K
105	65K

Figure 3-3 Digital Thermometer application reference circuit

4. Function Outline

4.1. Internal Block Diagram

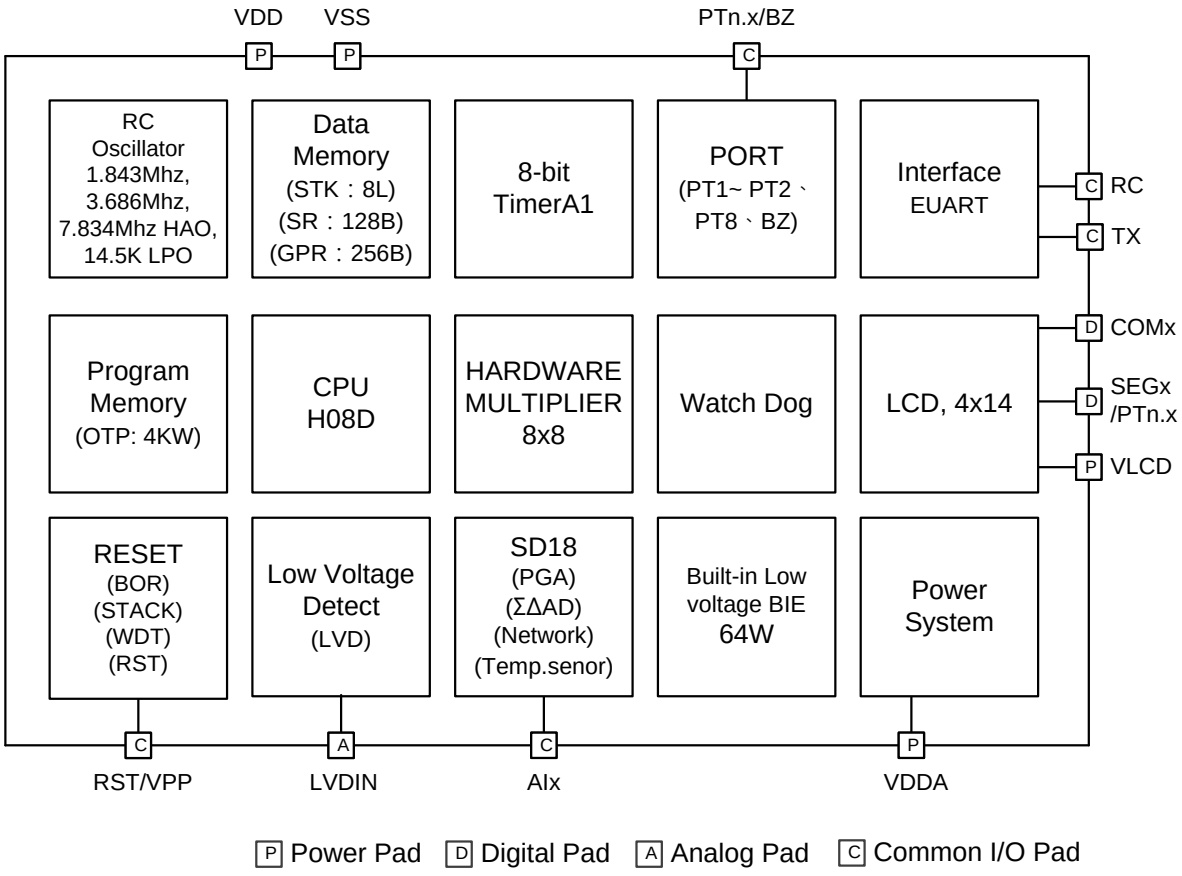


Figure 4-1 Internal Block Diagram

4.2. Related Description and Supporting Document

File Name	Description
DS-HY17P52	HY17P52 Datasheet
UG-HY17S58	HY17S58 chip User's Manual
APD-CORE002	H08A, H08C, H08D Instruction Set User's Manual
APD-HY17PIDE001	HY17P Series development tool software User's Manual
APD-HY17PIDE002	HY17P Series development tool hardware User's Manual
APD-HYIDE016	H08 C IDE software User's Manual
APD-HY17PIDE003	HY17P4x/5x Series Peripheral Driver C Library User's Manual
APD-HY17PIDE004	HY17P Series HexLoader User's Manual
APD-HYIDE014	HY10000-WK08D Integrated Writer software User's Manual
APD-HYIDE013	HY10000-WK08D Integrated Writer hardware User's Manual

4.3. Clock System

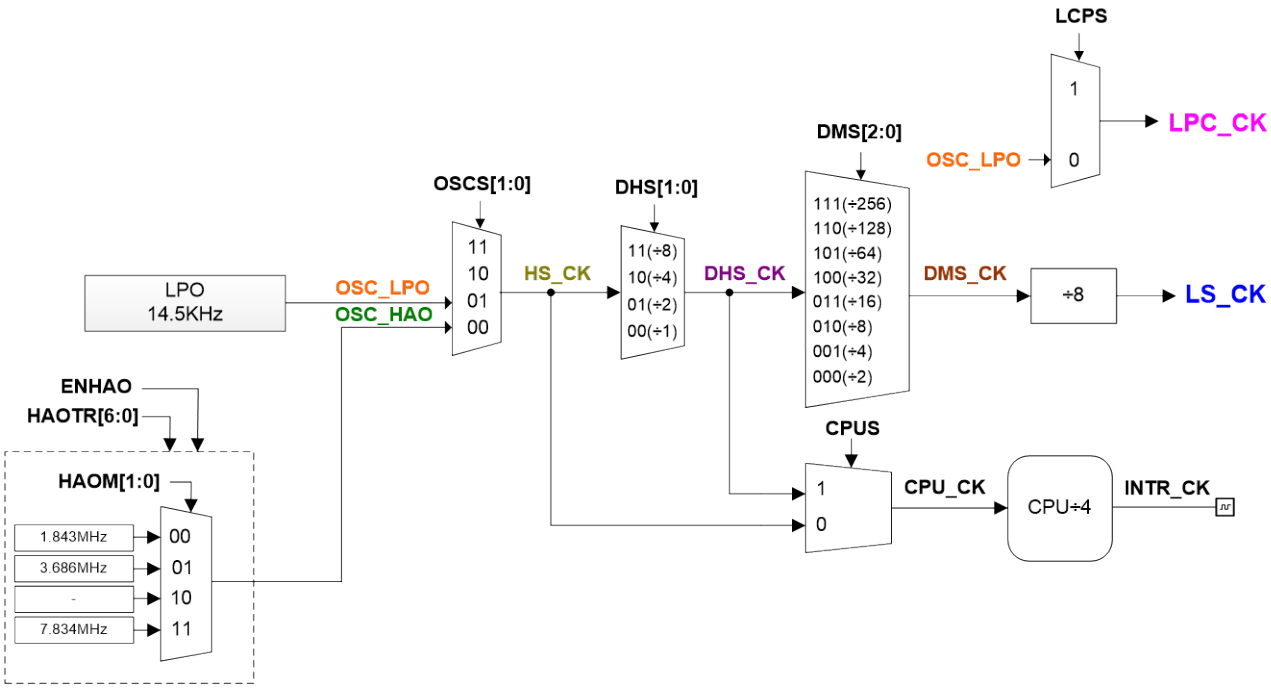


Figure 4-2 Clock System block diagram (1)

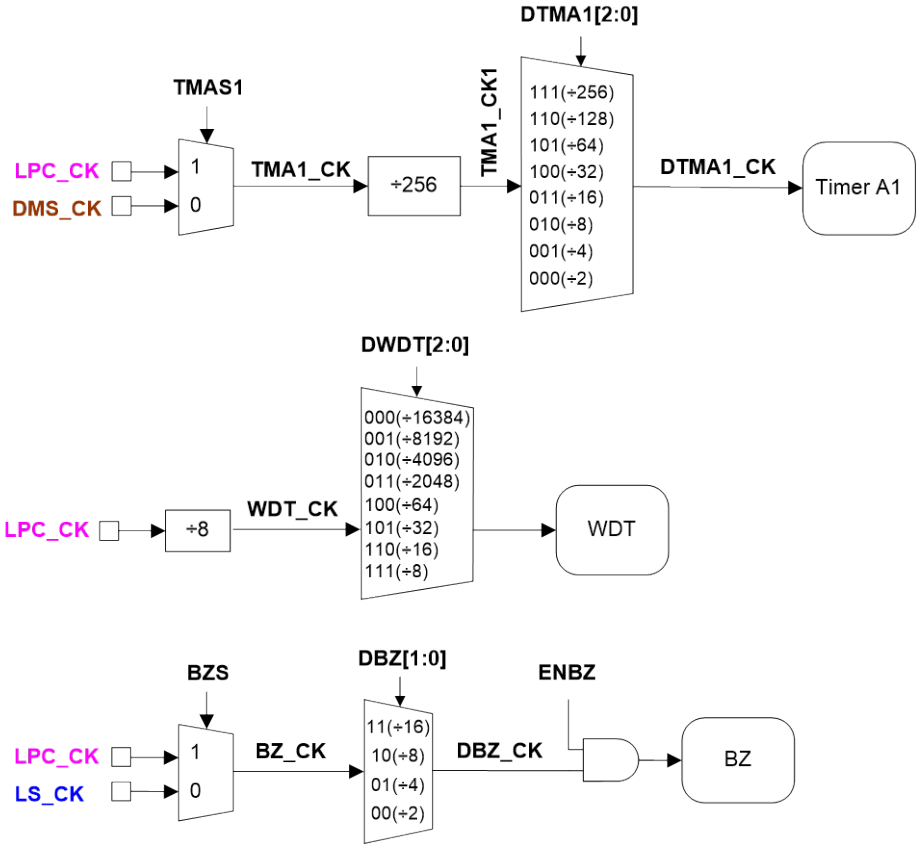


Figure 4-3 Clock System block diagram (2)

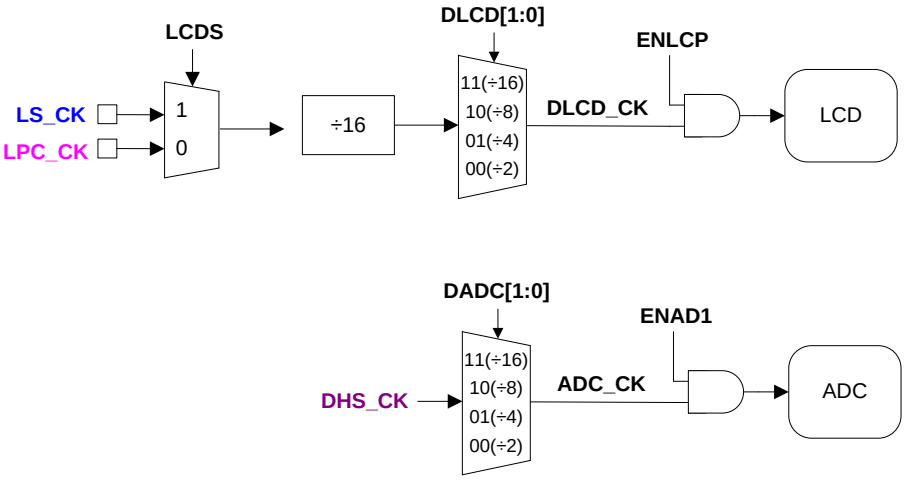


Figure 4-4 Clock System block diagram (3)

4.4. Low Voltage Detect(LVD)

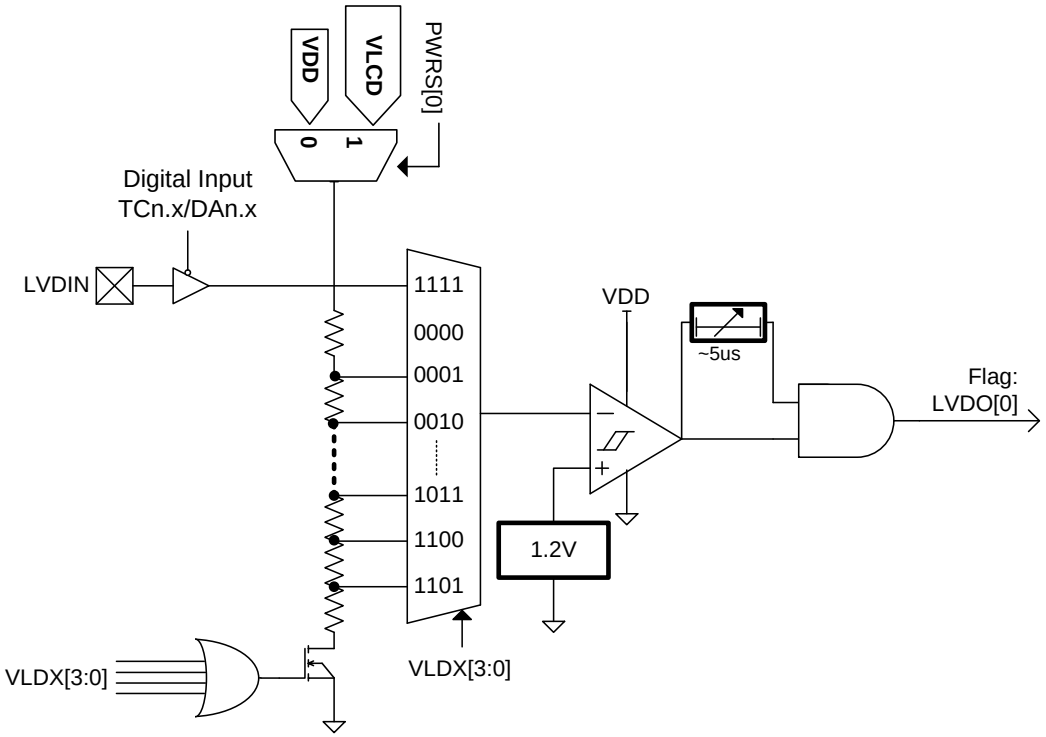


Figure 4-5 Low Voltage Detect block diagram

4.5. Reset

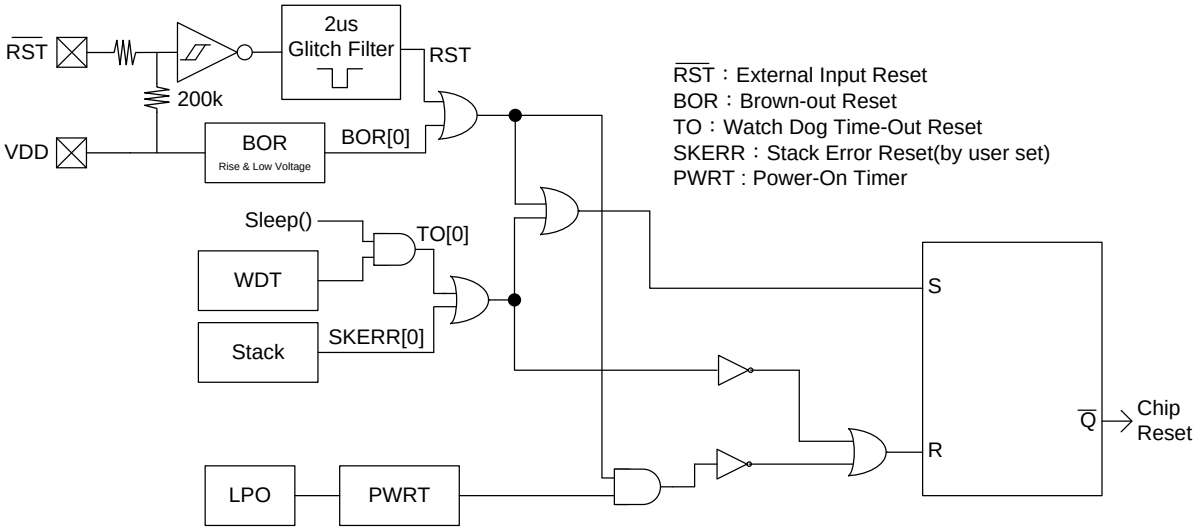


Figure 4-6 Reset block diagram

4.6. Power System

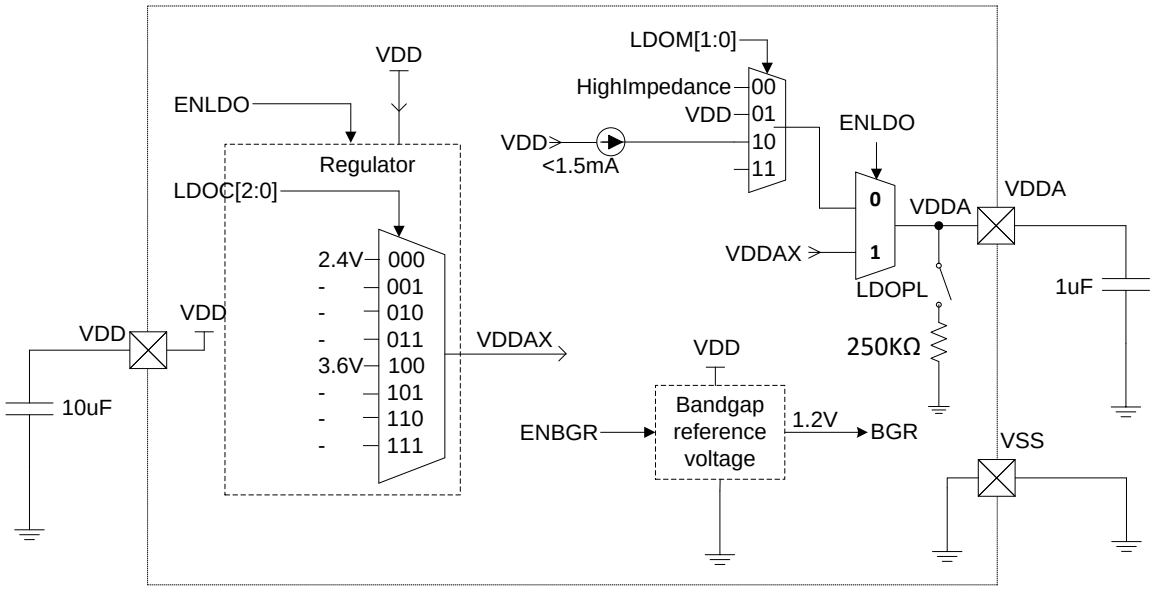
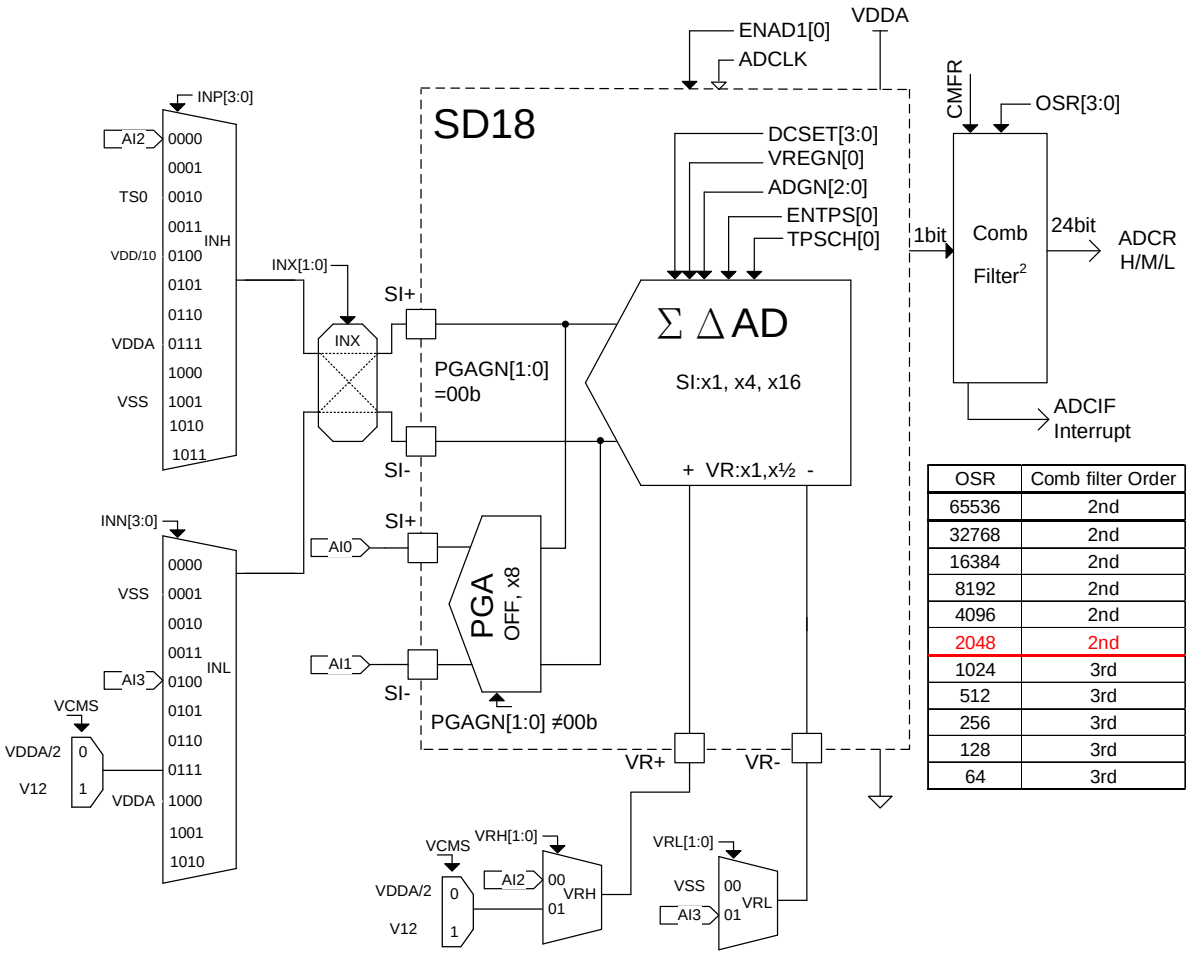


Figure 4-7 Power System block diagram

4.7. ΣΔADC Network



OSR	Comb filter Order
65536	2nd
32768	2nd
16384	2nd
8192	2nd
4096	2nd
2048	2nd
1024	3rd
512	3rd
256	3rd
128	3rd
64	3rd

Figure 4-8 ΣΔADC Network

4.8. GPIO PT1 and PT2

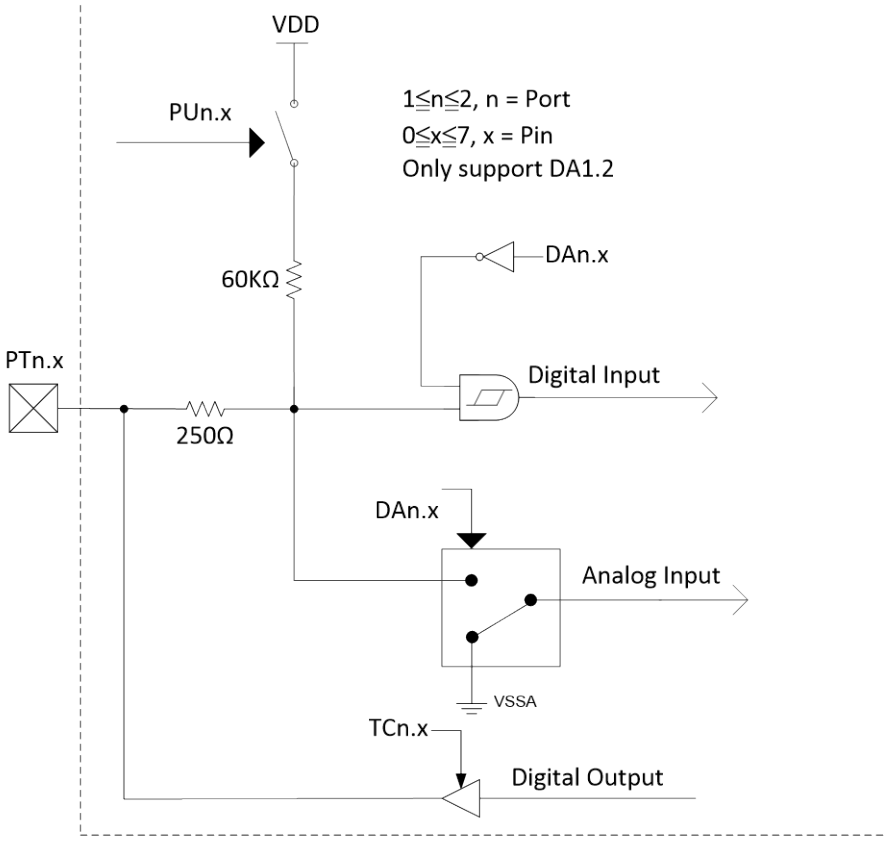


Figure 4-9 GPIO PT1 and PT2 block diagram

4.9. GPIO PT8/SEG14~SEG15

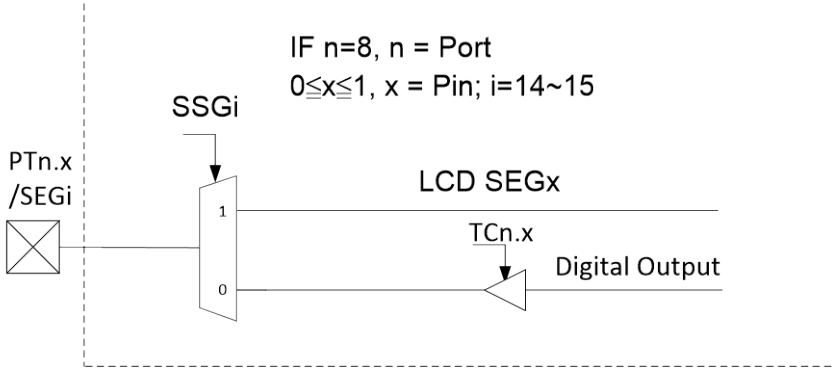


Figure 4-10 GPIO PT8/SEG14~SEG15 block diagram

4.10. Watch Dog

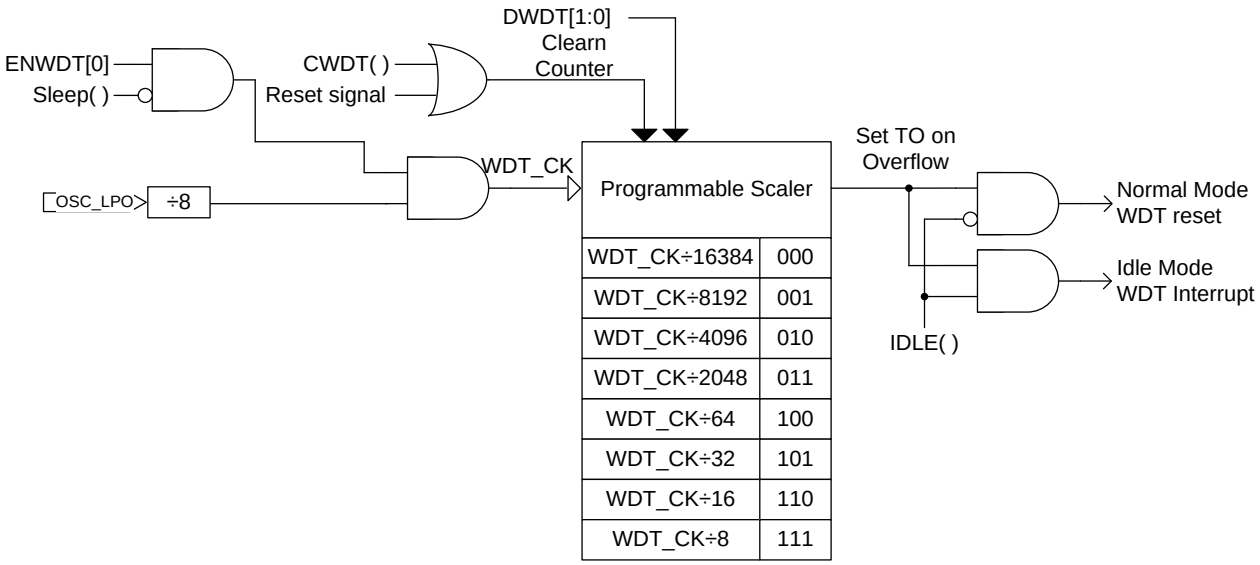


Figure 4-11 Watch Dog block diagram

4.11. 8-bit Timer A1

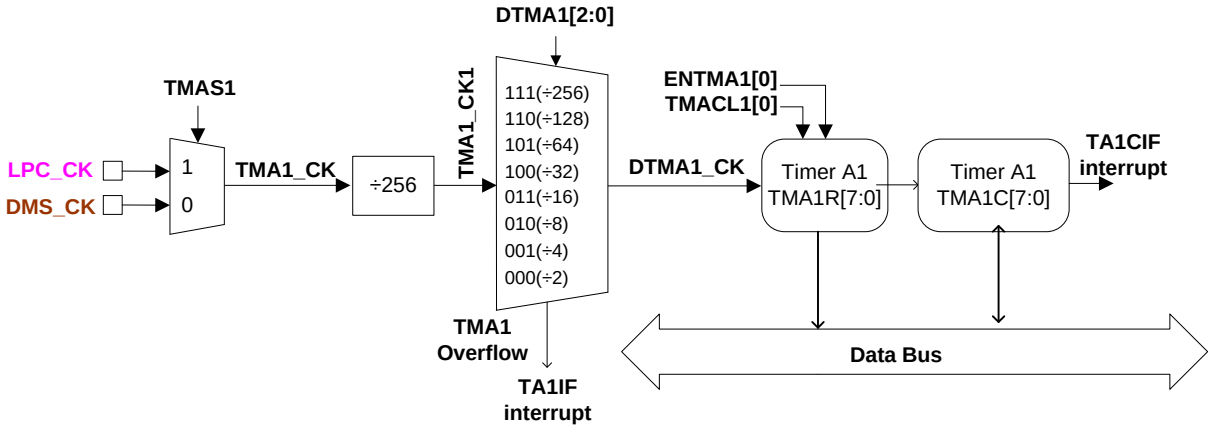


Figure 4-12 8-bit Timer A1 block diagram

4.12. LCD

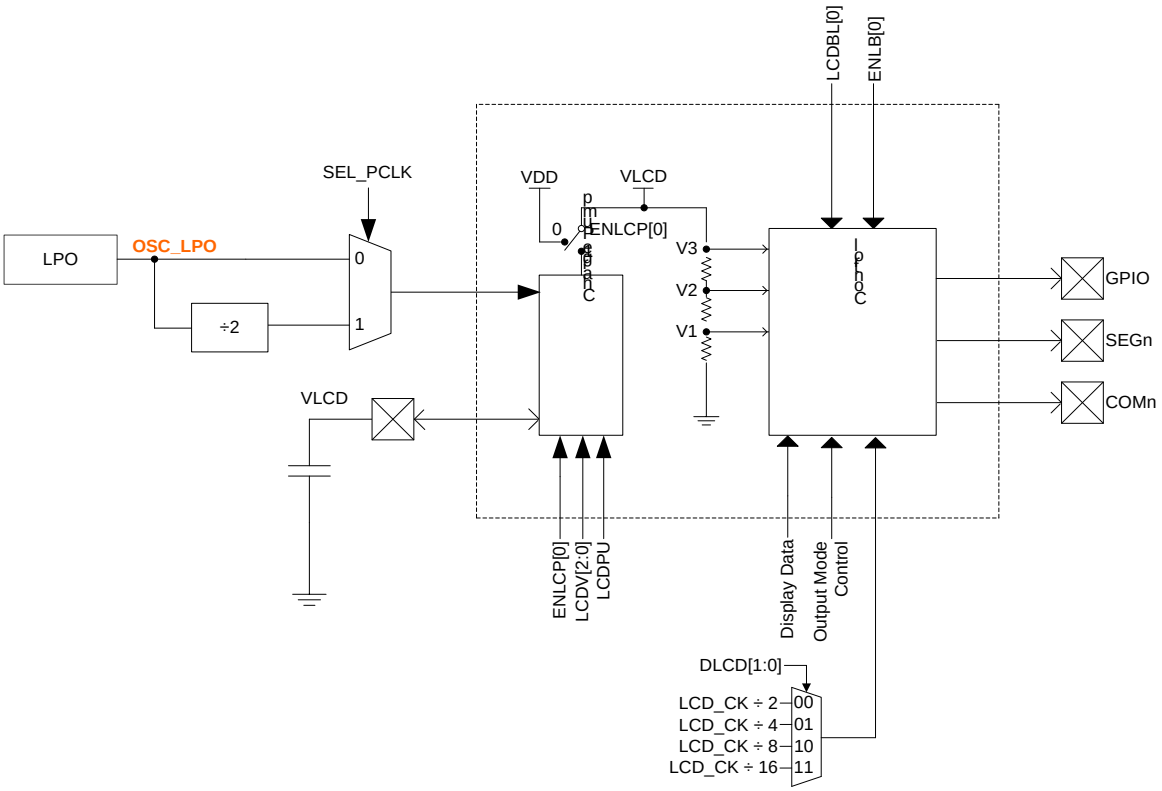


Figure 4-13 LCD block diagram

4.13. EUART

EUART TRANSMIT BLOCK DIAGRAM

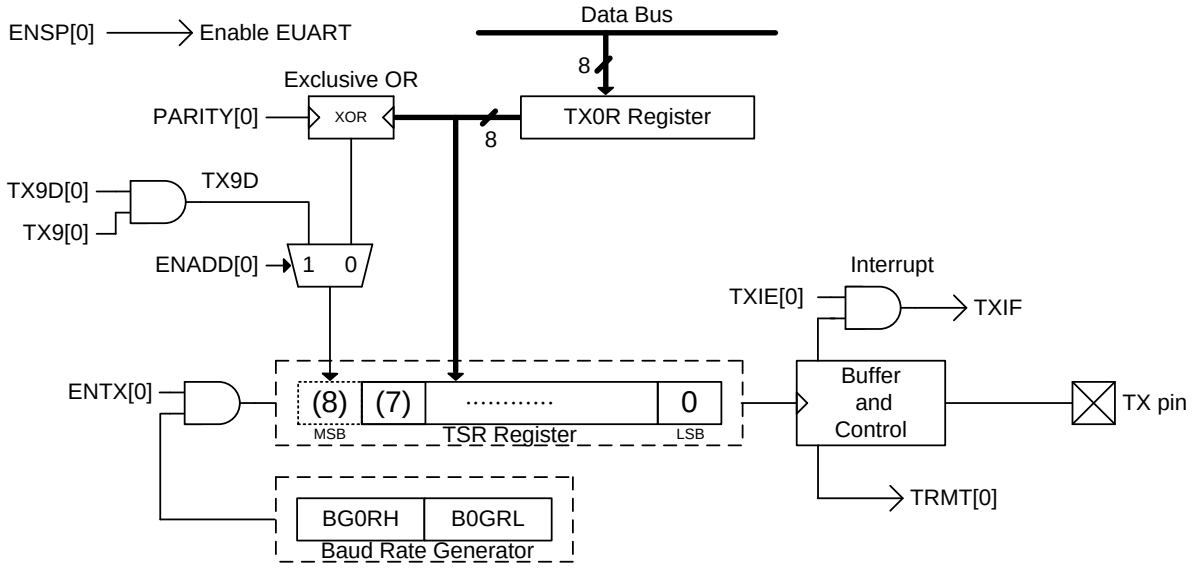
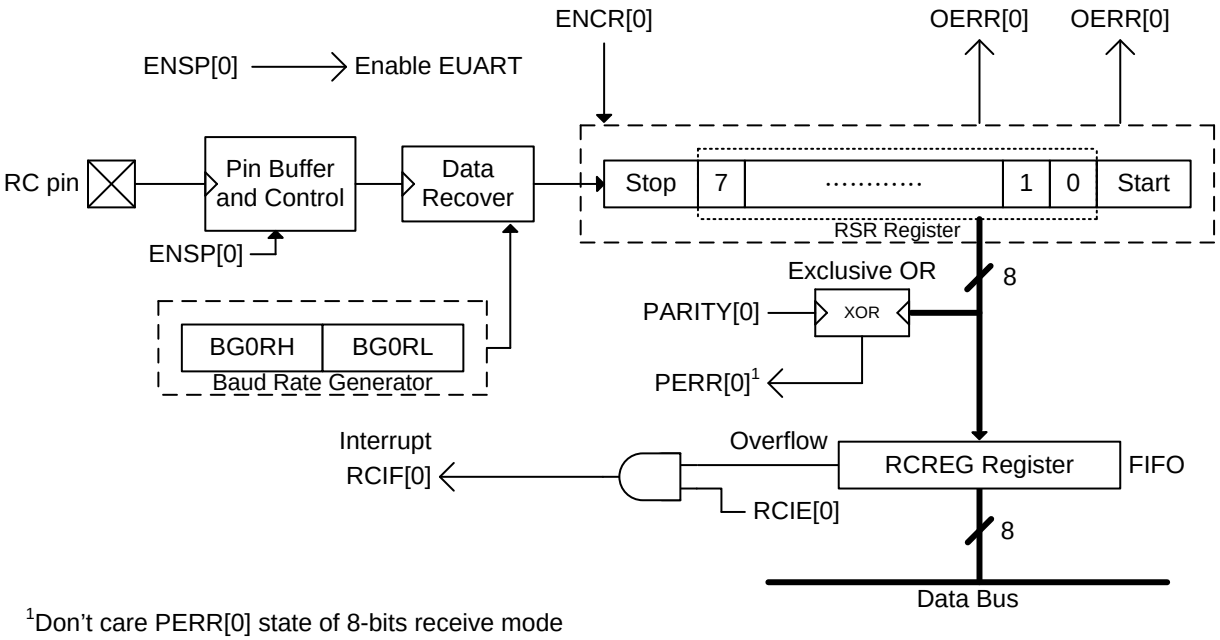


Figure 4-14 EUART transmit block diagram

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

Figure 4-15 EUART 8-bits receive block diagram

5. Register list

"-"no use,"*"read/write,"w"write,"r"read,"r0"onlyread 0,"r1"onlyread 1,"w0"onlywrite 0,"w1"omlywrite 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008h	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Fh	FSR0H	-	-	-	-	-	-	-	FSR0[8]	…. ...x	…. ...u	-,-,-,- -,-,-,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR1H	-	-	-	-	-	-	-	FSR1[8]	…. ...x	…. ...u	-,-,-,- -,-,-,*
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	-	TOS[11:8]				…. 0000	…. uuuu	-,-,-,- *,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	SKPRT[3:0]				000. 0000	u$$. $$$$	rw 0,rw 0,rw 0,- *,*,*,*
01Ah	PCLATH	-	-	-	-	PC[11:8]				…. 0000	…. 0000	-,-,-,- *,*,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Dh	TBLPTRH	-	-	-	-	TBLPTR11:8]				…. xxxx	…. uuuu	-,-,-,- *,*,*,*
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021h	PRODH	Product Register of Multiply High Byte								0001 0010	uuuu uuuu	*,*,*,*,*,*,*,*
022h	PRODL	Product Register of Multiply Low Byte								0011 0100	uuuu uuuu	*,*,*,*,*,*,*,*
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	-	-	E1IE	E0IE	0000 ..00	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	TA1IE	-	TXIE	RCIE	-	-	-	-	0.00 ..00	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	TA1CIF	ADIF	WDTIF	-	-	E1IF	E0IF	.000 ..00	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	TA1IF	-	TXIF	RCIF	-	-	-	-	0.01 ….	uuuu uuuu	*,*,*,* r,r,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Ah	BSRCN	-	-	-	-	-	-	-	BSR[0]	…. …0	…. ...u	-,-,-,- -,-,-,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	…x xxxx	...u uuuu	-,-,-,*,*,*,*,*
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	-	-	$000 $0..	uu$u u$..	rw0,rw0,rw0,rw0 rw0,rw0,-,-
02Eh	BIECN	1	-	-	ENBVD	VPPHV	ENBCP	BIEWR	BIERD	1..0 $000	1.00 $uuu	r1,-,*,* r,*,*,*
030h	BIEARL			BIE Address Register as BIEAL[5:0]						..11 1111	uuuu uuuu	*,*,*,*,*,*,*,*
031h	BIEDRH	BIE High Byte Data Register								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
032h	BIEDRL	BIE Low Byte Data Register								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
033h	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	CSFON	1000 0000	uuuu u00u	*,*,*,*,*,w r0,w r0,*
034h	OSCCN0	-	OSCS[0]	DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
035h	OSCCN1	-	-	DADC[1:0]		-	-	-	LCDS	0000 0000	uuuu uuu.	*,*,*,*,*,*,-
036h	OSCCN2	DLCD[1:0]		-	-	-	HAOM[1:0]		ENHAO	0000 0001	uuuu uu11	*,*,*,*,*,*,*,*
037h	CSFCN0	SKRST	HAOTR[6:0]							xxxx xxxx	…. ….	-,-,-,- -,-,-,-
038h	CSFCN1	ENSDRV			-	-	-	-	-	0… ….	uuuu uuuu	*,*,*,*,*,*,*,*
039h	WDTCN	ENBZ	BZS	DBZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw 1,*,*,*
03Ah	AD1H	ADC1 conversion high byte data register								0000 0000	..uu uuuu	-,-,*,*,*,*,*,*
03Bh	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Ch	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Dh	AD1CN0	ENAD1			OSR[3:0]				CMFR	0xx0 0000	uuu. uuuu	*,*,*,*,*,*,*,*
03Eh	AD1CN1	-		VREGN	PGAGN[1:0]		ADGN[2:0]			xx00 0000	u.uu uuuu	*,*,*,*,*,*,*,*
03Fh	AD1CN2	INIS1	-	-	-	DCSET[3:0]				xxx0 0000	…. uuuu	*,*,*,*,*,*,*,*
040h	AD1CN3	INP[3:0]				INN[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
041h	AD1CN4	VRH[1:0]		VRL[1:0]		INX[1:0]		VRIS	INIS	0000 00xx	uuuu uuuu	*,*,*,*,*,*,*,*
042h	AD1CN5	ENACM	-	VCMS	LDOPL	-	-	ENTPS	-	0x00 ..0.	uuuu ..u.	*,*,*,*,*,*,*,*
043h	LVDCN			PWRS	LVDS[3:0]				LVDO	xx00 0000	..uu uuuu	*,*,*,*,*,*,*,*

Table 5-1 Data memory list (1)

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
044h	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-	-	0000 00..	u0uu uuu.	*,rw1,*,* *,*,*,-
045h	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
046h	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
047h	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
048h	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
049h	PT1DA	-	-	-	-	-	DA1.2	-	-	.... .1..	uuuu uuuu	*,*,*,*,*,*,*,*
04Ah	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
04Bh	PT1M1	-	-	-	-	INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Ch	PT2	-	-	-	-	-	-	PT2.1	PT2.0	xx	uuuu uuuu	*,*,*,*,*,*,*,*
04Dh	TRISC2	-	-	-	-	-	-	TC2.1	TC2.0	00	uuuu uuuu	*,*,*,*,*,*,*,*
04Fh	PT2PU	-	-	-	-	-	-	PU2.1	PU2.0	11	uuuu uuuu	*,*,*,*,*,*,*,*
050h	PT8	-	-	-	-	-	-	PT8.1	PT8.0	00	uuuu uuuu	*,*,*,*,*,*,*,*
051h	TRISC8	-	-	-	-	-	-	TC8.1	TC8.0	00	uuuu uuuu	*,*,*,*,*,*,*,*
053h	PT8PU	-	-	-	-	-	-	PU8.1	PU8.0	00	uuuu uuuu	*,*,*,*,*,*,*,*
054h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	000x x..0	uuuu u..u	*,*,*,* *,-,-,*
055h	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.x00 0110	.uuu uuuu	-,r,r,r r,r,r,rw0
056h	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD	 0000	.... uuuu	-,-,-,- *,*,*,*'
057h	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,* *,*,*,*
058h	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
059h	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
05Ah	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05Bh	LCDCN1	ENLCP	LCDV[2:0]			ENLB	SELPCLK	-	LCDPU	0000 00..	uuuu uu.u	*,*,*,*,*,*,*,*
05Ch	LCDCN2	-	-	-	-	-	-	LCDBL	LCI	00	.... ..uu	*,*,*,*,*,*,*,*
05Dh	LCDCN3	SCM3[1:0]		SCM2[1:0]		SCM1[1:0]		SCM0[1:0]		1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
05Eh	LCDCN4	-	-	-	-	-	-	SSG15	SSG14	00	uuuu uuuu	*,*,*,*,*,*,*,*
05Fh	LCD0	LCD SEG3[4:7] data				LCD SEG2[3:0] data				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
060h	LCD1	LCD SEG5[4:7] data				LCD SEG4[3:0] data				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
061h	LCD2	LCD SEG7[4:7] data				LCD SEG6[3:0] data				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
062h	LCD3	LCD SEG9[4:7] data				LCD SEG8[3:0] data				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
063h	LCD4	LCD SEG11[4:7] data				LCD SEG10[3:0] data				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
064h	LCD5	LCD SEG13[4:7] data				LCD SEG12[3:0] data				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
065h	LCD6	LCD SEG15[4:7] data				LCD SEG14[3:0] data				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
080h ~ 17Fh		SRAM as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

Table 5-2 Data memory list (2)

6. Electrical Characteristics

Absolute Maximum Ratings :

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD to VSS . . . . −0.2 V to 6.0 V

Voltage applied to any pin . . . . −0.2 V to VDD + 0.3 V

Voltage applied to RST/VPP pin . . . . −0.2 V to 8.75 V

Diode current at any device terminal . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . −55℃ to 125℃

(programmed device) . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any I/O pin. 20mA

6.1. Recommended operating conditions

TA = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
VDD	Supply Voltage	All digital peripherals and CPU VDD = 2.0V~5.5V, Frequency<=9.6Mhz, VDD = 3.6V~5.5V, Frequency<=16Mhz,	2.2		5.5	V
VDDA	Supply Voltage	Analog peripherals	2.4		4.5	
VSS	Supply Voltage		0		0	

6.2. Internal RC Oscillator

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00	-20%	1.843	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=01	-20%	3.686	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=11	-20%	7.834	+20%	MHz
		After Frequency Trim by Writer(guarantee 3.686M)	-2%		+2%	MHz
LPO	Low Power Oscillator frequency	VDD supply voltage be enable LPO	-20%	14.5	+20%	KHz

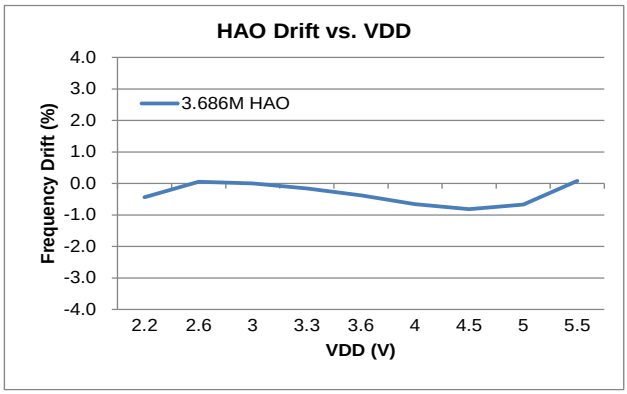


Figure 6.2-1 HAO vs. VDD

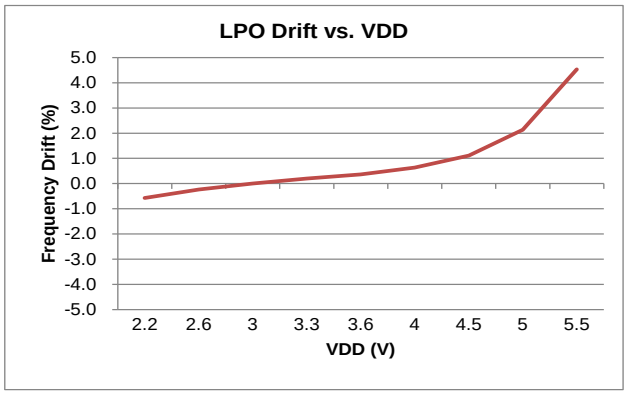


Figure 6.2-2 LPO vs. VDD

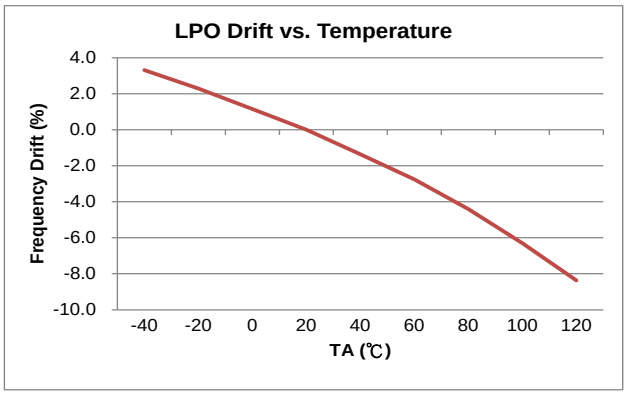


Figure 6.2-3 LPO vs. Temperature

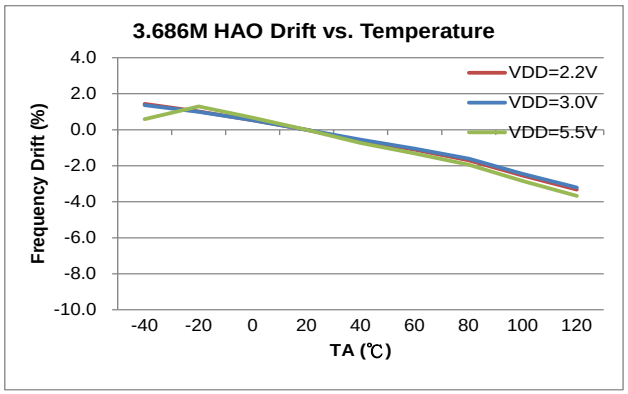


Figure 6.2-4 HAO(3.686MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

TA = 25℃,VDD = 3.0V,OSC_LPO = 14.5KHz, , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =3.686MHz, CPU_CK = 3.686MHz		320	650	uA
I_{AM5}	Active mode 5	OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz/2		250	500	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO		2	5	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state		1.1	2.5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state		0.4	1.0	uA

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

TA = 25℃,VDD = 5.5V,OSC_LPO = 14.5KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =3.686MHz, CPU_CK = 3.686MHz		720	1200	uA
I_{AM5}	Active mode 5	OSC_CY = off, OSC_HAO = 3.686MHz, CPU_CK = 3.686MHz/2		600	900	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO		4	10	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state		2.5	5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state		0.4	2	uA

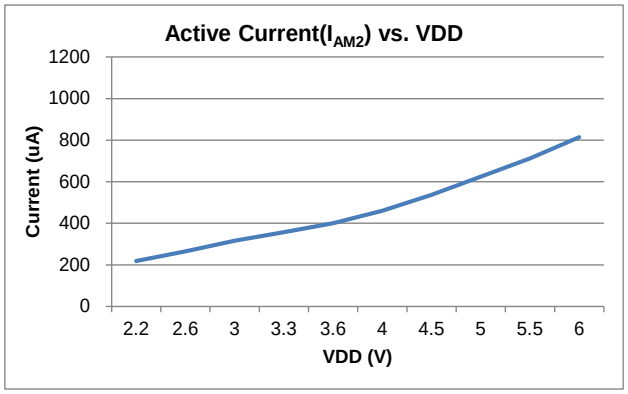


Figure 6.3-1 I_{AM2} vs. VDD

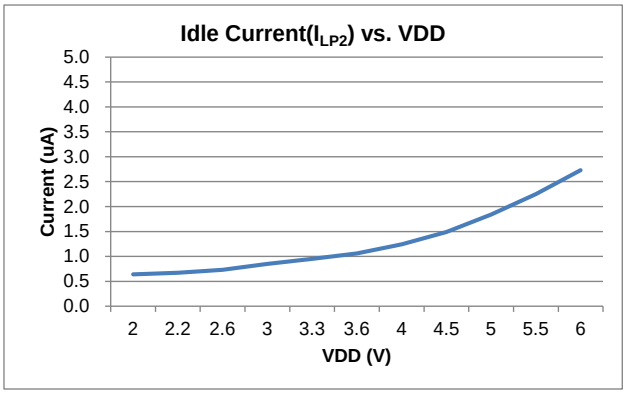


Figure 6.3-2 I_{LP2} vs. VDD

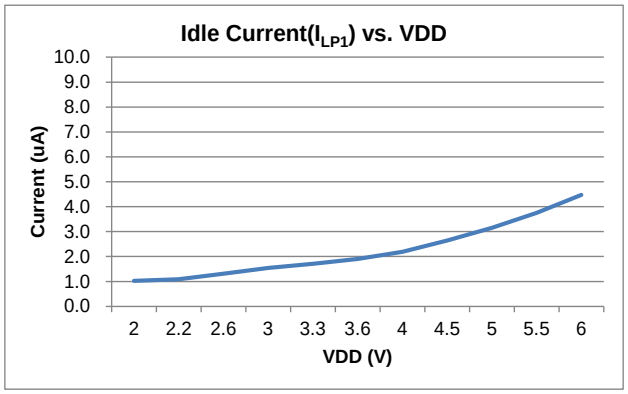


Figure 6.3-3 I_{LP1} vs. VDD

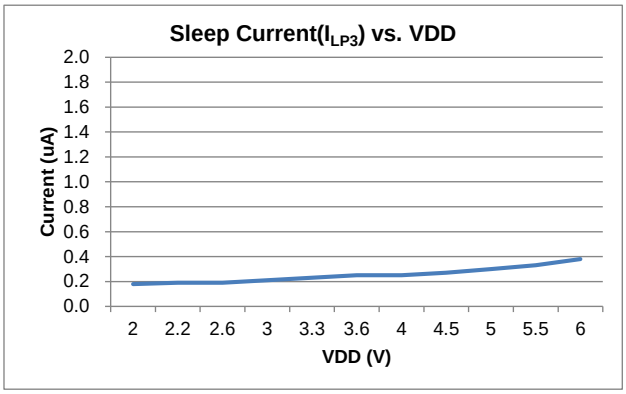


Figure 6.3-4 I_{LP3} vs. VDD

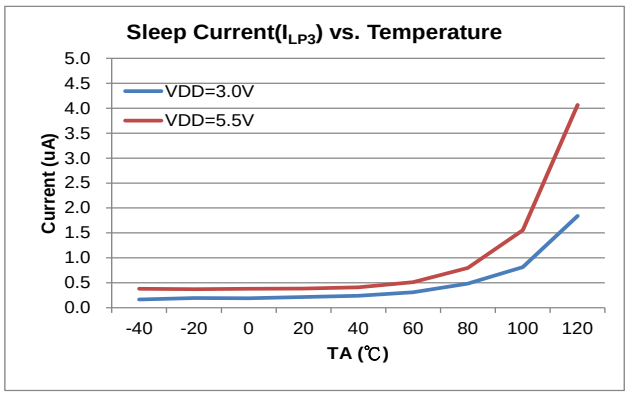


Figure 6.3-5 I_{LP3} vs. Temperature

6.4. Port 1~2 & 8

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*VDD	V
V_{IL}	Low-Level input voltage		0.3*VDD			
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*VDD		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance(PT1、PT2)			60		kΩ
	Port pull high resistance(PT8)			110		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD<4V, I_{OH}=3mA,	VDD -0.3			V
		VDD>=4V, I_{OH}=5mA,	VDD -0.3			
V_{OL}	Low-level output voltage	VDD<4V, I_{OL}=-3mA			VSS +0.3	
		VDD>=4V, I_{OL}=-5mA			VSS +0.3	

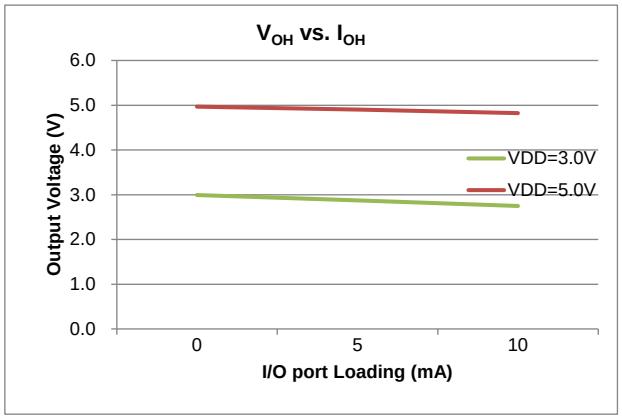


Figure 6.4-1 V_{OH} vs. I_{OH}

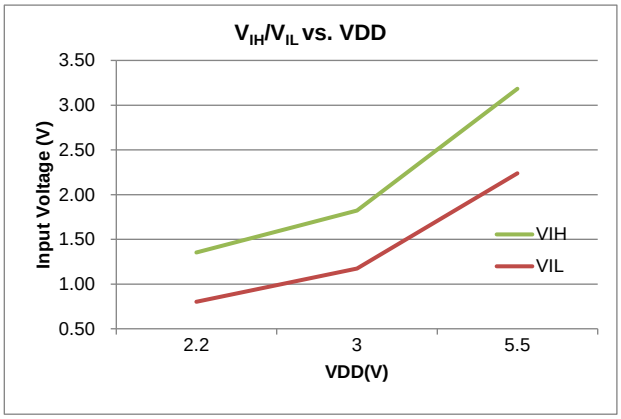


Figure 6.4-2 V_{IH}/V_{IL} vs. VDD

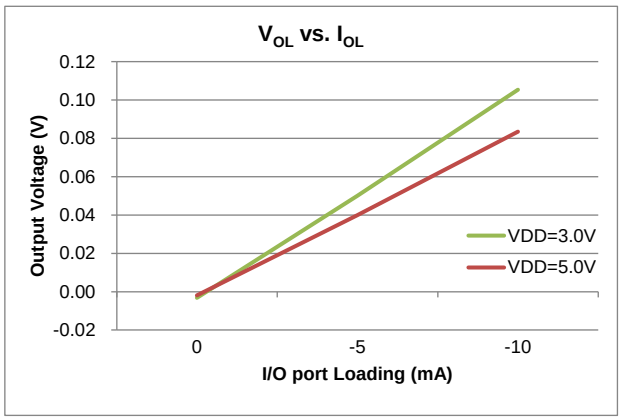


Figure 6.4-3 V_{OL} vs. I_{OL}

6.5. Port1.6~Port1.7

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*VDD	V
V_{IL}	Low-Level input voltage		0.3*VDD			
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*VDD		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD<4V, I_{OH}=10mA,	VDD -0.4			V
		VDD>=4V, I_{OH}=15mA,	VDD -0.4			
V_{OL}	Low-level output voltage	VDD<4V, I_{OL}=-10mA			VSS +0.3	
		VDD>=4V, I_{OL}=-15mA			VSS +0.3	

6.6. Reset(Brownout, Low Voltage Detect)

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR1}		2			us
	VDD Start Voltage to accepted reset internally (L➔H),V_{HYS1}		1.6	1.85	2.1	V
	BOR1 current, I_{BOR1}			0.4		uA
	Temperature Drift			5		%
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset voltage			1.1		V
	Reset release voltage			2		V
LVD	Operation current, I_{LVD}			10		uA
	External input voltage to compare reference voltage		1.15	1.2	1.25	V
	Compare reference voltage temperature drift	TA = -40℃ ~ 85 ℃		50		ppm/℃
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1110b		-0.1V	4.0	+0.1V	V
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1101b			3.6		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1100b			3.3		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1011b			3.0		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1010b			2.9		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1001b			2.8		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1000b			2.7		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0111b			2.6		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0110b			2.5		

	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0101b		2.4		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0100b		2.3		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0011b		2.2		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0010b		2.1		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0001b		2.0		

BOR1：Brownout Reset 1

LVD：Low Voltage Detect

RST：External Reset pin

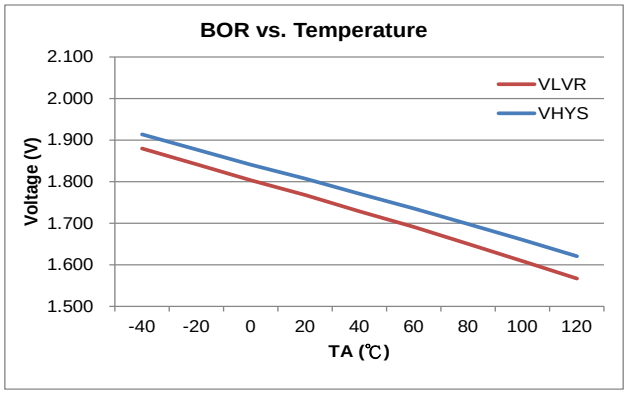


Figure 6.6-1 BOR vs. Temperature

6.7. Power System

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.25V	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=100b		3.6		V
	Dropout voltage	I_L = 10mA	LDOC [2:0]=000b		500		mV
	Temperature drift	LDOC [2:0]=000b I_L = 0.1mA	TA=-40℃~85℃		50		PPM/℃
	VDD Voltage drift	LDOC [2:0]=000b	VDD=2.2V~5.5V		±0.2		%/V
VDDA/2	operation current, I_{ACM}	ENADC[0]=1b,	ENACM [0]=1b		50		uA
	Internal Analog Common Mode Voltage ,V_{ACM}=VDDA/2		I_L = 0uA		VDDA/2		V
	Temperature drift	ENADC[0]=1b,	TA=-40℃~85℃, ENACM [0]=1b		50		PPM/℃
V12	operation current, I_{V12}	ENADC[0]=1b,	ENV12 [0]=1b		50		uA

	Internal Analog Common Mode Voltage ,V_{ACM}=V12		I_L = 0uA	1.1	1.2	1.3	V
	Temperature drift	ENADC[0]=1b,	TA=-40℃~85℃, ENV12 [0]=1b		50		PPM/℃
VDDA：Adjust Voltage Regulator, ACM：Internal Analog Common Mode Voltage VDDA/2 (No voltage output)							

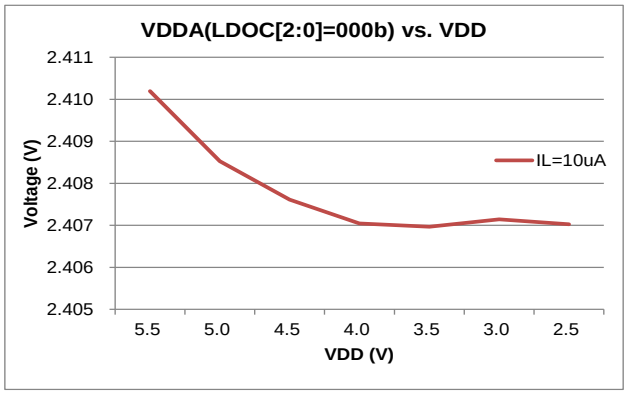


Figure 6.7-1 VDDA(000b) vs. VDD

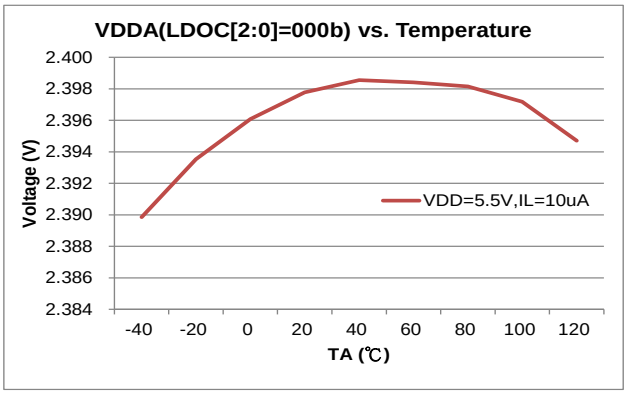


Figure 6.7-2 VDDA(000b) vs. Temperature

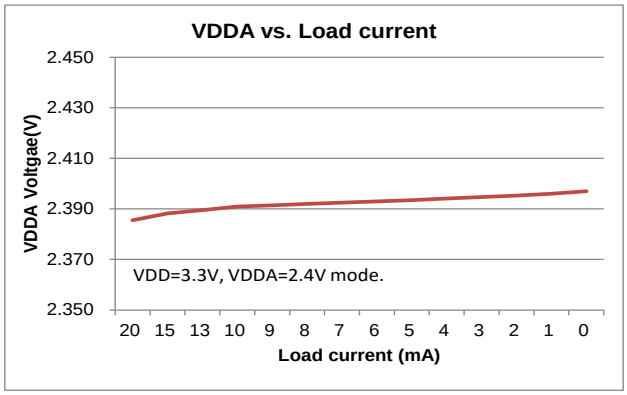


Figure 6.7-3 VDDA vs. Load current

6.8. LCD

TA = 25℃,VDD = 3.3V, CVLCD =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current with output buffer.(all segment turn on, No load)	ENLCP[0]=1	VDD = 3.0V		5		uA
VLCD	Supply Voltage at VLCD pin	ENLCP [0]=0		2.4		5	V
	Embedded Charge Pump output voltage at VLCD pin	VDD = 3.3V, ENLCP [0]=1 CVLCD =4.7uF	LCDV[2:0]=111b	-10%	2.45	+10%	V
			LCDV[2:0]=110b	-10%	2.70	+10%	
			LCDV[2:0]=101b	-10%	2.85	+10%	
			LCDV[2:0]=100b	-10%	3.10	+10%	

			LCDV[2:0]=011b	-10%	3.30	+10%
			LCDV[2:0]=010b	-10%	4.10	+10%
			LCDV[2:0]=001b (VDD>2.4V mode)	-10%	4.55	+10%
			LCDV[2:0]=000b (VDD>2.75V)	-10%	5.1	+10%
	VDD Voltage drift	ENLCP [0]=1, CVLCD =4.7uF, LCDV[2:0]>010b,VDD=2.2V~ 5.5V; LCDV[2:0]=001b,VDD>2.4V; LCDV[2:0]=000b,VDD>2.75V;		4		%/V
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V		10		kΩ

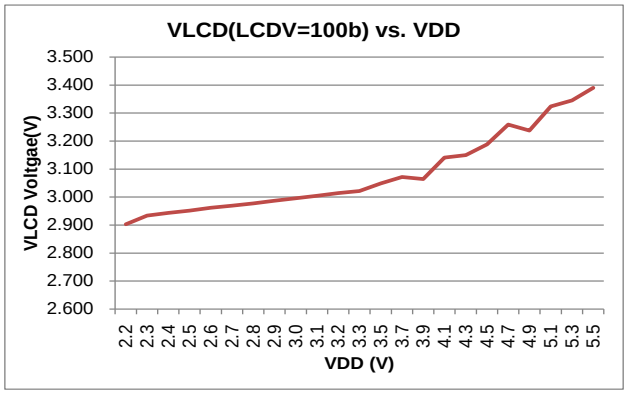


Figure6.8-1 VLCD(LCDV=100b) vs. VDD

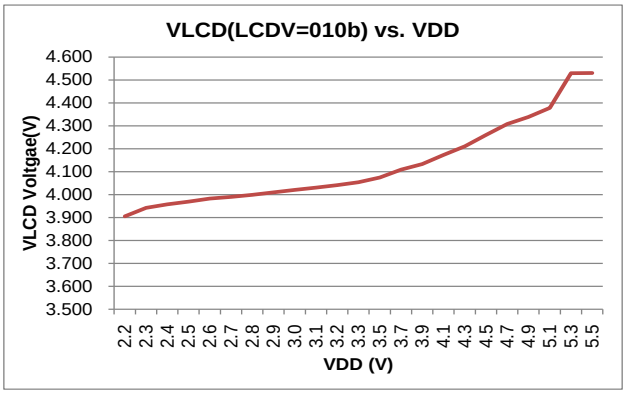


Figure6.8-2 VLCD(LCDV=010b) vs. VDD

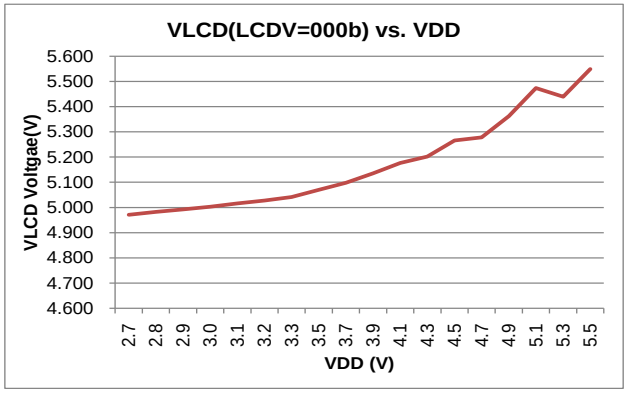


Figure6.8-3 VLCD(LCDV=000b) vs. VDD

6.9. ΣΔADC, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENLDO[0]=0		2.4		5.5	V
f_{SD18}	Modulator sample frequency, ADC_CK			230	921		KHz
	Over Sample Ratio, OSR			64		65536	
I_{SD18}	Operation supply current without PGA	ENAD1 [0]=1	GAIN =16, ADC_CK=921KHz		260		uA

6.9.1. PGA, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENLDO [0]=0		2.4		5.5	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<11>			450		uA
G_{PGA}	Gain temperature drift	TA = -40℃~ 85℃	GAIN=128		15		ppm/℃

6.9.2. ΣΔADC,performance

TA = 25℃,VDD = 3.6V, VDDA=2.4V,V_{VR}= AI2(short to VDDA)/2

GAIN=16 with PGA=8,f_{SD18}=921KHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,VVR= AI2/2, ΔSI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes3	ADC_CK=921KHz,OSR[3:0]=0000b		23			Bits
G_{SD18}	Temperature drift Gain x16	TA = -40℃~ 85℃			10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=1.2V DCSET[3:0]=<0000> *ΔAI is external short	Gain=2			1	%FSR
	Offset temperature drift with chopper without PGA		GAIN=1		2		uV/℃
			GAIN=2		1		
			GAIN=4		0.5		
			GAIN=16		0.15		
	Offset temperature drift with chopper		GAIN=128		0.02		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}= 1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
			V_{SI}=0V,		75		dB

			GAIN=16		
PSRR	DC power supply rejection	VDDA=3.0V Δ_{VDDA}=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI}-=1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16 PGA=8		dB

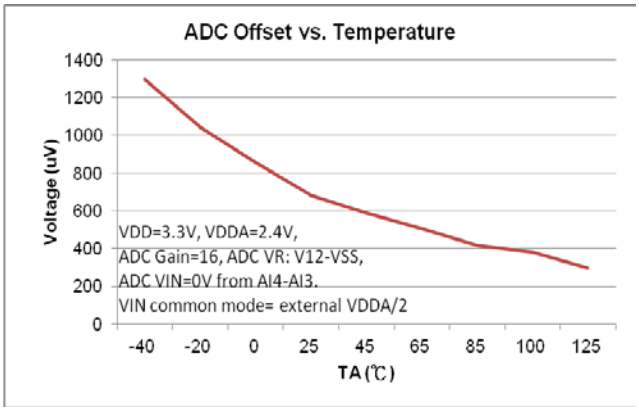


Figure 6.9-1 ADC Offset drift with Temperature

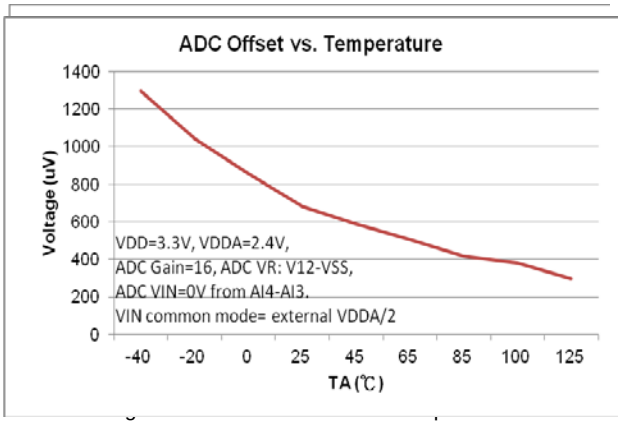


Figure 6.9-1 ADC Offset drift with Temperature

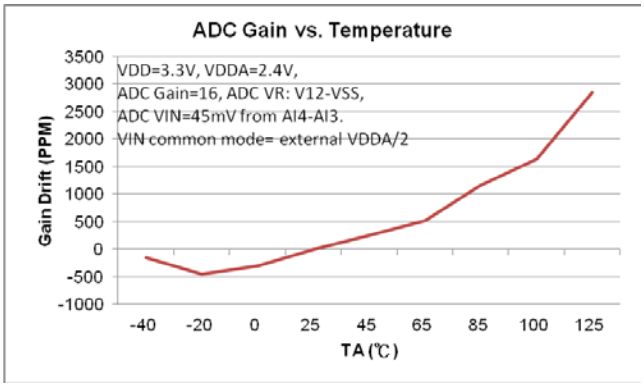


Figure 6.9-3 ADC Gain drift with Temperature

6.9.3. ΣΔADC Noise Performance

Provide important input noise specifications for the ΣΔ ADC. Table 6.9-1 below shows the typical noise specification table and the relationship between Gain, Output rate, and differential maximum input voltage., sampling 1024 datas.

ENOB(RMS) with OSR/GAIN at A/D Clock=921KHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V															
Max. Vin(mV) =0.9VREF(1)	OSR					64	128	256	512	1024	2048	4096	8196	16384	32768	65536
	Output rate(Hz)					15625	7813	3906	1953	977	488	244	122	61	28	14
	Gain	=	PGAGN	x	ADGN											
±1080	1	=	off	x	1	14.05	15.24	15.8	16.24	16.65	17.03	17.52	18.09	18.56	18.98	19.52
±270	4	=	off	x	4	14.09	15.14	15.59	16.02	16.6	16.87	17.31	17.82	18.29	18.74	19.1
±68	16	=	off	x	16	11.95	14.88	15.39	15.94	16.47	16.81	17.21	17.73	18.13	18.6	19.02
±135	8	=	8	x	1	13.67	15.14	15.6	16.04	16.47	16.88	17.35	17.87	18.42	18.87	19.34
±8.5	128	=	8	x	16	11.61	12.63	13.13	13.55	14.11	14.47	14.92	15.36	15.96	16.46	16.92

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

RMS(uV) with OSR/GAIN at A/D Clock=921KHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V															
Max. Vin(mV) =0.9VREF(1)	OSR					64	128	256	512	1024	2048	4096	8196	16384	32768	65536
	Output rate(Hz)					15625	7813	3906	1953	977	488	244	122	61	28	14
	Gain	=	PGAGN	x	ADGN											
±1080	1	=	off	x	1	142.74	62.37	42.43	31.17	23.40	18.04	12.83	8.65	6.22	4.65	3.20
±270	4	=	off	x	4	34.62	16.74	12.22	9.06	6.06	5.03	3.71	2.61	1.88	1.38	1.08
±68	16	=	off	x	16	38.02	4.99	3.52	2.41	1.66	1.32	0.99	0.69	0.53	0.38	0.28
±135	8	=	8	x	1	23.17	8.36	6.06	4.47	3.33	2.50	1.80	1.26	0.86	0.63	0.46
±8.5	128	=	8	x	16	6.05	2.97	2.11	1.58	1.07	0.83	0.61	0.45	0.30	0.21	0.15

Table6.9-1(a) ΣΔADC ENOB and RMS Noise Table at VDDA=2.4V

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V at High Accuracy Mode															
Max. Vin(mV) =0.9VREF(1)	OSR					64	128	256	512	1024	2048	4096	8196	16384	32768	65536
	Output rate(Hz)					7813	3906	1953	977	488	244	122	61	31	14	7
	Gain	=	PGAGN	x	ADGN											
±1080	1	=	off	x	1	14.95	15.76	16.25	16.8	17.13	17.51	17.99	18.51	19	19.61	20.04
±270	4	=	off	x	4	14.94	15.64	16.07	16.52	17.02	17.34	17.83	18.43	18.92	19.39	19.82
±68	16	=	off	x	16	14.75	15.44	15.89	16.46	16.96	17.32	17.79	18.3	18.81	19.22	19.62
±135	8	=	8	x	1	14.94	15.59	16.1	16.59	17.06	17.37	17.89	18.31	18.92	19.37	19.81
±8.5	128	=	8	x	16	12.57	12.89	13.53	13.94	14.48	14.68	15.25	15.85	16.38	16.98	17.49

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS)

RMS Noise(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=1.2V at High Accuracy Mode															
Max. Vin(mV) =0.9VREF(1)	OSR					64	128	256	512	1024	2048	4096	8196	16384	32768	65536
	Output rate(Hz)					7813	3906	1953	977	488	244	122	61	31	14	7
	Gain	=	PGAGN	x	ADGN											
±1080	1	=	off	x	1	76.21	43.47	30.92	21.16	16.80	12.95	9.29	6.45	4.61	3.01	2.24
±270	4	=	off	x	4	19.21	11.84	8.76	6.40	4.53	3.63	2.59	1.71	1.22	0.88	0.65
±68	16	=	off	x	16	5.46	3.39	2.48	1.68	1.18	0.92	0.67	0.47	0.33	0.25	0.19
±135	8	=	8	x	1	9.62	6.11	4.30	3.06	2.20	1.78	1.24	0.93	0.61	0.44	0.33
±8.5	128	=	8	x	16	3.11	2.49	1.59	1.20	0.83	0.72	0.48	0.32	0.22	0.15	0.10

Table6.9-1(b) High Accuracy Mode, ΣΔADC ENOB and RMS Noise Table at VDDA=2.4V

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \ln\left(\frac{FSR}{RMS\ Noise}\right) \Big/ \ln(2)$$

$$RMS\ Noise = \left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right) \Big/ 2^{23}$$

$$Where\ FSR\ (Full\text{-}Scale\ Range) = 2 \times VREF/Gain.$$

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$

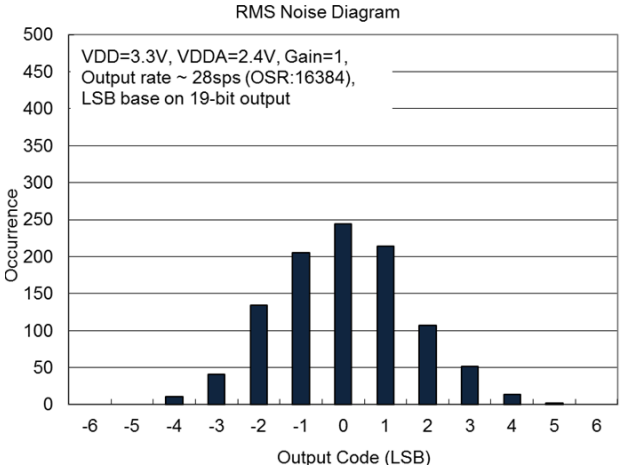


Figure 6.9-4 RMS Noise Diagram

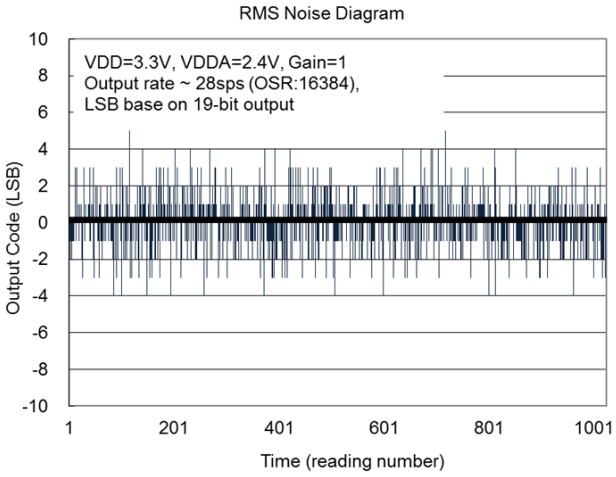


Figure 6.9-5 Output Code Diagram

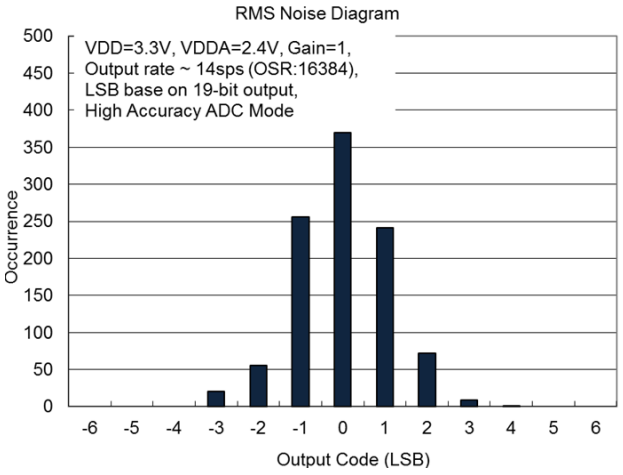


Figure 6.9-6 RMS Noise Diagram

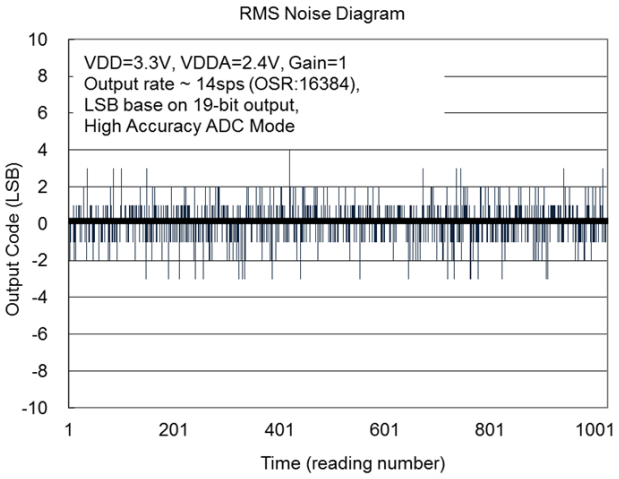


Figure 6.9-7 Output Code Diagram

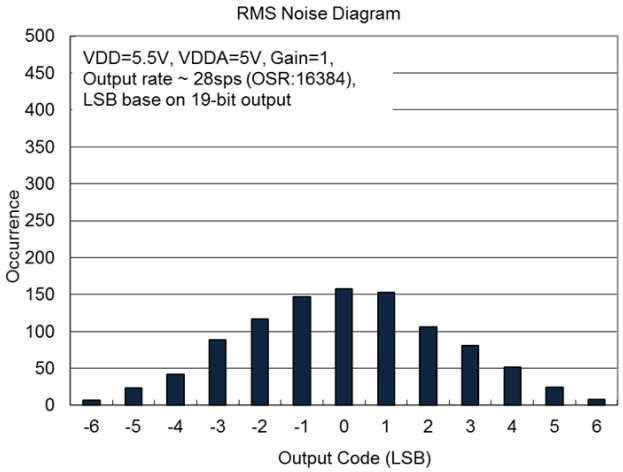


Figure 6.9-8 RMS Noise Diagram

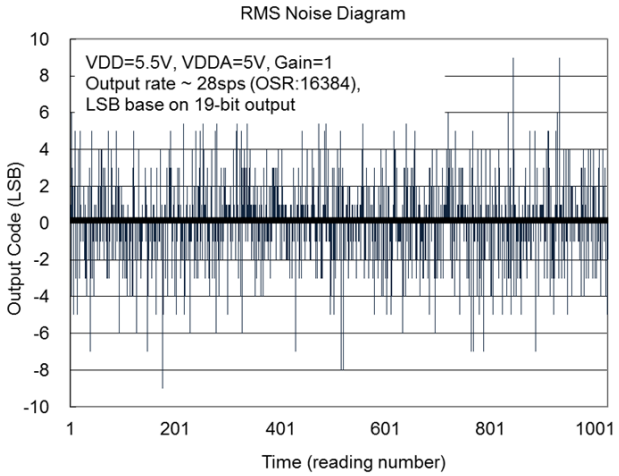


Figure 6.9-9 Output Code Diagram

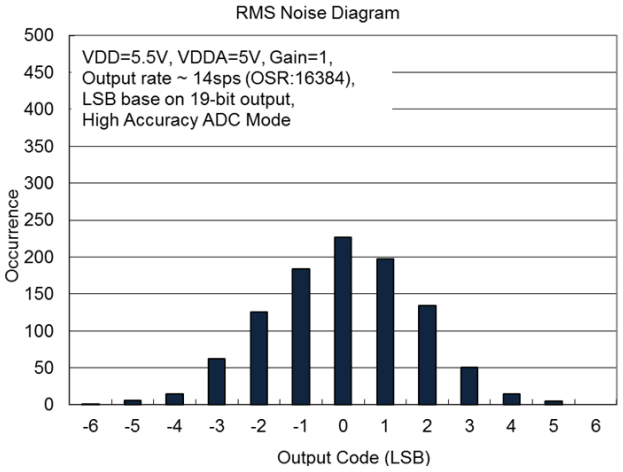


Figure 6.9-10 RMS Noise Diagram

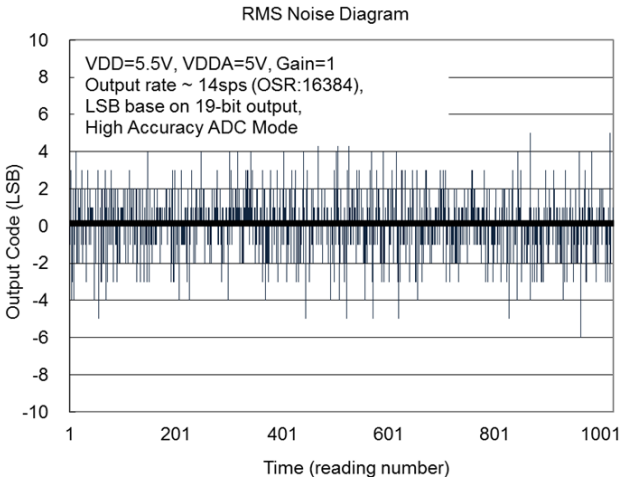


Figure 6.9-11 Output Code Diagram

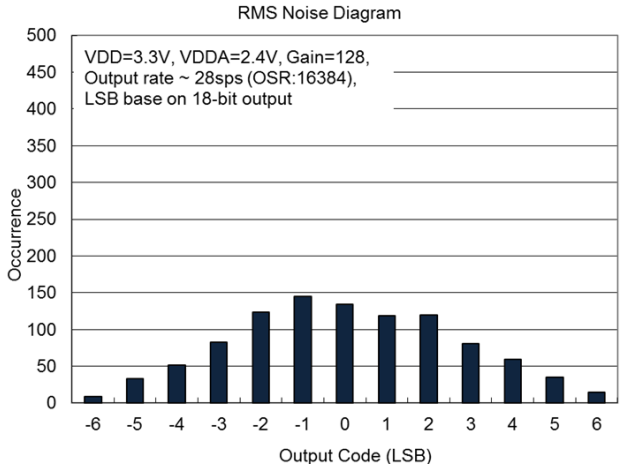


Figure 6.9-12 RMS Noise Diagram

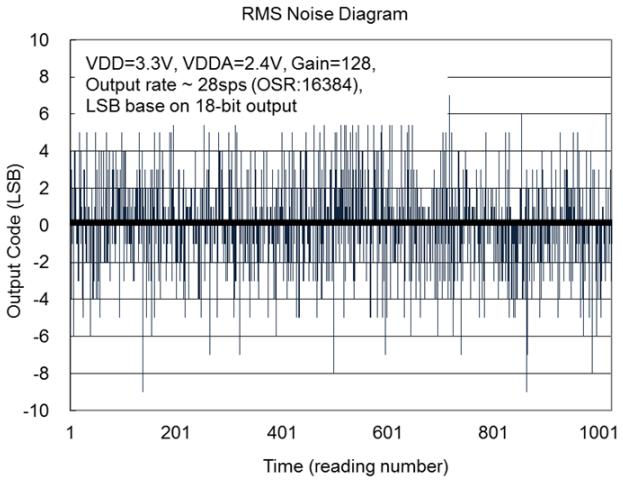


Figure 6.9-13 Output Code Diagram

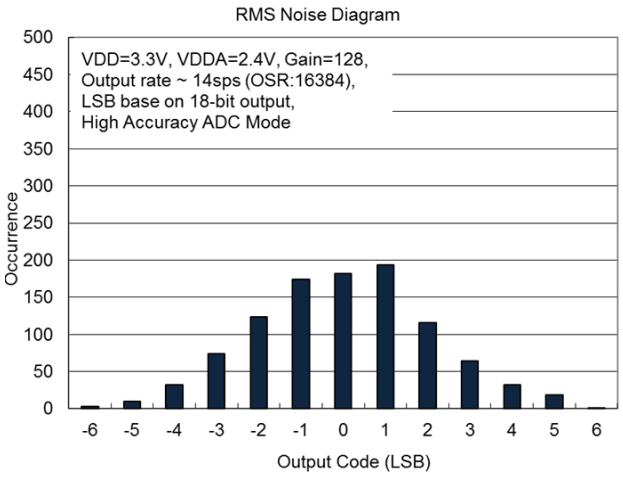


Figure 6.9-14 RMS Noise Diagram

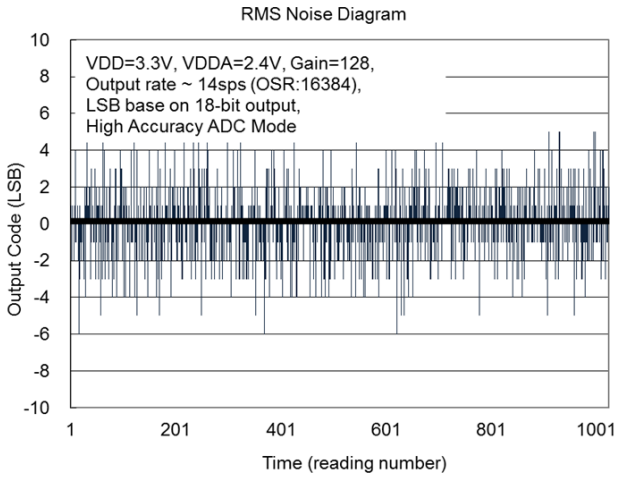


Figure 6.9-15 Output Code Diagram

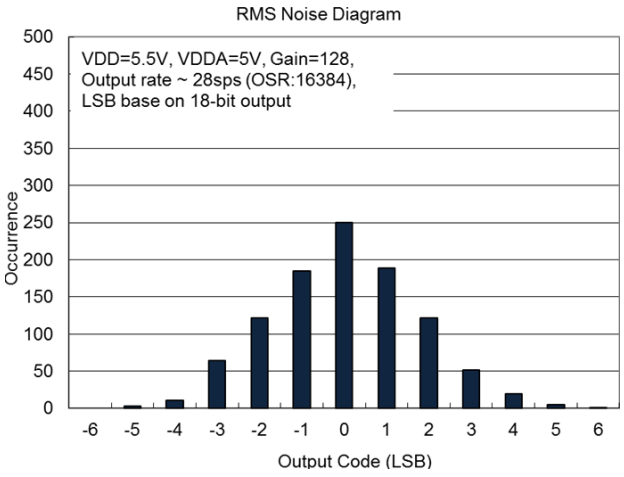


Figure 6.9-16 RMS Noise Diagram

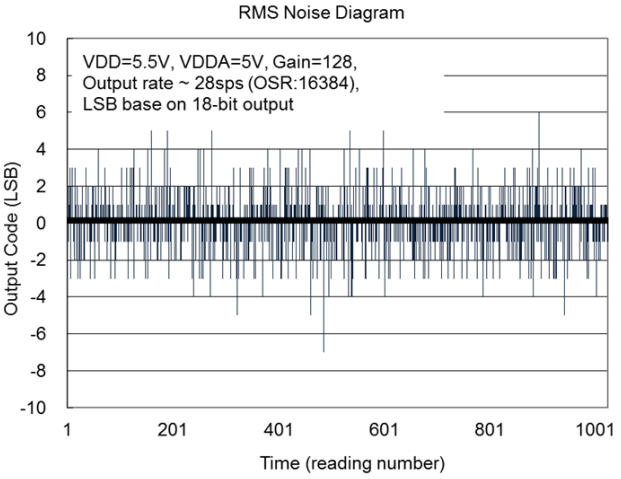


Figure 6.9-17 Output Code Diagram

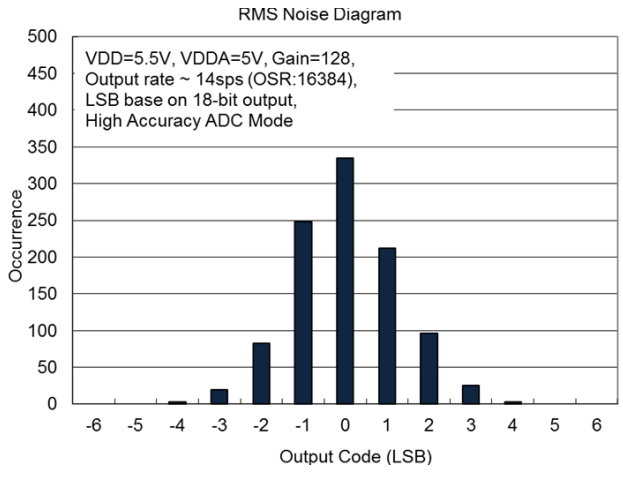


Figure 6.9-18 RMS Noise Diagram

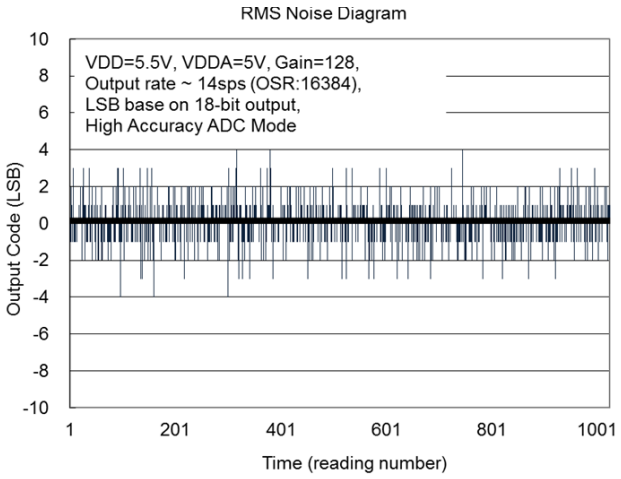


Figure 6.9-19 Output Code Diagram

6.9.4. ΣΔADC, Temperature Sensor

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			1.7		mV/℃
KT	Absolute Temperature Scale 0°K			-279		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

Figure 6.9-20 ADC Temperature Error

6.10. Build-In EPROM(BIE)

TA = 25℃,VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage at VPP PIN			8.5	8.75	V
I_{BIE}	Operation supply current			3		mA
V_{SS}	Supply Voltage			0		V
When connecting to the external VBIE power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.						

6.11. Build-In EPROM(BIE) Low voltage control circuit

TA = 25℃,VDD = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		2.75		5.5	V
V_{SS}	Supply Voltage			0		V
When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external VBIE power source.						

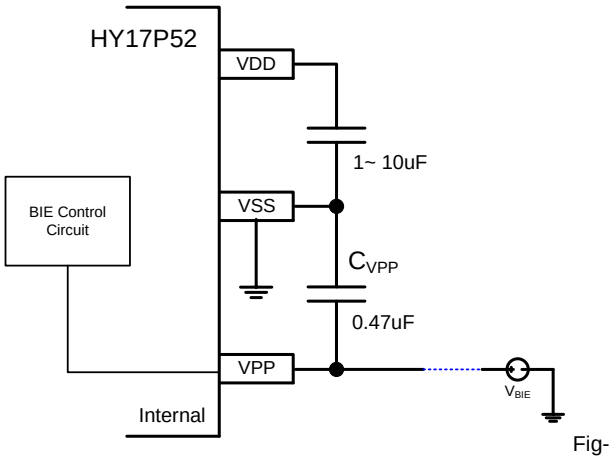


Figure 6.11-1 BIE typical application circuit

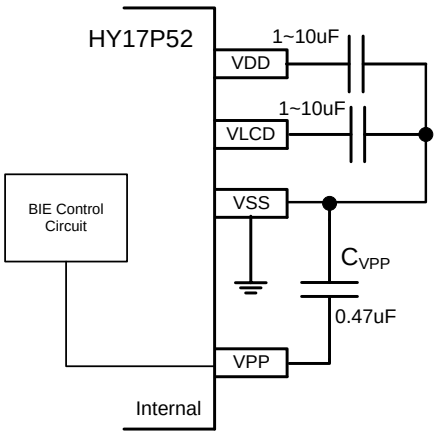


Figure 6.11-2 Use low voltage control circuit

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY17P52-D000	Die	-	D	000	000	-	250	Green[4]	-
HY17P52-L048	LQFP	48	L	048	000	Tray	250	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code (Blank Code/ Standard/Customized Programming Code)**

Ex: You request blank code in Die package. The device No. will be HY17P52-D000

Ex: Your customized programming code is 008 and you require products in Die package. The device No. will be HY17P52-D000-008.

Ex: You request blank code in LQFP48 package. The device No. will be HY17P52-L048, and please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in LQFP48 package. The device No. will be HY17P52-L048-009. and please clearly indicate the shipment packing type when placing orders.

[2] Code

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] MSL:

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

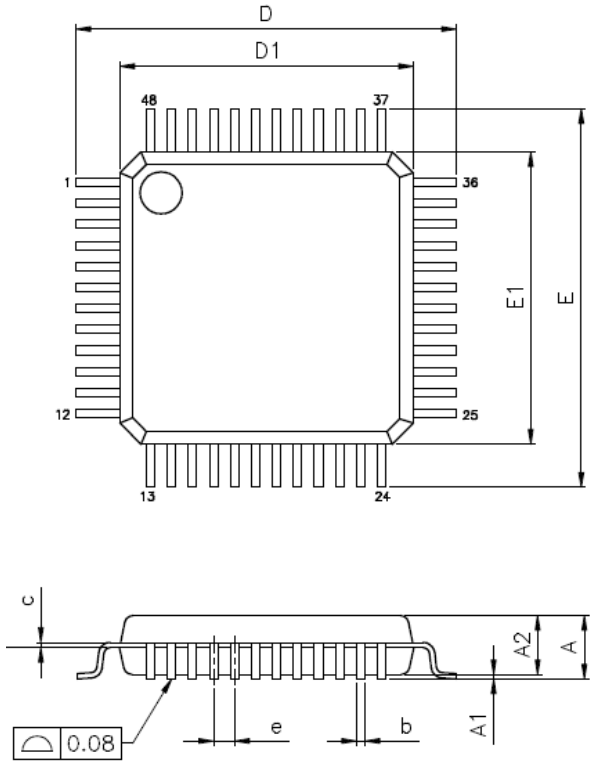
[4] Green (RoHS & no Cl/Br):

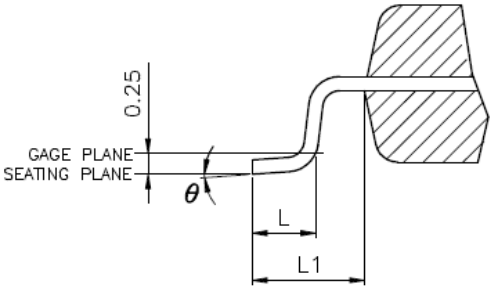
HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

8. Package Information

8.1. LQFP48(L048)

8.1.1. Package Dimensions LQFP48(7x7)





SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:
1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

9. Revision Record

Major differences are stated thereinafter.

Version	Page	Date	Revision Summary
V03	All	2022/08/27	First edition