HY17P56
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller

Embedded 4x20 LCD Driver

18-Bit ΣΔADC

Table of Contents

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4、 请注意输入电压、输出电压、负载电流的使用条件，使 IC 内的功耗不超过封装的容许功耗。对于客户在超出说明书中规定额定值使用产品，即使是瞬间的使用，由此所造成的损失，本公司不承担任何责任。

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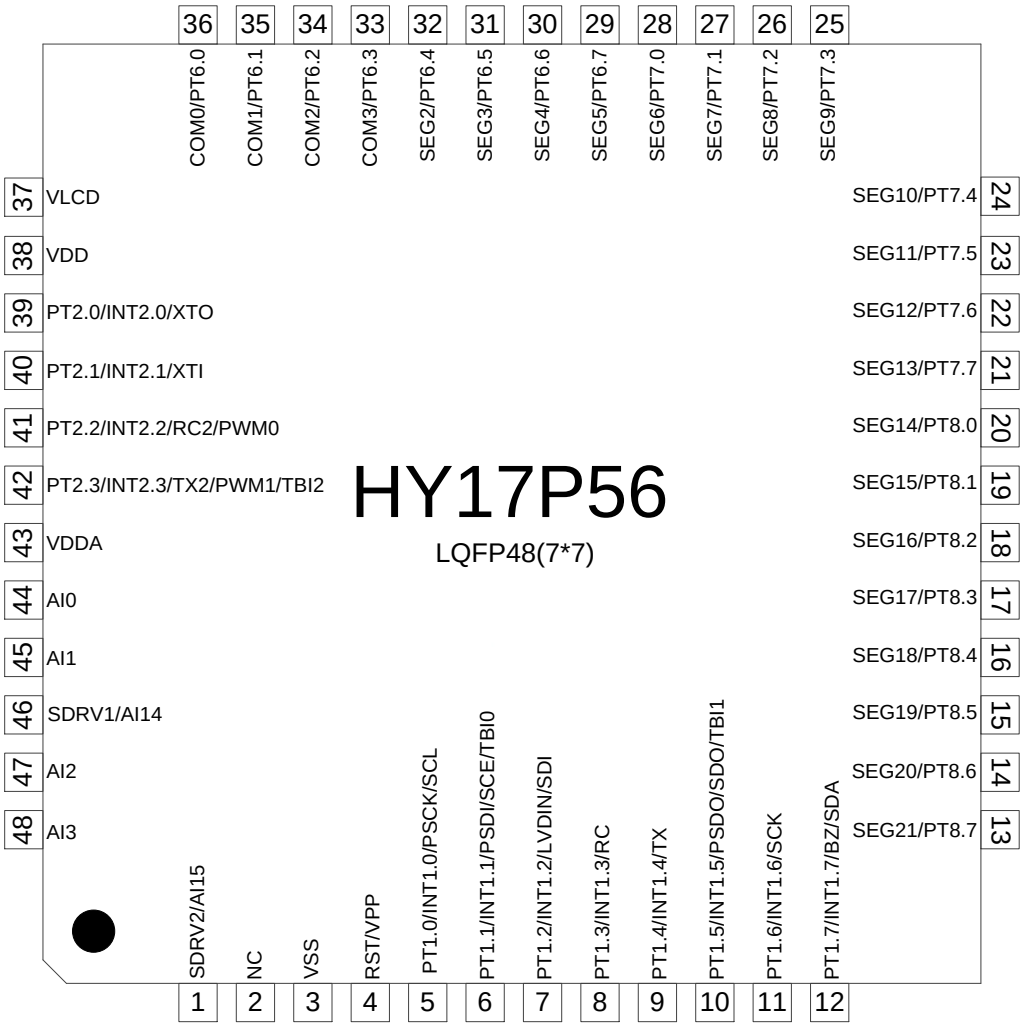
1. 特点

- 8 位加强型精简指令集，共有 71 个指令包含硬件乘法指令及查表指令 H08D
- 2.2V to 5.5V 工作电压范围，-40℃~85℃工作温度范围.
- 支持外部石英振荡器 1MHz~16MHz /32768Hz 及内部高精度 RC 振荡器 1.843MHz/3.686MHz/7.834MHz Mode 多种 CPU 工作频率切换选择，可让使用者达到最佳省电规划
  - 运行模式
  - 待机模式
  - 休眠模式
- 8KWord OTP Type 程序存储器，512Byte 数据存储器
- Brownout detector 及 Watch dog Timer ,可防止 CPU 进入死机模式.
- 4x20 LCD 液晶驱动器
  - 1/4 Duty、1/3 Bias
  - 内建 Charge Pump 稳压线路 ,可提供多种 LCD 偏压
  - 24 个 LCD 端口可设定复用为数字输入输出端口
- LVD 低电压检测功能具有 14 段检测电压设置与外部输入电压检测功能
- 模拟电压源 VDDA 具有 10mA 稳压电压源输出，快速启动功能，可提供传感器驱动电压
- 24-Bit ΣΔADC 模拟数字转换器
  - 梳状滤波器采二阶/三阶设计，转换频率达 7.2Ksps
  - 取样频率 460KHz
  - 超取样频率设置 64 ~ 16384
  - 全差动输入信号、测量范围零点调整
  - 内置 PGA(Programmable Gain Amplifier)有 1/4 ~ 128 倍输入信号放大倍率选择
  - 内置绝对温度传感器
- 8-bit 定时器 Timer A1
- 16-bit 定时器 Timer B 模块具 Compare/PWM 功能
- 串行通讯 2*EUART，SPI，I2C 模块
- Built-In EPROM (BIE)，内建 2.75V 低压烧写控制电路
- Support 8 stack Level.

2. 引脚定义

2.1. LQFP48 引脚图



注：VPP 与 RST 复用同一接口，非烧录 OTP 时禁止输入高电压

2.2. I/O 定义与说明

LQFP48 引脚编号	引脚名称	引脚特性		功能说明
		格式	缓冲	
1	SDRV2/AI15 SDRV2 AI15	 O A	 P A	 传感器驱动 模拟输入通道
3	VSS	P	P	芯片工作电压源接地端
4	RST/VPP RST VPP	 I P	 S P	 复位芯片 OTP 读/写时的电压源
5	PT1.0/INT1.0/PSCK/SCL PT1.0 INT1.0 PSCK SCL	 I/O I I I/O	 S/C S S S	 数字输入/输出 中断源 E0IF OTP 读/写界面接口 I2C 通讯接口引脚
6	PT1.1/INT1.1/PSDI/SCE/TBI0 PT1.1 INT1.1 PSDI SCE TBI0	 I/O I I I/O I	 S/C S S S S	 数字输入/输出 中断源 E1IF OTP 读/写界面接口 SPI 通讯接口 TimerB 置能引脚
7	PT1.2/INT1.2/LVDIN/SDI PT1.2 INT1.2 LVDIN SDI	 I/O I A I/O	 S/C S A S	 数字输入/输出 中断源 E2IF LVD 外部信号输入接口 SPI 通讯接口
8	PT1.3/INT1.3/RC PT1.3 INT1.3 RC	 I/O I I	 S/C S S	 数字输入/输出 中断源 E3IF EUART1 通讯接口
9	PT1.4/INT1.4/TX PT1.4 INT1.4 TX	 I/O I O	 S/C S C	 数字输入/输出 中断源 INTF1.4 EUART1 通讯接口
10	PT1.5/INT1.5/PSDO/SDO/TBI1 PT1.5	 I/O	 S/C	 数字输入/输出

LQFP48 引脚编号	引脚名称	引脚特性		功能说明
		格式	缓冲	
	INT1.5	I	S	中断源 INTF1.5
	PSDO	O	C	OTP 读/写界面接口
	SDO	I/O	S	SPI 通讯接口
	TBI1	I	S	TimerB 置能引脚
11	PT1.6/INT1.6/SCK			
	PT1.6	I/O	S/C	数字输入/输出
	INT1.6	I	S	中断源 INTF1.6
	SCK	I/O	S	SPI 通讯接口接口
12	PT1.7/INT1.7/BZ/SDA			
	PT1.7	I/O	S/C	数字输入/输出
	INT1.7	I	S	中断源 INTF1.5
	BZ	O	C	蜂鸣器输出端
	SDA	I/O	S	I2C 通讯接口引脚
13	PT8.7/SEG21			
	PT8.7	I/O	S/C	数字输入/输出
	SEG21	O	A	LCD Segment 输出
14	PT8.6/SEG20			
	PT8.6	I/O	S/C	数字输入/输出
	SEG20	O	A	LCD Segment 输出
15	PT8.5/SEG19			
	PT8.5	I/O	S/C	数字输入/输出
	SEG19	O	A	LCD Segment 输出
16	PT8.4/SEG18			
	PT8.4	I/O	S/C	数字输入/输出
	SEG18	O	A	LCD Segment 输出
17	PT8.3/SEG17			
	PT8.3	I/O	S/C	数字输入/输出
	SEG17	O	A	LCD Segment 输出
18	PT8.2/SEG16			
	PT8.2	I/O	S/C	数字输入/输出
	SEG16	O	A	LCD Segment 输出
19	PT8.1/SEG15			
	PT8.1	I/O	S/C	数字输入/输出
	SEG15	O	A	LCD Segment 输出
20	PT8.0/SEG14			

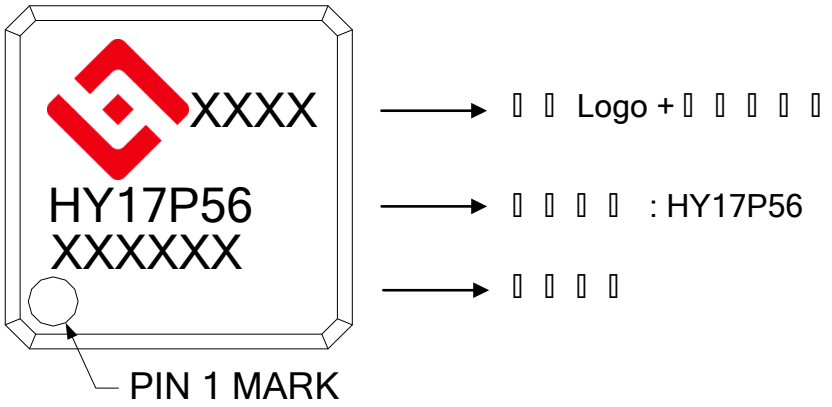
LQFP48 引脚编号	引脚名称	引脚特性		功能说明
		格式	缓冲	
	PT8.0 SEG14	I/O O	S/C A	数字输入/输出 LCD Segment 输出
21	PT7.7/SEG13 PT7.7 SEG13	I/O O	S/C A	数字输入/输出 LCD Segment 输出
22	PT7.6/SEG12 PT7.6 SEG12	I/O O	S/C A	数字输入/输出 LCD Segment 输出
23	PT7.5/SEG11 PT7.5 SEG11	I/O O	S/C A	数字输入/输出 LCD Segment 输出
24	PT7.4/SEG10 PT7.4 SEG10	I/O O	S/C A	数字输入/输出 LCD Segment 输出
25	PT7.3/SEG9 PT7.3 SEG9	I/O O	S/C A	数字输入/输出 LCD Segment 输出
26	PT7.2/SEG8 PT7.2 SEG8	I/O O	S/C A	数字输入/输出 LCD Segment 输出
27	PT7.1/SEG7 PT7.1 SEG7	I/O O	S/C A	数字输入/输出 LCD Segment 输出
28	PT7.0/SEG6 PT7.0 SEG6	I/O O	S/C A	数字输入/输出 LCD Segment 输出
29	PT6.7/SEG5 PT6.7 SEG5	I/O O	S/C A	数字输入/输出 LCD Segment 输出
30	PT6.6/SEG4 PT6.6 SEG4	I/O O	S/C A	数字输入/输出 LCD Segment 输出
31	PT6.5/SEG3 PT6.5 SEG3	I/O O	S/C A	数字输入/输出 LCD Segment 输出

LQFP48 引脚编号	引脚名称	引脚特性		功能说明
		格式	缓冲	
32	PT6.4/SEG2 PT6.4 SEG2	 I/O O	 S/C A	 数字输入/输出 LCD Segment 输出
33	PT6.3/COM3 PT6.3 COM3	 I/O O	 S/C A	 数字输入/输出 LCD COM 输出
34	PT6.2/COM2 PT6.2 COM2	 I/O O	 S/C A	 数字输入/输出 LCD COM 输出
35	PT6.1/COM1 PT6.1 COM1	 I/O O	 S/C A	 数字输入/输出 LCD COM 输出
36	PT6.0/COM0 PT6.0 COM0	 I/O O	 S/C A	 数字输入/输出 LCD COM 输出
37	VLCD	P	P	LCD 的电压源
38	VDD	P	P	芯片工作电压源
39	PT2.0/INT2.0/XTO PT2.0 INT2.0 XTO	 I/O I A	 S/C S A	 数字输入/输出 中断源 INTF2.0 外接振荡器输出端
40	PT2.1/INT2.1/XTI PT2.1 INT2.1 XTI	 I/O I A	 S/C S A	 数字输入/输出 中断源 INTF2.1 外接振荡器输入端
41	PT2.2/INT2.2/RC2/PWM0 PT2.2 INT2.2 RC2 PWM0	 I/O I I O	 S/C S S C	 数字输入/输出 中断源 INTF2.2 EUART2 通讯接口 PWM0 输出接口
42	PT2.3/INT2.3/TX2/PWM1/TBI2 PT2.3 INT2.3 TX2 PWM1	 I/O I O O	 S/C S C C	 数字输入/输出 中断源 INTF2.3 EUART2 通讯接口 PWM1 输出接口

LQFP48 引脚编号	引脚名称	引脚特性		功能说明
		格式	缓冲	
	TBI2	I	S	TimerB 置能引脚
43	VDDA	P	P	稳压器输出，模拟电路电压源
44	AI0	A	A	模拟输入通道
45	AI1	A	A	模拟输入通道
46	SDRV1/AI14 SDRV1 AI14	 O A	 P A	 传感器驱动 模拟输入通道
47	AI2	A	A	模拟输入通道
48	AI3	A	A	模拟输入通道
Others	NC	-	-	未使用(不可连接)

2.3. 封装片丝印信息

2.3.1. LQFP 封装片丝印信息



3. 应用电路

3.1. 桥式传感器 LCD 显示

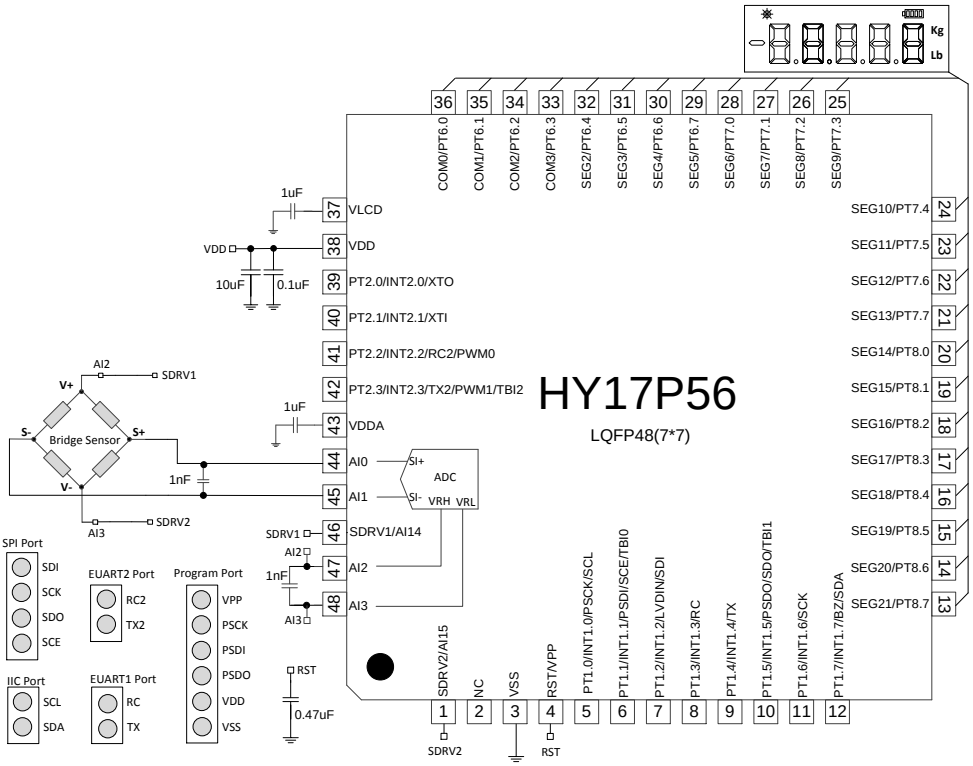


图 3-1 桥式传感器 LCD 显示应用电路

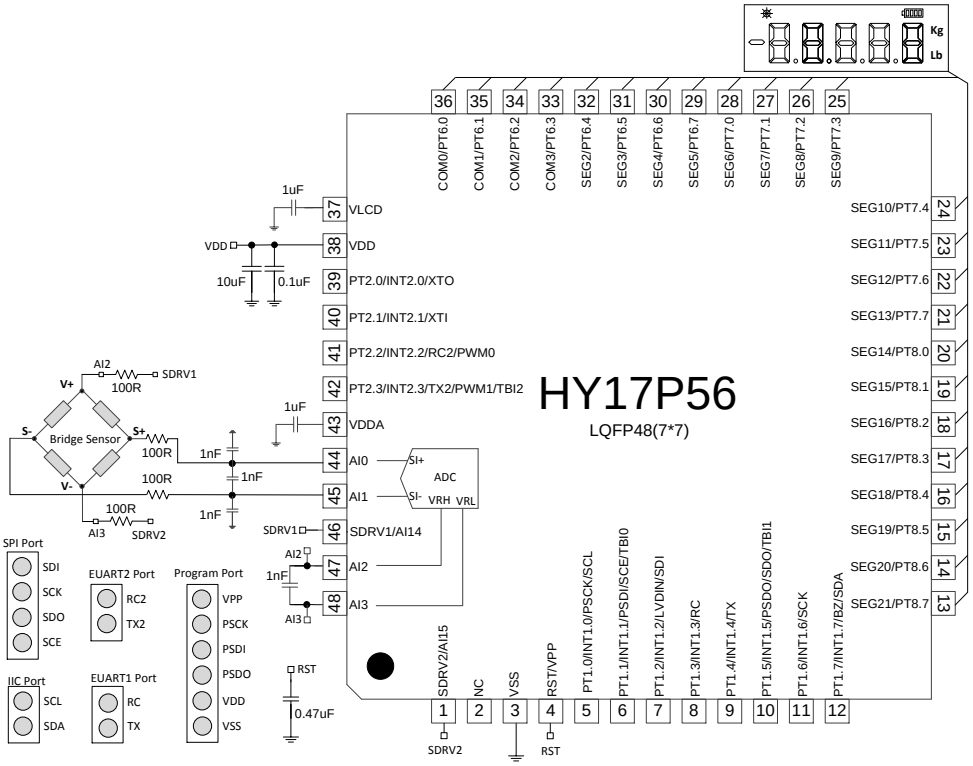


图 3-2 桥式传感器 LCD 显示应用电路-增强 RS 抗干扰能力

4. 功能概述

4.1. 内部方框图

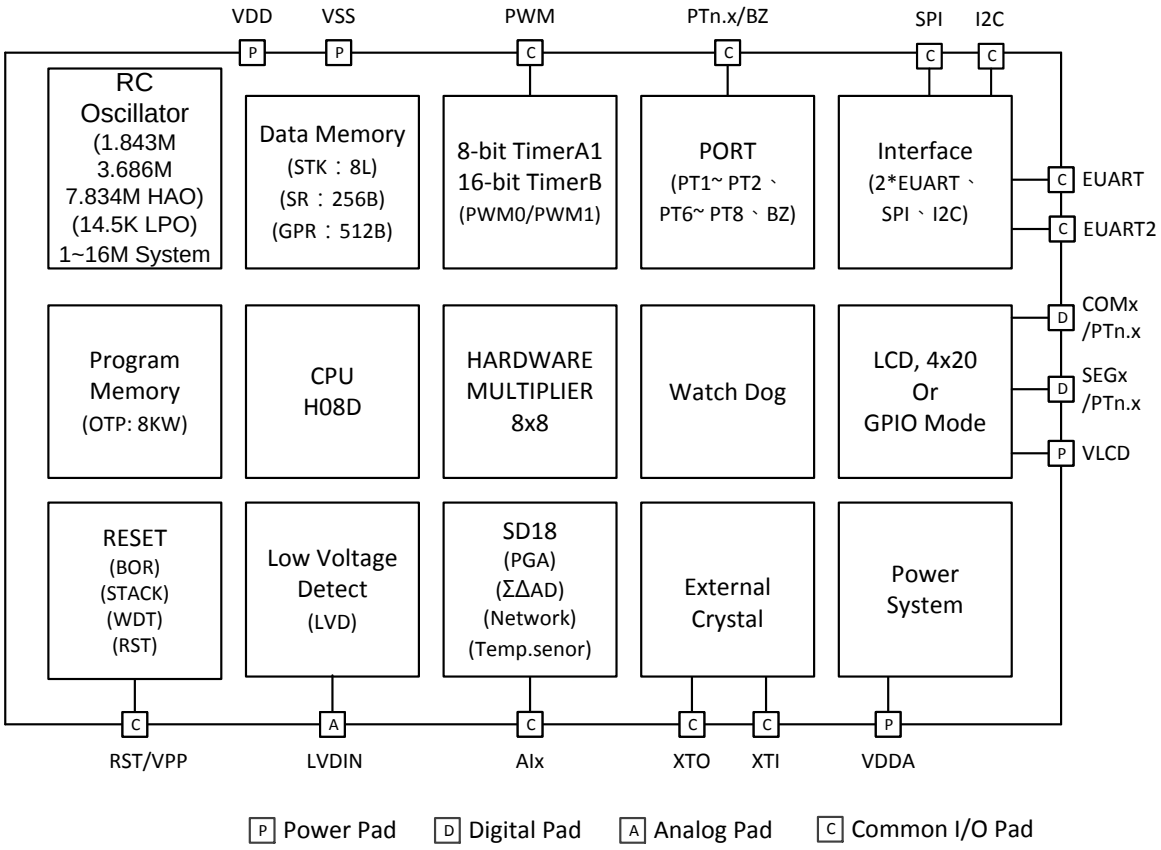


图 4-1 HY17P56 内部方框图

4.2. 相关说明与支持文件

芯片功能相关使用说明书

DS-HY17P56	HY17P56 说明书
UG-HY17S58	HY17S58 使用说明书
APD-CORE002	H08D 指令集说明书

开发工具相关使用说明书

APD-HY17PIDE001	HY17P 系列开发工具软件使用说明书
APD-HY17PIDE002	HY17P 系列开发工具硬件使用说明书
APD-OTP006	HY17P OTP 刻录引脚信息

产品生产相关使用说明书

APD-HY17PIDE004	HY17P 系列生产线专用刻录器说明书

4.3. Clock System

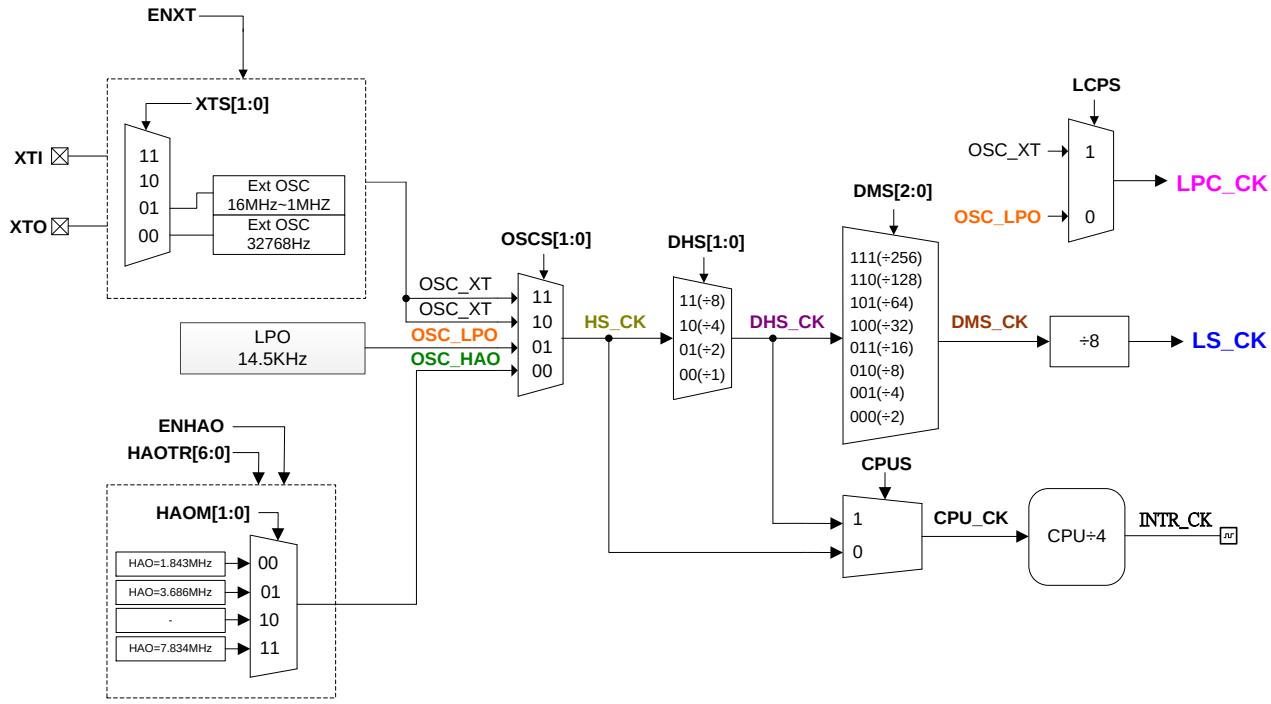


图 4-2 Clock System 模块方框图(一)

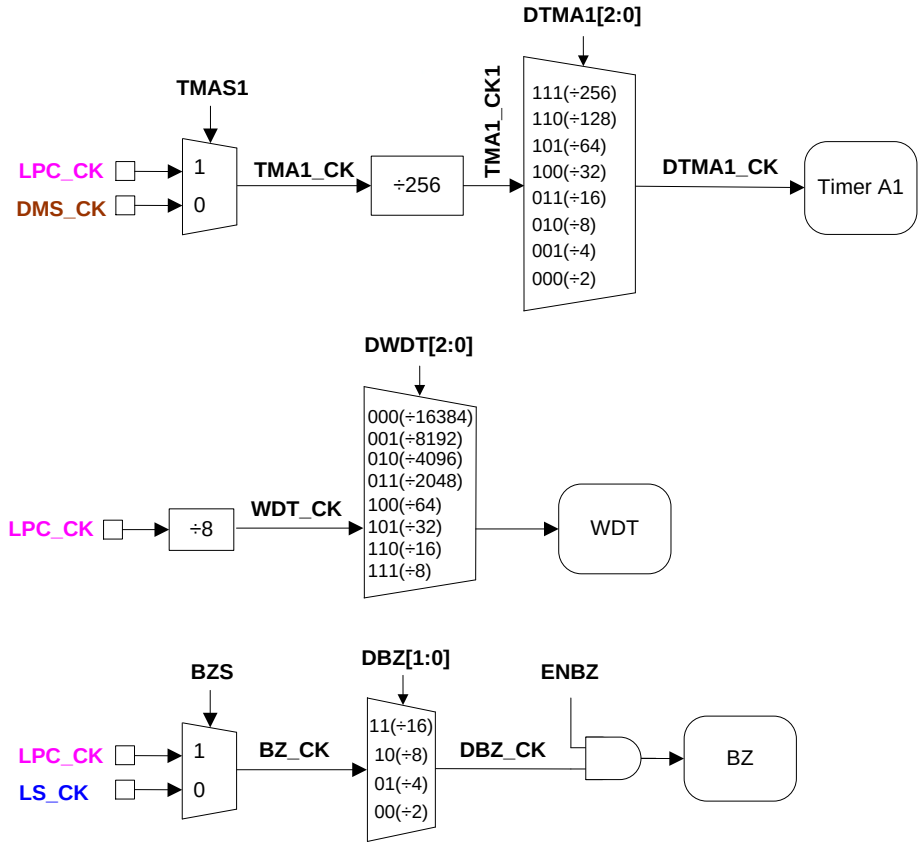


图 4-3 Clock System 模块方框图(二)

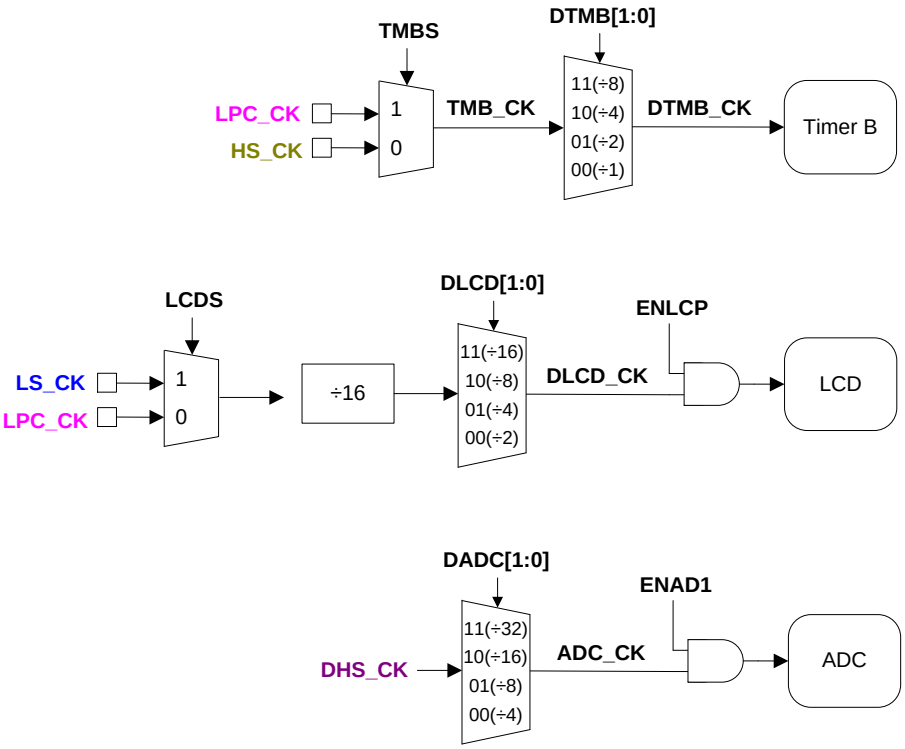


图 4-4 Clock System 模块方框图(三)

4.4. Low Voltage Detect(LVD)

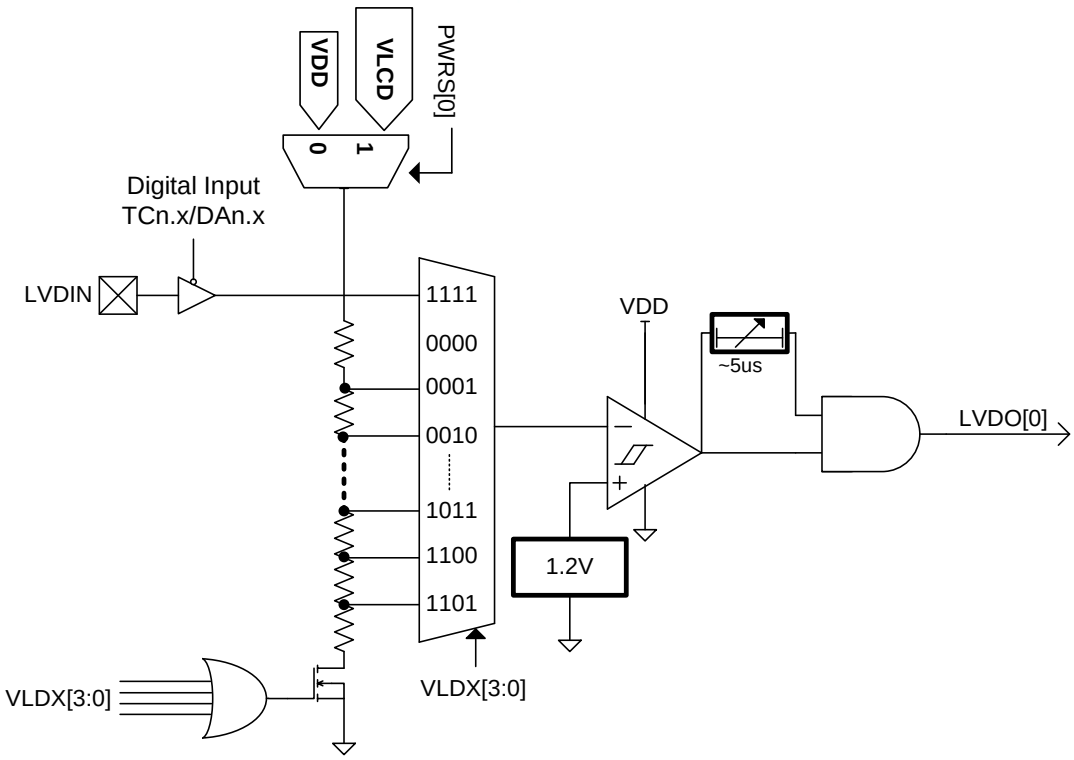


图 4-5 Low Voltage Detect 模块方框图

4.5. Reset

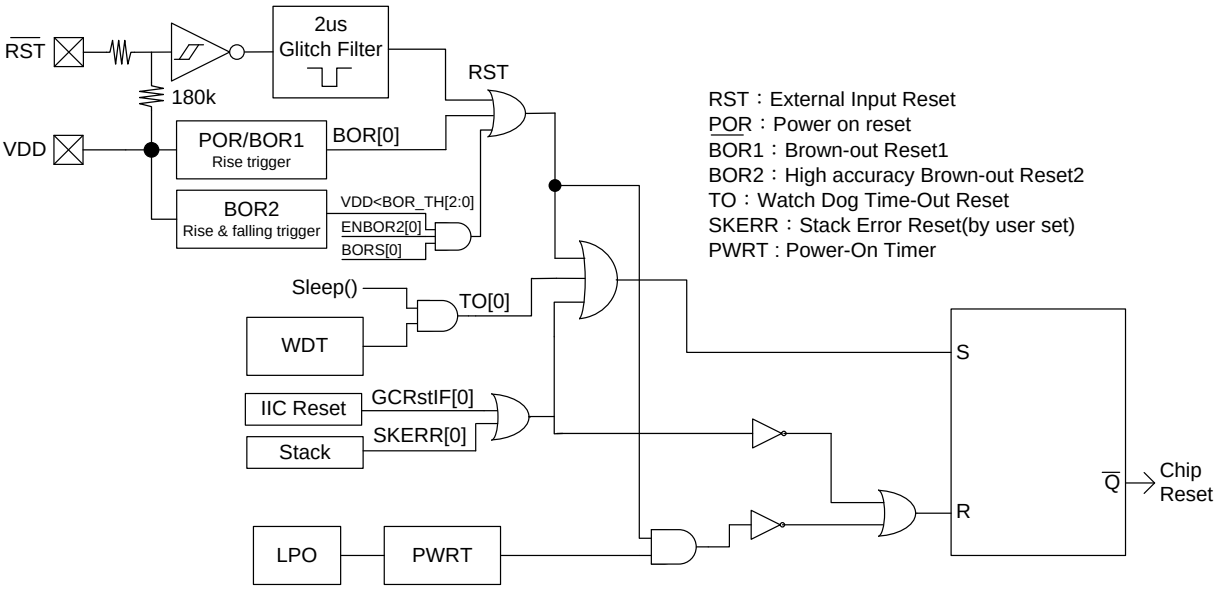


图 4-6 Reset 模块方框图

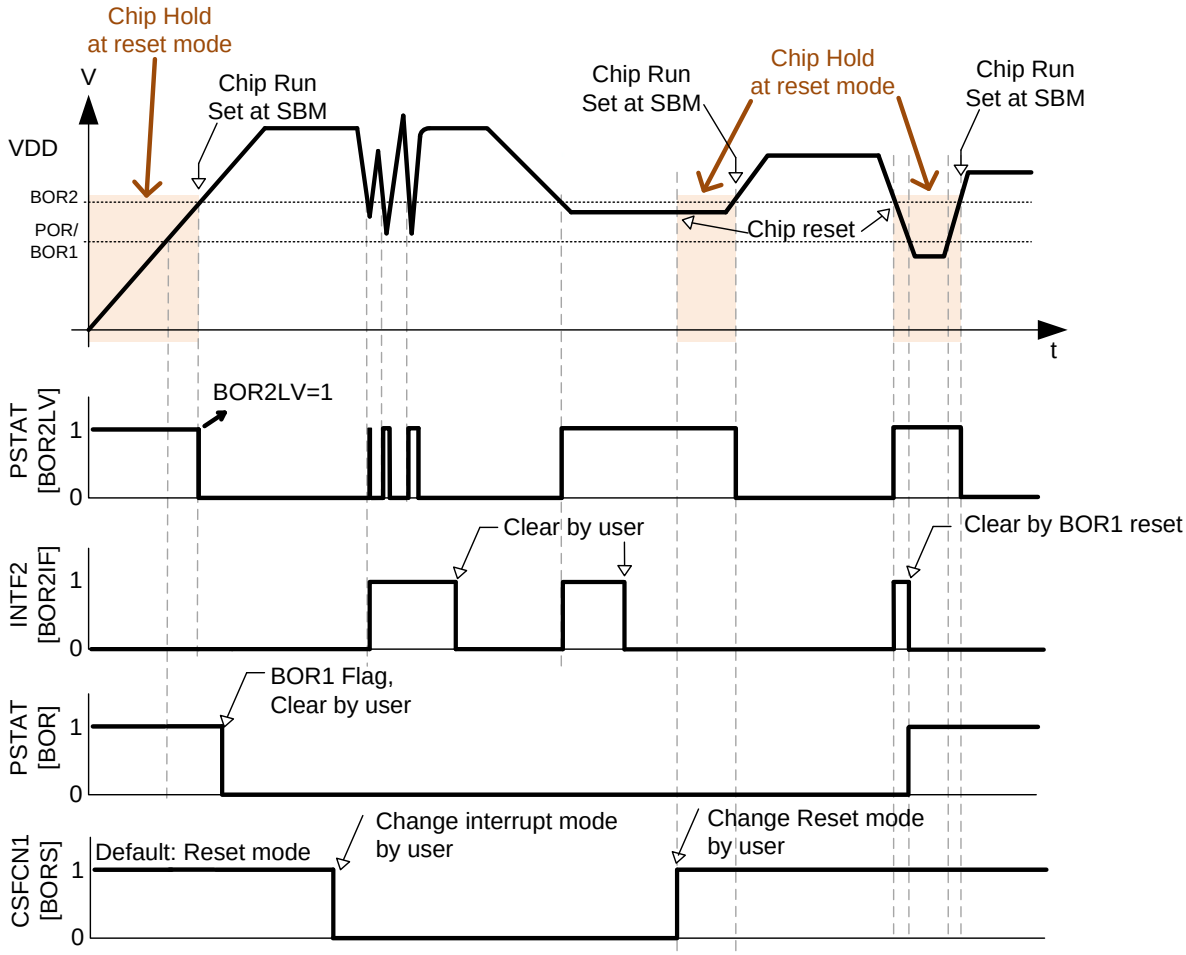


图 4-7 BOR1 and BOR2 Chart

4.6. Power System

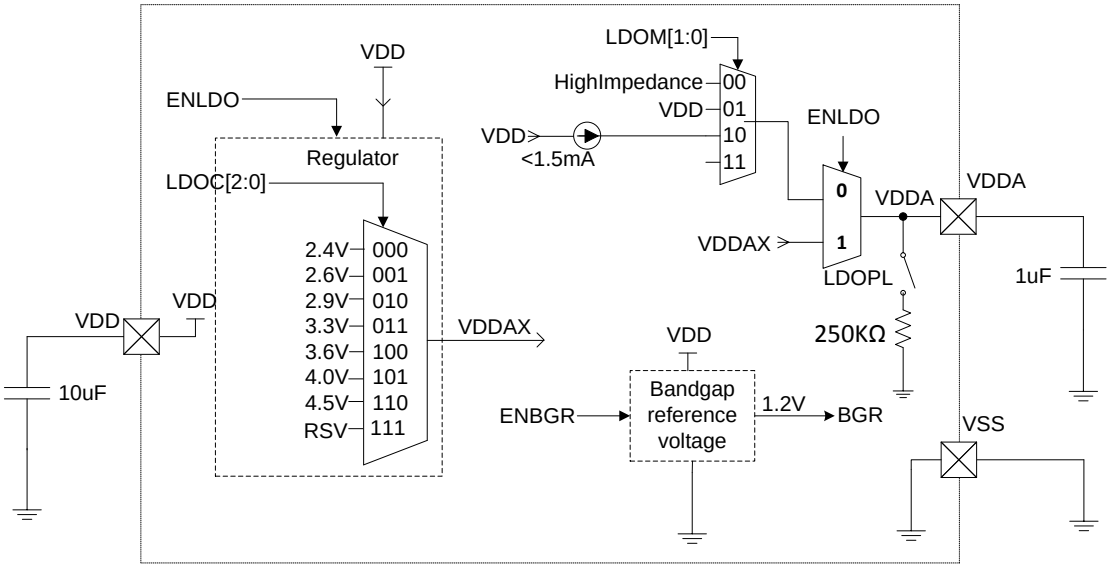
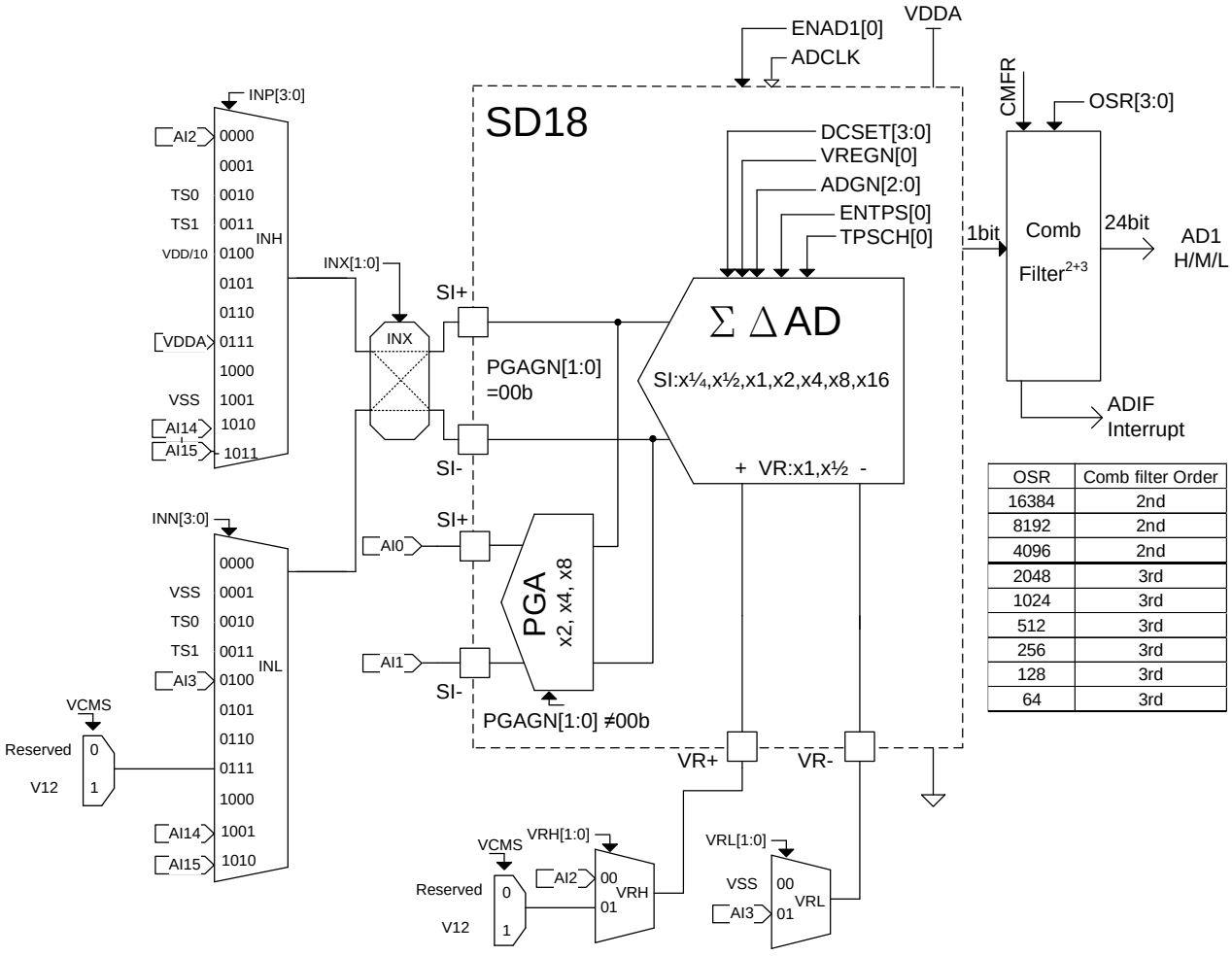


图 4-8 Power System 模块方框图

4.7. SD18 Network



OSR	Comb filter Order
16384	2nd
8192	2nd
4096	2nd
2048	3rd
1024	3rd
512	3rd
256	3rd
128	3rd
64	3rd

图 4-9 SD18 Network 模块方框图

4.8. GPIO PT1 and PT2

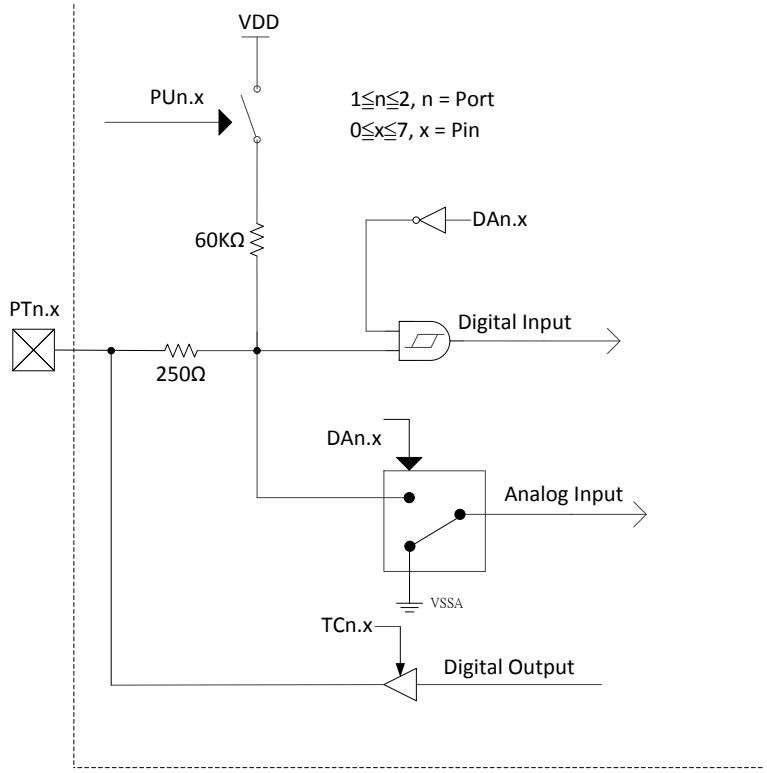


图 4-10 GPIO PT1 and PT2 模块方框图

4.9. GPIO PT6/COM0~COM3

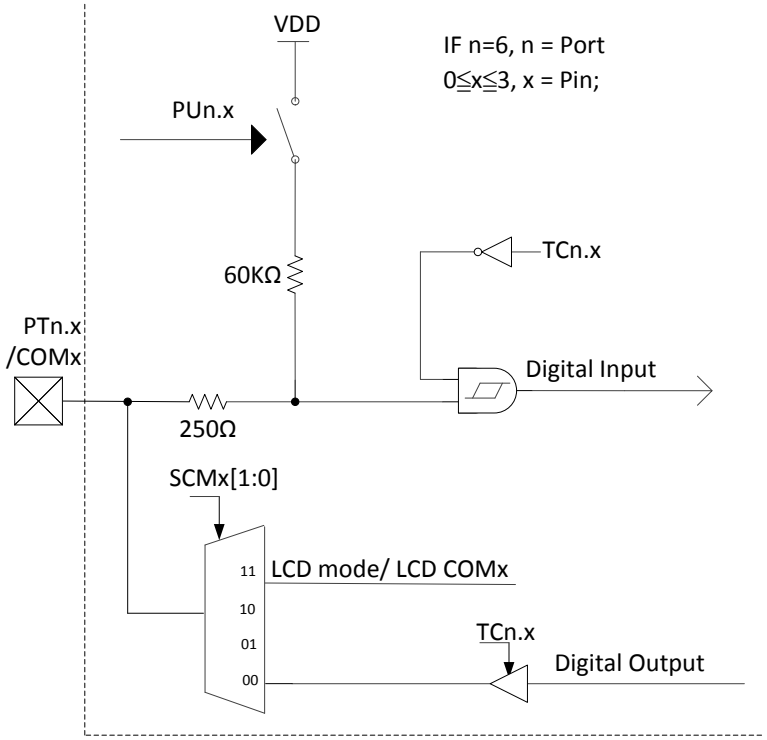


图 4-11 GPIO PT6/COM0~COM3 模块方框图

4.10. GPIO PT6~PT7/SEG2~SEG13

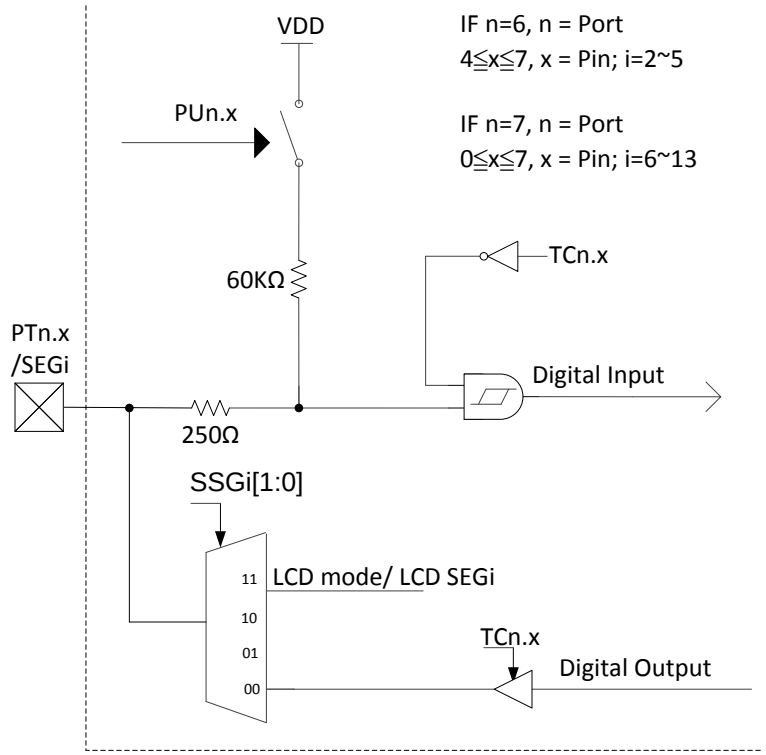


图 4-12 GPIO PT6~PT7/SEG2~SEG13 模块方框图

4.11. GPIO PT8/SEG14~SEG21

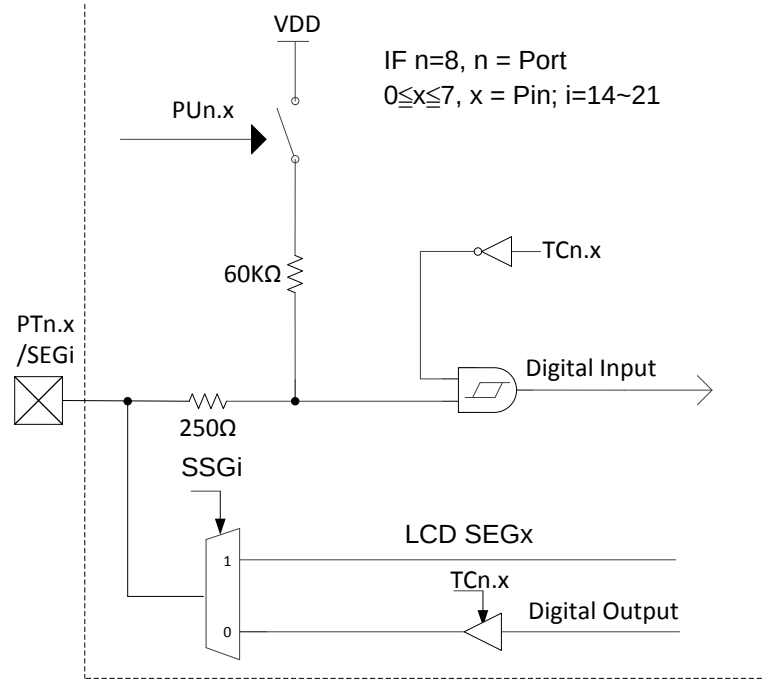


图 4-13 GPIO PT8/SEG14~SEG21 模块方框图

4.12. Watch Dog

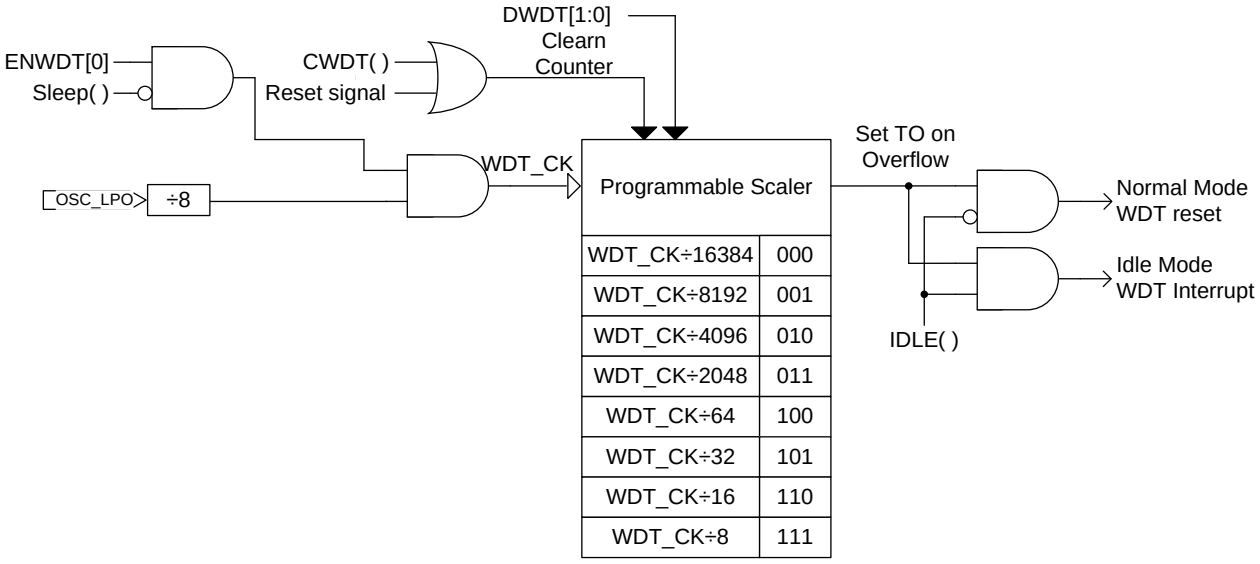


图 4-14 Watch Dog 模块方框图

4.13. 8-bit Timer A1

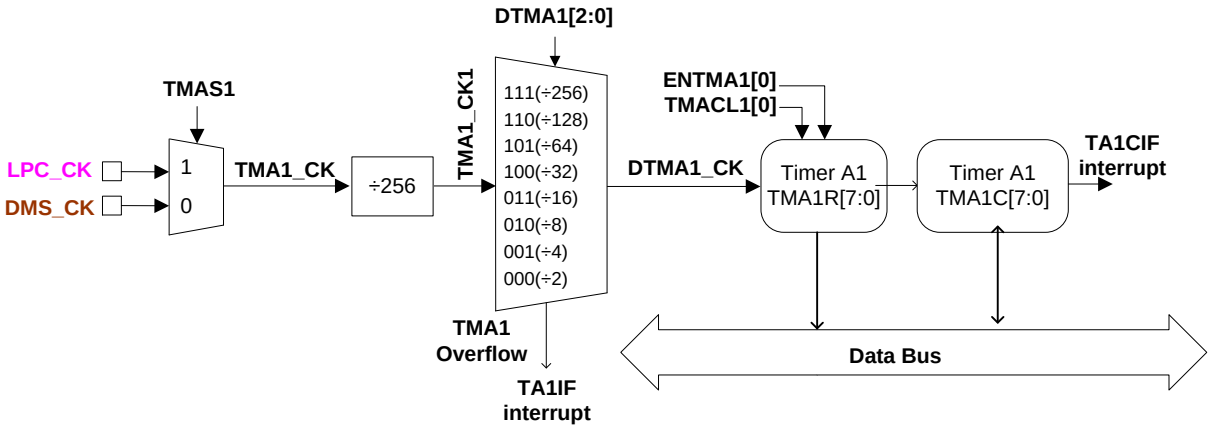


图 4-15 8-bit Timer A1 模块方框图

4.14. 16-bit Timer B

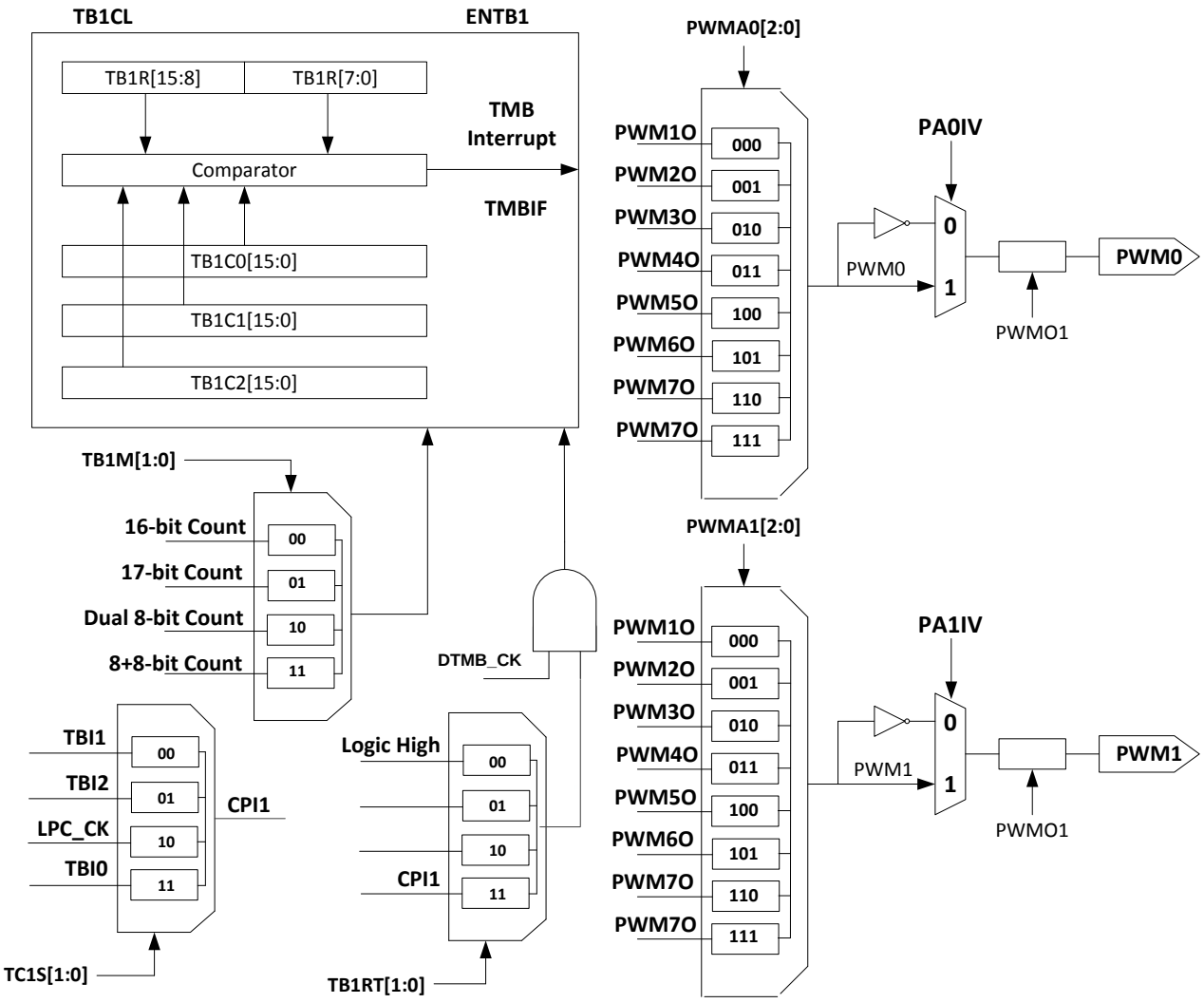


图 4-16 16-bit Timer B 模块方框图

4.15. LCD

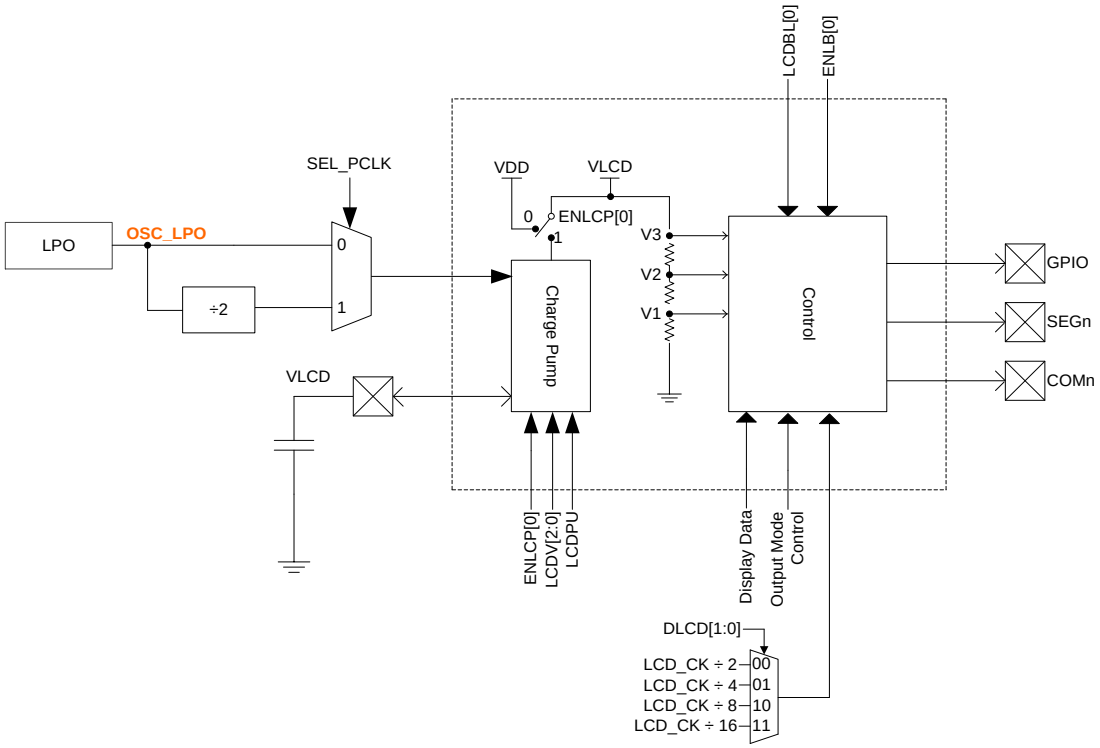


图 4-17 LCD 模块方框图

4.16. EUART and EUART2

EUART TRANSMIT BLOCK DIAGRAM

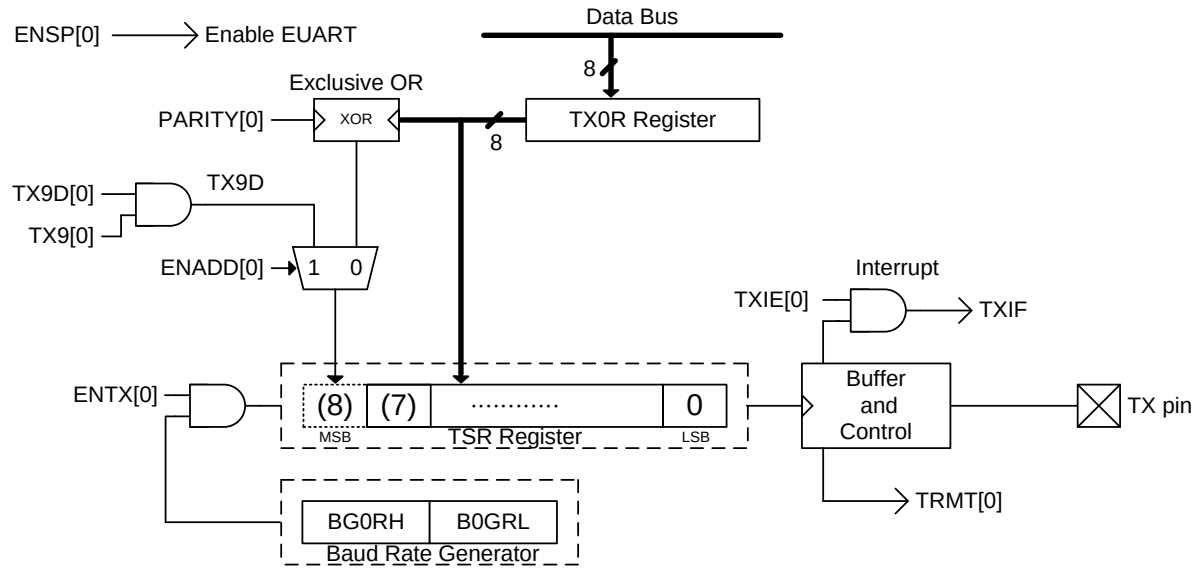
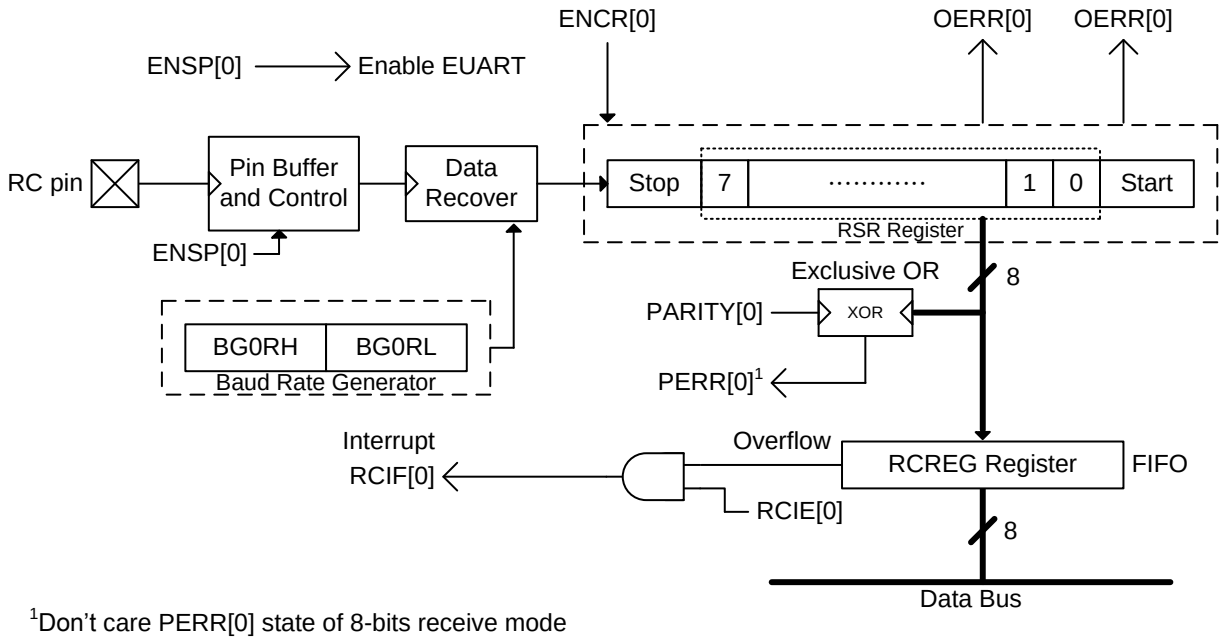


图 4-18 EUART 传送功能方框图

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

图 4-19 EUART 8-bits 接收功能方框图

4.17. SPI

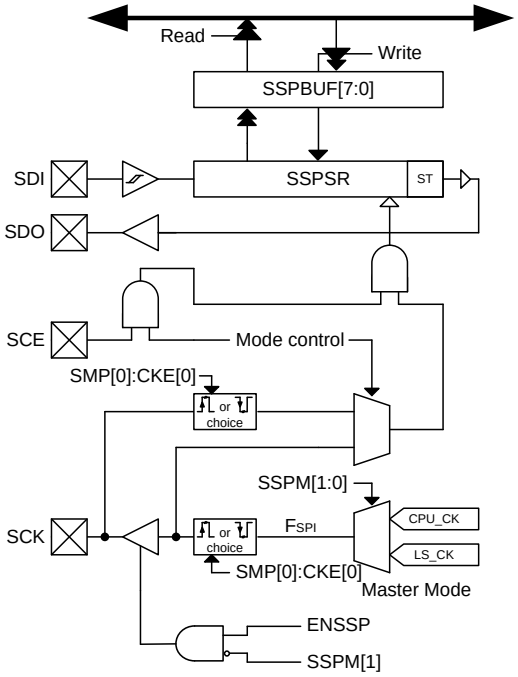


图 4-20 SPI 模块方框图

4.18. I2C

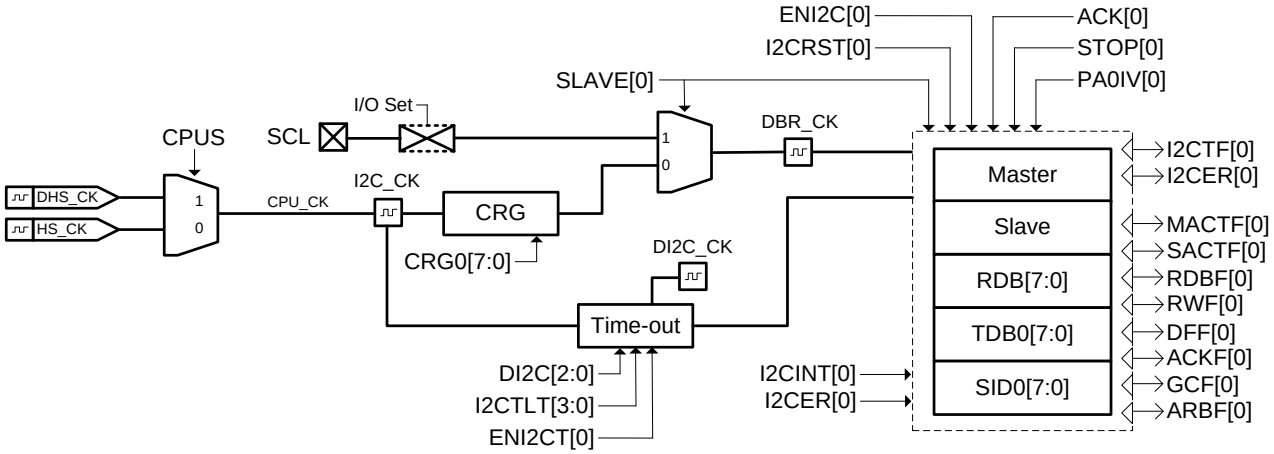


图 4-21 I2C 模块方框图

5. 存储器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005h	INDF1	Contents of FSR1 to address data memory value of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006h	POINC1	Contents of FSR1 to address data memory value of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007h	PODEC1	Contents of FSR1 to address data memory value of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008h	PRINC1	Contents of FSR1 to address data memory value of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009h	PLUSW1	Contents of FSR1 to address data memory value of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ah	INDF2	Contents of FSR2 to address data memory value of FSR2 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Bh	POINC2	Contents of FSR2 to address data memory value of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ch	PODEC2	Contents of FSR2 to address data memory value of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Dh	PRINC2	Contents of FSR2 to address data memory value of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Eh	PLUSW2	Contents of FSR2 to address data memory value of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Fh	FSR0H	-	-	-	-	-	-	FSR0[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR1H	-	-	-	-	-	-	FSR1[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
013h	FSR2H	-	-	-	-	-	-	FSR2[9:8]		xx	.... ..uu	-,-,-,- -,-,*,*
014h	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	TOS[12:8]					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	SKPRT[3:0]				000. 0000	u$$. $$$$	rw 0,rw 0,rw 0,- *,*,*,*
01Ah	PCLATH	-	-	-	PC[12:8]					...0 0000	...0 0000	*,*,*,*,*,*,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Dh	TBLPTRH	-	-	-	TBLPTR[12:8]					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE		E1IE	E0IE	0000 0000	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	TA1IE	SPIIE	TXIE	RCIE	I2CERIE	I2CIE	E3IE	E2IE	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
025h	INTE2	-	-	-	-	TX2IE	RC2IE	-	BOR2IE	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF	-	E1IF	E0IF	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	TA1IF	SPIIF	TXIF	RCIF	I2CERIF	I2CIF	E3IF	E2IF	0000 0000	uuuu uuuu	*,*,*,* r,r,*,*
028h	INTF2	-	-	-	-	TX2IF	RC2IF	-	BOR2IF	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Ah	BSRCN	-	-	-	-	-	-	BSR[1:0]		xx	.... ..uu	-,-,-,- -,-,*,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	BOR2LV	GCRstIF	$000 $000	uu$u u$uu	rw0,rw0,rw0,rw0 rw0,rw0,r,rw0
02Eh	BIECN	1	-	-	ENBVD	VPPHV	ENBCP	BIEWR	BIERD	1.00 $000	1.00 $uuu	r1,-,*,* r,*,*,*
02Fh	BIEARH	-	-	1	1	1	1	1	1	0.xx xxxx	u.uu uuuu	*,-,*,*,*,*,*,*
030h	BIEARL			BIE Address Register as BIEAL[5:0]						xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
031h	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
032h	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
033h	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	CSFON	0000 0000	uuuu u00u	*,*,*,* *,w r0,w r0,*
034h	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
035h	OSCCN1	CCOPT	LCPS	DADC[1:0]		DTMB[1:0]		TMBS	LCDS	0000 0000	uuuu uuu.	*,*,*,*,*,*,-
036h	OSCCN2	DLCD[1:0]		ENXT	XTS[1:0]		HAOM[1:0]		ENHAO	0000 0001	uuuu uuu1	*,*,*,*,*,*,*,*
037h	CSFCN0	SKRST	HAOTR[6:0]							.1..	....	-,-,-,- -,-,-,-
038h	CSFCN1	ENSDRV	-	-	BOR_TH[2:0]			BORS	ENBOR2	...0 0011	uuuu uuuu	-,-,-,*,*,*,*,*
039h	WDTCN	ENBZ	BZS	DBZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw 1,*,*,*

表 5-1 数据存储器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
03Ah	AD1H	ADC1 conversion high byte data register								..00 0000	..uu uuuu	-,-,*,*,*,*,*
03Bh	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*
03Ch	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	*,*,*,*,*,*,*
03Dh	AD1CN0	ENAD1	-	-	OSR[3:0]				CMFR	0..0 0000	uuu. uuuu	*,*,*,*,*,*,*
03Eh	AD1CN1	-	-	VREGN	PGAGN[1:0]		ADGN[2:0]			xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
03Fh	AD1CN2	INIS1	-	-	-	DCSET[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
040h	AD1CN3	INP[3:0]				INN[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
041h	AD1CN4	VRH[1:0]		VRL[1:0]		INX[1:0]		VRIS	INIS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
042h	AD1CN5	ENACM	-	VCMS	LDOPL	-	-	ENTPS	TPSCH	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
043h	LVDCN	-	-	PWRS	LVDS[3:0]				LVDO	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
044h	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-	-	0000 00.0	u0uu uu.u	*,rw1,*,*,*,-,*
045h	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
046h	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
047h	TB1Flag	-	PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,-,r,r r,r,r,r
048h	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	PWMO1	PWMO0	0000 0000	uuuu u0uu	*,*,*,*,rw1,*,*
049h	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*
04Ah	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04Bh	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04Ch	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
04Dh	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
04Eh	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
04Fh	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
050h	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
051h	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
052h	TC1CN0	-	TC1S[1:0]		-	-	-	-	-	0000 0000	uuuu uuuu	uuuu uuuu
053h	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
054h	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
055h	PT1DA	DA1.7	DA1.6	DA1.5	DA1.4	DA1.3	DA1.2	DA1.1	DA1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
056h	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
057h	PT1M1	-	-	-	-	INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*
058h	PT1INT	INTEG7	INTEG6	INTEG5	INTEG4	INTEG3	INTEG2	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
059h	PT1INTE	INTE1.7	INTE1.6	INTE1.5	INTE1.4	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
05Ah	PT1INTF	INTF1.7	INTF1.6	INTF1.5	INTF1.4	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
05Bh	PT2	-	-	-	-	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
05Ch	TRISC2	-	-	-	-	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
05Dh	PT2DA	-	-	-	-	DA2.3	DA2.2	DA2.1	DA2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
05Eh	PT2PU	-	-	-	-	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
05Fh	PT2INT	-	-	-	-	INTG2.3	INTG2.2	INTG2.1	INTG2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
060h	PT2INTE	-	-	-	-	INTE2.3	INTE2.2	INTE2.1	INTE2.0	0000 0000	uuuu uuuu	
061h	PT2INTF	-	-	-	-	INTF2.3	INTF2.2	INTF2.1	INTF2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
062h	PT6	PT6.7	PT6.6	PT6.5	PT6.4	PT6.3	PT6.2	PT6.1	PT6.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
063h	TRISC6	TC6.7	TC6.6	TC6.5	TC6.4	TC6.3	TC6.2	TC6.1	TC6.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
064h	PT6DA	DA6.7	DA6.6	DA6.5	DA6.4	DA6.3	DA6.2	DA6.1	DA6.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
065h	PT6PU	PU6.7	PU6.6	PU6.5	PU6.4	PU6.3	PU6.2	PU6.1	PU6.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
066h	PT7	PT7.7	PT7.6	PT7.5	PT7.4	PT7.3	PT7.2	PT7.1	PT7.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
067h	TRISC7	TC7.7	TC7.6	TC7.5	TC7.4	TC7.3	TC7.2	TC7.1	TC7.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
068h	PT7DA	DA7.7	DA7.6	DA7.5	DA7.4	DA7.3	DA7.2	DA7.1	DA7.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
069h	PT7PU	PU7.7	PU7.6	PU7.5	PU7.4	PU7.3	PU7.2	PU7.1	PU7.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
06Ah	PT8	PT8.7	PT8.6	PT8.5	PT8.4	PT8.3	PT8.2	PT8.1	PT8.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*
06Bh	TRISC8	TC8.7	TC8.6	TC8.5	TC8.4	TC8.3	TC8.2	TC8.1	TC8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
06Ch	PT8DA	DA8.7	DA8.6	DA8.5	DA8.4	DA8.3	DA8.2	DA8.1	DA8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
06Dh	PT8PU	PU8.7	PU8.6	PU8.5	PU8.4	PU8.3	PU8.2	PU8.1	PU8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*
06Eh	SSPCN0	ENSSP	CKP	CKE	SMP	-	-	SSPM[1:0]		0000 ..00	uuuu ..uu	*,*,*,*,-,-,*,*
06Fh	SSPSTA0	SSPBY	SSPOV	-	-	-	-	-	BF	00.. ...0	uu.. ...u	*,*,-,-,-,-,-,*
070h	SSPBUF0	SSP Receive/Transmit Buffer Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*

表 5-2 数据存储器列表(续)

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
071h	CFG0	-	-	-	-	-	GCRst	ENI2CT	ENI2C	0000 0000	.... .uuu	-,-,-,- -,*,*,*
072h	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
073h	STA0	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
074h	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
075h	TOC0	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
076h	RDB0	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
077h	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
078h	SID0	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
079h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,*,-,-,*
07Ah	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw0
07Bh	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD	 0000	.... uuuu	-,-,-,- *,*,*,*'
07Ch	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
07Dh	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
07Eh	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
07Fh	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
180h	LCDCN1	ENLCP	LCDV[2:0]			ENLB	SELPCLK	-	LCDPU	0000 00.0	uuuu uu.u	*,*,*,*,*,*,*,*
181h	LCDCN2	-	-	-	-	-	-	LCDBL	LCI	0000 00..	uuuu uu..	*,*,*,*,*,-,-,-
182h	LCDCN3	SCM3[1:0]		SCM2[1:0]		SCM1[1:0]		SCM0[1:0]		1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
183h	LCDCN4	SSG21	SSG20	SSG19	SSG18	SSG17	SSG16	SSG15	SSG14	1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
185h	LCDCN6	SSG5[1:0]		SSG4[1:0]		SSG3[1:0]		SSG02[1:0]		1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
186h	LCDCN7	SSG9[1:0]		SSG8[1:0]		SSG7[1:0]		SSG6[1:0]		1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
187h	LCDCN8	SSG13[1:0]		SSG12[1:0]		SSG11[1:0]		SSG10[1:0]		1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
188h	LCD0	LCD SEG3[4:7] data				LCD SEG2[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
189h	LCD1	LCD SEG5[4:7] data				LCD SEG4[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Ah	LCD2	LCD SEG7[4:7] data				LCD SEG6[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Bh	LCD3	LCD SEG9[4:7] data				LCD SEG8[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Ch	LCD4	LCD SEG11[4:7] data				LCD SEG10[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Dh	LCD5	LCD SEG13[4:7] data				LCD SEG12[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Eh	LCD6	LCD SEG15[4:7] data				LCD SEG14[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18Fh	LCD7	LCD SEG17[4:7] data				LCD SEG16[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
190h	LCD8	LCD SEG19[4:7] data				LCD SEG18[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
191h	LCD9	LCD SEG21[4:7] data				LCD SEG20[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
192h	UR2CN	ENSP2	ENTX2	TX92	TX9D2	PARITY2	-	-	WUE2	0000 0..0	uuuu u..u	*,*,*,*,*,-,-,*
193h	UR2STA	-	RC9D2	PERR2	FERR2	OERR2	RCIDL2	TRMT2	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw0
194h	BA2CN	-	-	-	-	ENCR2	RC92	ENADD2	ENABD2	 0000	.... uuuu	-,-,-,- *,*,*,*'
195h	BG2RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
196h	BG2RL	Baud Rate2 Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
197h	TX2R	UART2 Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
198h	RC2REG	UART2 Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
080h ~ 0FFh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
100h ~ 17Fh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
200h ~ 2FFh		SRAM as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-3 数据存储器列表(续)

6. 电气特性

Absolute Maximum Ratings :

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD to VSS . . . . . −0.2 V to 6.0 V

Voltage applied to any pin . . . . . −0.2 V to VDD + 0.3 V

Voltage applied to RST/VPP pin . . . . . −0.2 V to 8.75 V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 125℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any I/O pin. 20mA

6.1. Recommended operating conditions

TA = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
VDD	Supply Voltage		All digital peripherals and CPU VDD = 2.0V~5.5V, Frequency<=9.6Mhz, VDD = 3.6V~5.5V, Frequency<=16Mhz,		2.0		5.5	V
VDDA	Supply Voltage		Analog peripherals		2.4		4.5	
VSS	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	VDD = 2.2V~5.5V, ENXT[0]=1	XTS[1:0]=0x	32768			Hz
		Ceramic resonator, Crystal		XTS[1:0]=10	450K		4M	
				XTS[1:0]=11	1M		8M	
		Ceramic resonator, Crystal	VDD = 3.6V~5.5V, ENXT[0]=1	XTS[1:0]=11	450K		16M	

6.2. Internal RC Oscillator

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00	-20%	1.843	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=01	-20%	3.686	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=11	-20%	7.834	+20%	MHz
		After Frequency Trim by Writer	-2%		+2%	MHz
LPO	Low Power Oscillator frequency	VDD supply voltage be enable LPO	-20%	14.5	+20%	KHz

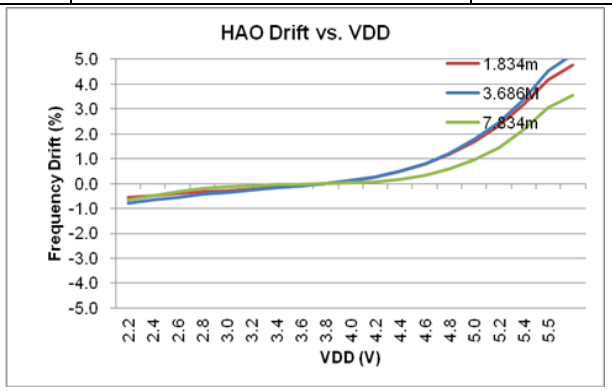


Figure 6.2-1 HAO vs. VDD

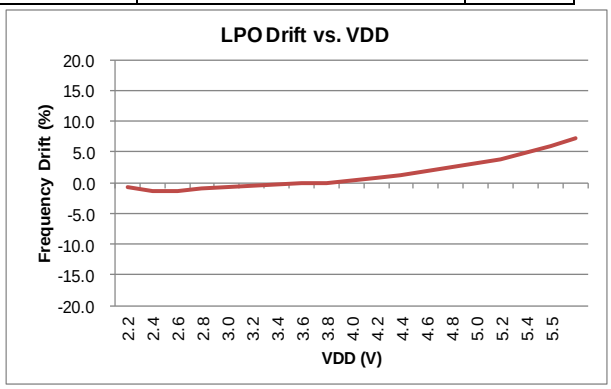


Figure 6.2-2 LPO vs. VDD

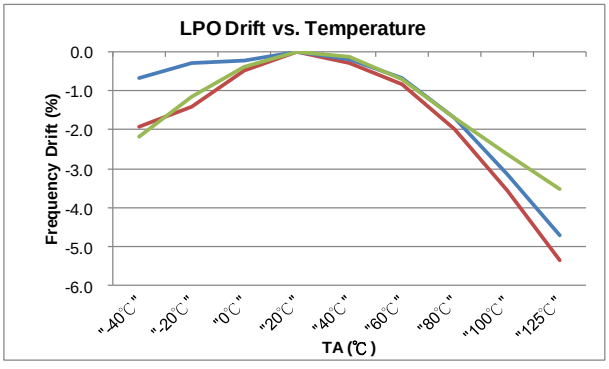


Figure 6.2-3 LPO vs. Temperature

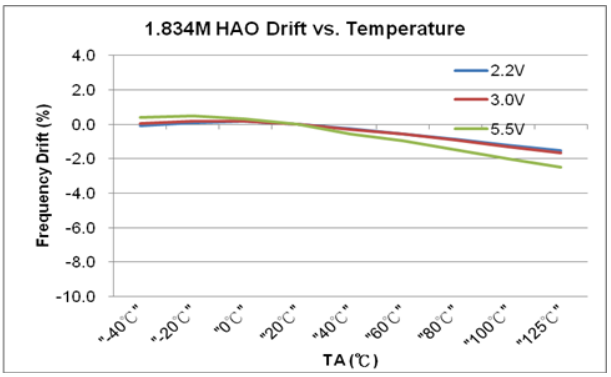


Figure 6.2-4 HAO(1.834MHz) vs. Temperature

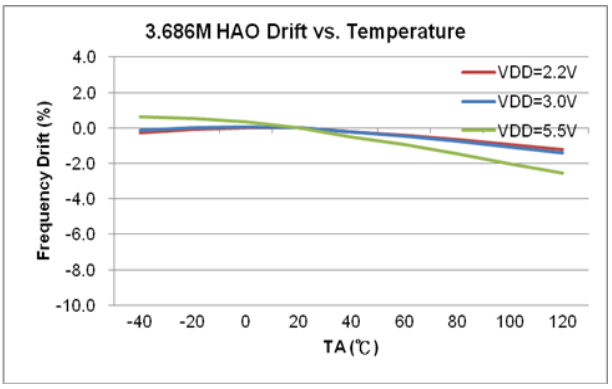


Figure 6.2-5 HAO(3.686MHz) vs. Temperature

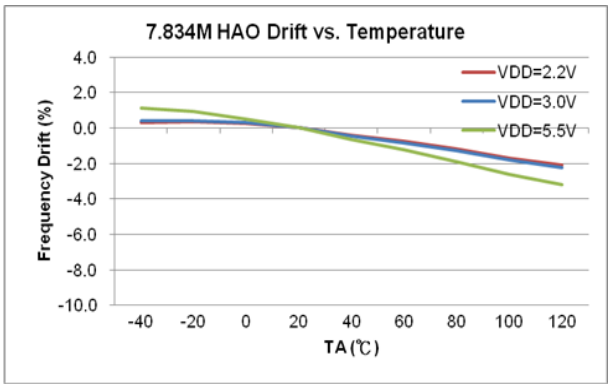


Figure 6.2-6 HAO(7.834MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

TA = 25℃,VDD = 3.0V,OSC_LPO = 14.5KHz, BOR2 OFF, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 7.834MHz, CPU_CK = 7.834MHz		600	1000	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =3.686MHz, CPU_CK = 3.686MHz		320	650	uA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz		280	500	uA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz/2		220	350	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO		2	5	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state		0.5	1.5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state		0.2	1.0	uA
I_{LP4}	Low Power 4	OSC_CY = 32768, OSC_HAO = off, CPU_CK = 32768, Idle state		3.59		uA
I_{LP5}	Low Power 5	OSC_CY = 32768, OSC_HAO = off, CPU_CK = off, Sleep state		1.54		uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

TA = 25℃,VDD = 5.5V,OSC_LPO = 14.5KHz, , BOR2 OFF, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 7.834MHz, CPU_CK = 7.834MHz		1200	1800	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =3.686MHz, CPU_CK = 3.686MHz		720	1200	uA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz		500	1000	uA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz/2		400	800	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO		4	10	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state		1	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state		0.3	2	uA
I_{LP4}	Low Power 4	OSC_CY = 32768, OSC_HAO = off, CPU_CK = 32768, Idle state		8.58		uA
I_{LP5}	Low Power 5	OSC_CY = 32768, OSC_HAO = off, CPU_CK = off, Sleep state		4.33		uA

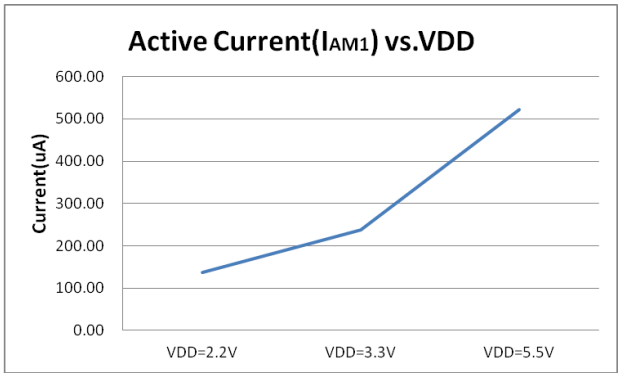


Figure 6.3-1 I_{AM1} vs. VDD

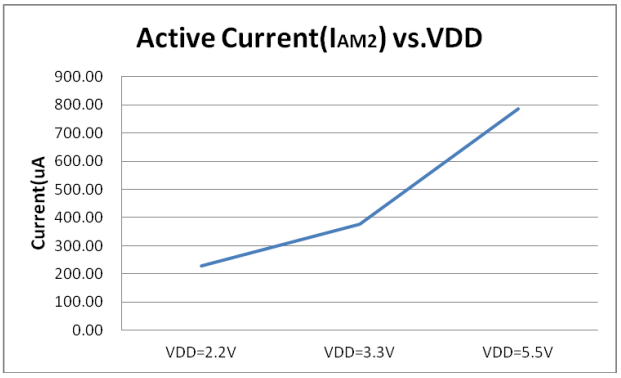


Figure 6.3-2 I_{AM2} vs. VDD

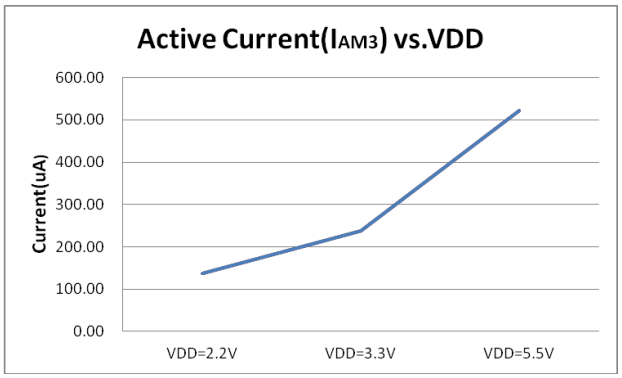


Figure 6.3-3 I_{AM3} vs. VDD

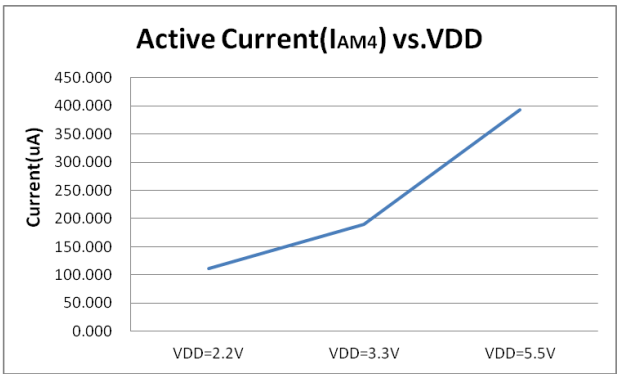


Figure 6.3-4 I_{AM4} vs. VDD

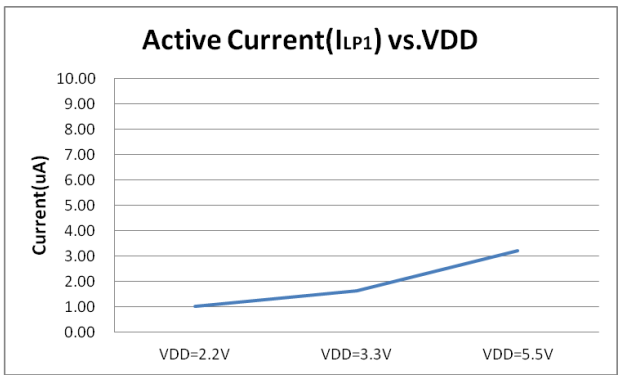


Figure 6.3-5 I_{LP1} vs. VDD

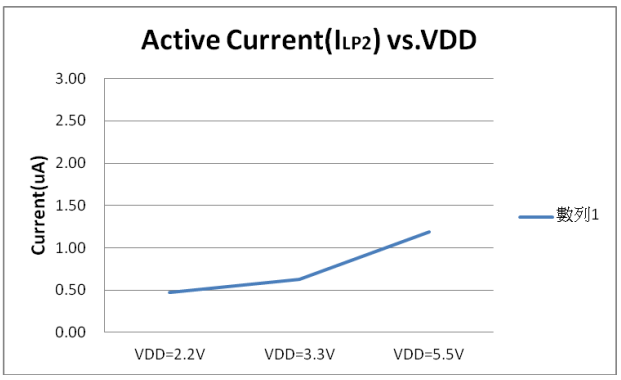


Figure 6.3-6 I_{LP2} vs. VDD

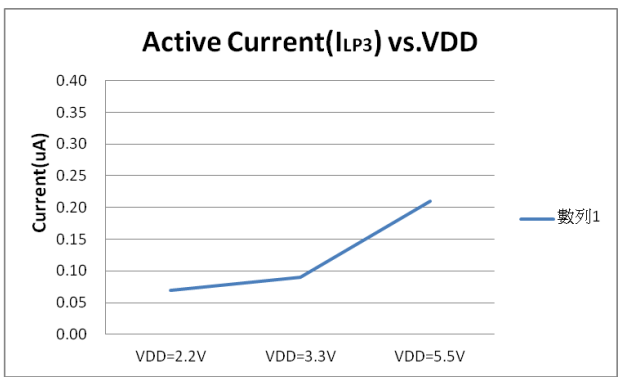


Figure 6.3-7 I_{LP3} vs. VDD

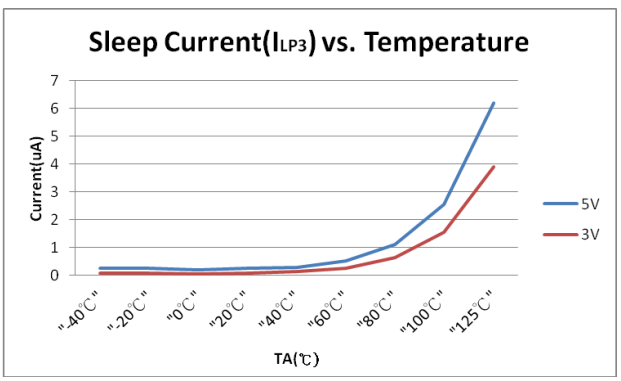


Figure 6.3-8 I_{LP3} vs. Temperature

6.4. Port 1~2, 6~8

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*VDD	V
V_{IL}	Low-Level input voltage		0.3*VDD			
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*VDD		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD<4V, IOH=10mA,	VDD -0.4			V
		VDD>=4V, IOH=15mA,	VDD -0.4			
V_{OL}	Low-level output voltage	VDD<4V, IOL=-10mA			VSS +0.3	
		VDD>=4V, IOL=-15mA			VSS +0.3	

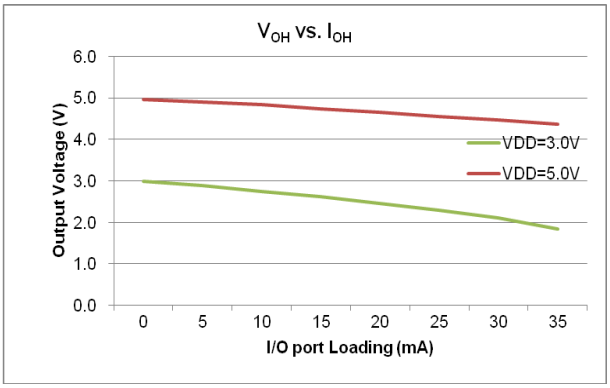


Figure 6.4-1 V_{OH} vs. I_{OH}

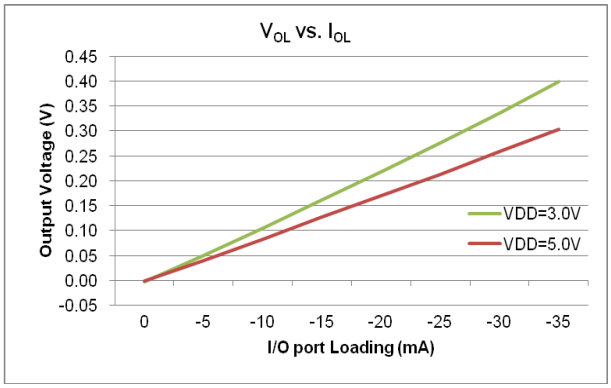


Figure 6.4-2 V_{IH}/V_{IL} vs. VDD

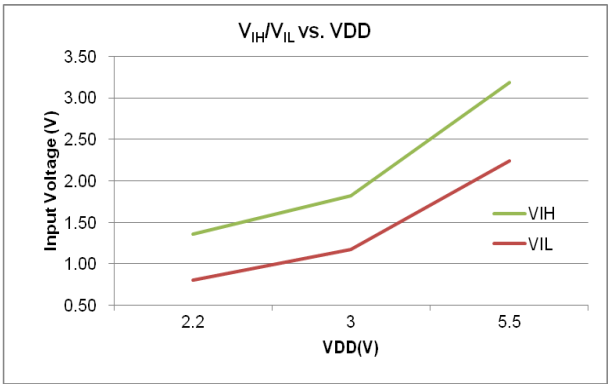


Figure 6.4-3 V_{OL} vs. I_{OL}

6.5. Reset(Brownout, Low Voltage Detect)

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR1}			2			us
	VDD Start Voltage to accepted reset internally (L➔H),V_{HYS1}			1.15	1.48	1.75	V
	BOR1 current, I_{BOR1}				0.2	0.5	uA
	Temperature Drift				30		%
BOR2	Pulse length needed to accepted reset internally, t_{d-LVR2}			2			us
	VDD Start Voltage to accepted reset internally (L➔H),V_{HYS2}, and BOR_TH[2:0]:		000b	1.56	1.70	1.84	V
			001b	1.82	1.98	2.14	
			010b	2.02	2.20	2.38	
			011b	2.27	2.47	2.67	
			100b	2.48	2.70	2.92	
			101b	2.73	2.97	3.21	
			110b	3.24	3.60	3.96	
			111b	3.56	3.95	4.35	
	VDD Start Voltage to accepted reset internally (H➔L),V_{LVR2}, and BOR_TH[2:0]:		000b	1.53	1.66	1.79	V
			001b	1.78	1.93	2.08	
			010b	1.98	2.15	2.32	
			011b	2.23	2.42	2.61	
			100b	2.44	2.65	2.86	
			101b	2.69	2.92	3.15	
			110b	3.19	3.54	3.89	
			111b	3.50	3.89	4.28	
	Hysteresis, $V_{HYS2-LVR2}$			25	60	90	mV
	BOR2 current, I_{BOR2}				10	15	uA
	Temperature Drift				3	5	%
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}			2			us
	Input Voltage to accepted reset voltage				1.1		V
	Reset release voltage				2		V
LVD	Operation current, I_{LVD}				10		uA
	External input voltage to compare reference voltage			1.15	1.2	1.25	V
	Compare reference voltage temperature drift	TA = -40℃ ~ 85 ℃			50		ppm/℃
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1110b			-0.1V	4.0	+0.1V	V

	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1101b		3.6		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1100b		3.3		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1011b		3.0		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1010b		2.9		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1001b		2.8		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=1000b		2.7		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0111b		2.6		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0110b		2.5		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0101b		2.4		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0100b		2.3		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0011b		2.2		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0010b		2.1		
	Detect VDD voltage rang by user option, VSVS VLDS[3:0]=0001b		2.0		

BOR1/BOR2：Brownout Reset 1/2

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

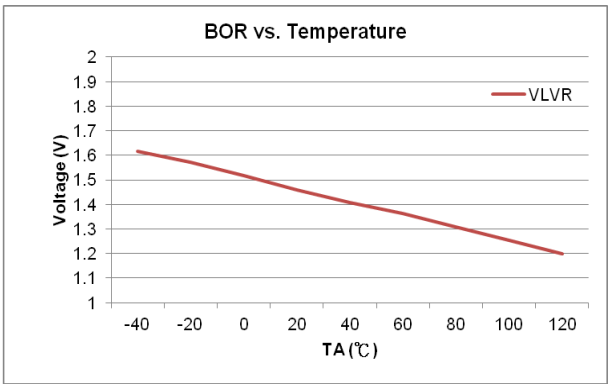


Figure 6.5-1 BOR vs. Temperature

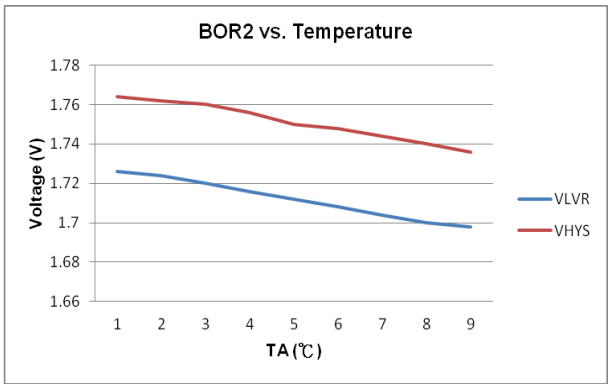


Figure 6.5-2 BOR2 vs. Temperature

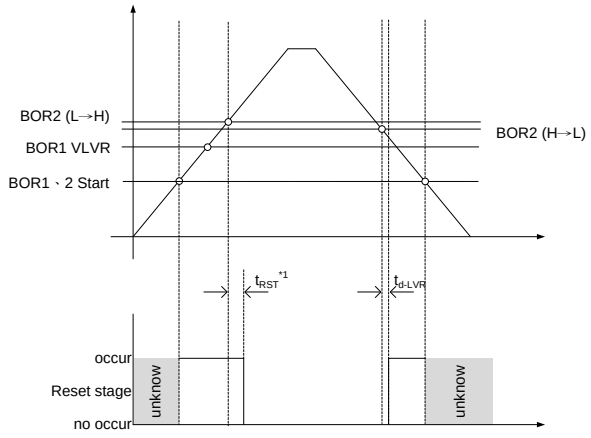


Figure 6.5-2 BOR reset diagram

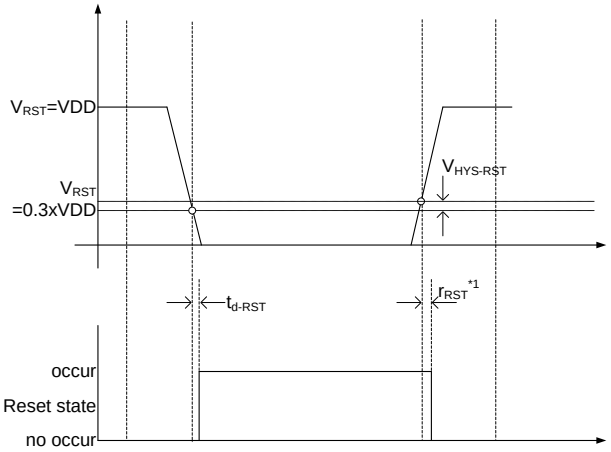


Figure 6.5-3 RST reset diagram

6.6. Power System

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.25V	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=001b		2.6		V
			LDOC [2:0]=010b		2.9		V
			LDOC [2:0]=011b		3.3		V
			LDOC [2:0]=100b		3.6		V
			LDOC [2:0]=101b		4.0		V
			LDOC [2:0]=110b		4.5		V
	Dropout voltage	I_L = 10mA	LDOC [2:0]=000b		250		mV
	Temperature drift	LDOC [2:0]=000b I_L = 0.1mA	TA=-40℃~85℃		50		PPM/℃
	VDD Voltage drift	LDOC [2:0]=000b	VDD=2.2V~5.5V		±0.2		%/V
V12	operation current, I_{V12}	ENAD1[0]=1b,	ENV12 [0]=1b		50		uA
	Internal Analog Common Mode Voltage ,V_{ACM}=V12		IL = 0uA	1.1	1.2	1.3	V
	Temperature drift	ENAD1[0]=1b,	TA=-40℃~85℃, ENV12 [0]=1b		50		PPM/℃
VDDA：Adjust Voltage Regulator							

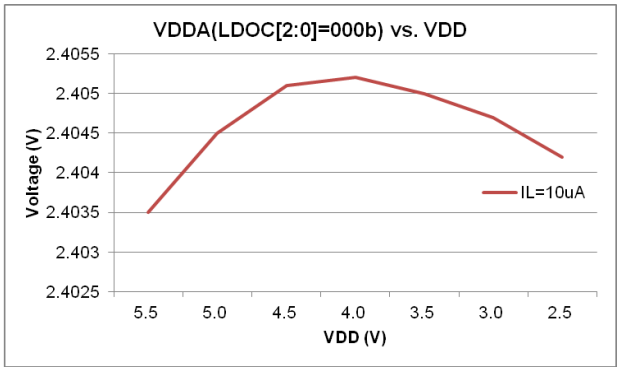


Figure 6.6-1 VDDA(000b) vs. VDD

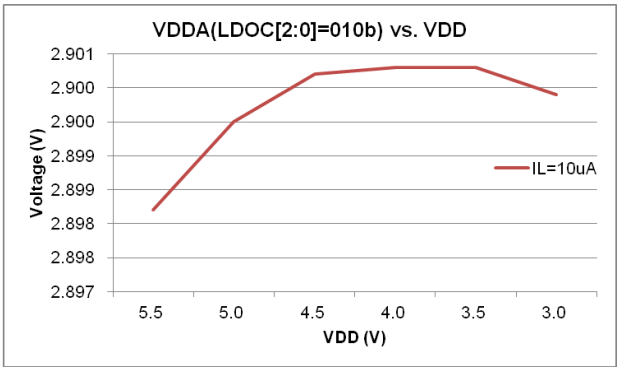


Figure 6.6-2 VDDA(010b) vs. VDD

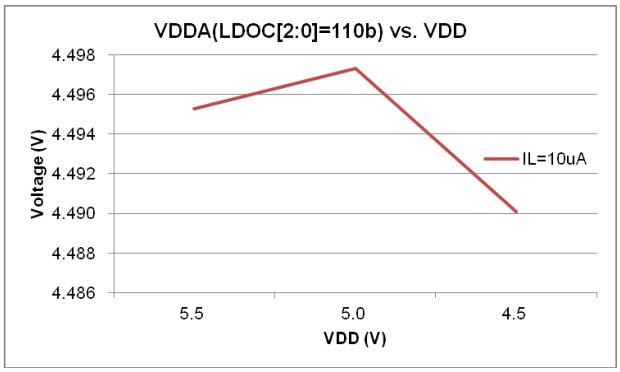


Figure 6.6-3 VDDA(110b) vs. VDD

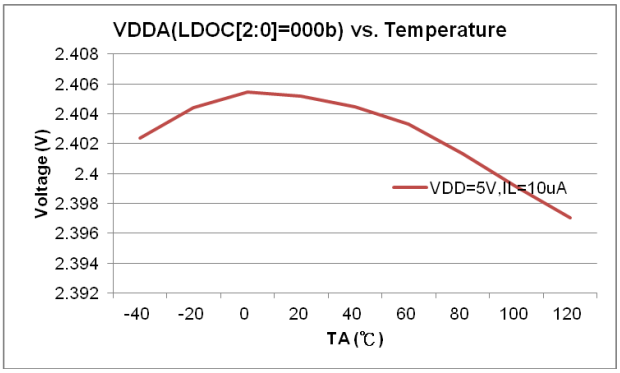


Figure 6.6-4 VDDA(000b) vs. Temperature

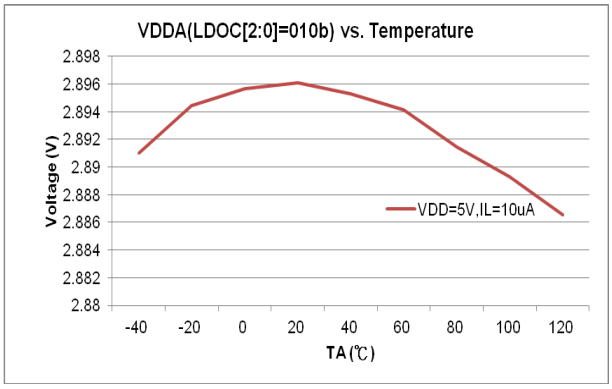


Figure 6.6-5 VDDA(010b) vs. Temperature

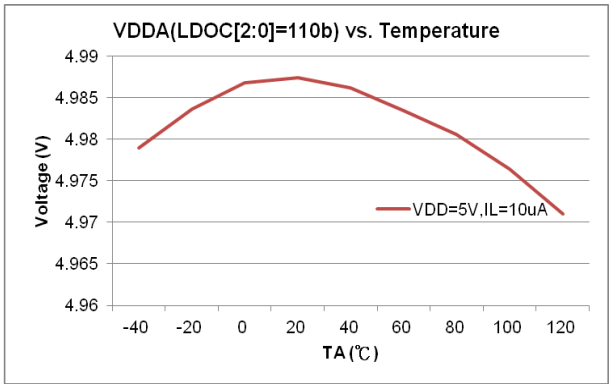


Figure 6.6-6 VDDA(110b) vs. Temperature

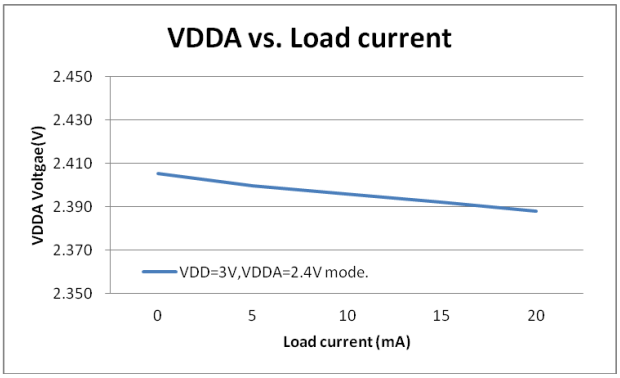


Figure 6.6-7 VDDA vs. Load current

6.7. LCD

TA = 25℃,VDD = 3.3V, CVLCD =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current with output buffer.(all segment turn on, No load)	ENLCP[0]=1	VDD = 3.0V		5		uA
VLCD	Supply Voltage at VLCD pin	ENLCP [0]=0		2.4		5	V
	Embedded Charge Pump output voltage at VLCD pin	VDD = 3.3V, ENLCP [0]=1 CVLCD =4.7uF	LCDV[2:0]=111b	-10%	2.45	+10%	V
			LCDV[2:0]=110b	-10%	2.70	+10%	
			LCDV[2:0]=101b	-10%	2.85	+10%	
			LCDV[2:0]=100b	-10%	3.10	+10%	
			LCDV[2:0]=011b	-10%	3.30	+10%	
			LCDV[2:0]=010b	-10%	4.10	+10%	
			LCDV[2:0]=001b (VDD>2.4V mode)	-10%	4.55	+10%	
			LCDV[2:0]=000b (VDD>2.75V)	-10%	5.1	+10%	
	VDD Voltage drift	ENLCP [0]=1, CVLCD =4.7uF, LCDV[2:0]>010b,VDD=2.2V ~ 5.5V; LCDV[2:0]=001b,VDD>2.4V; LCDV[2:0]=000b,VDD>2.75 V;			4		%/V
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

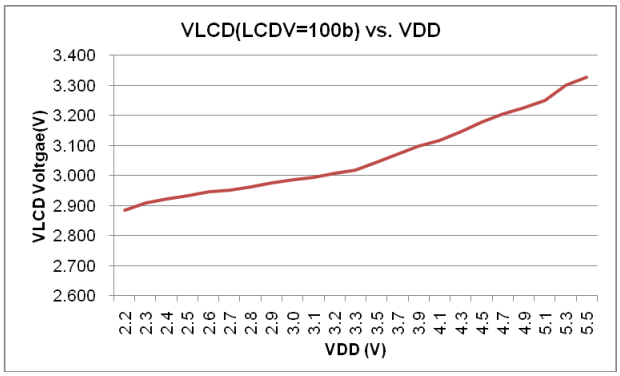


Figure6.7-1 VLCD(LCDV=100b) vs. VDD

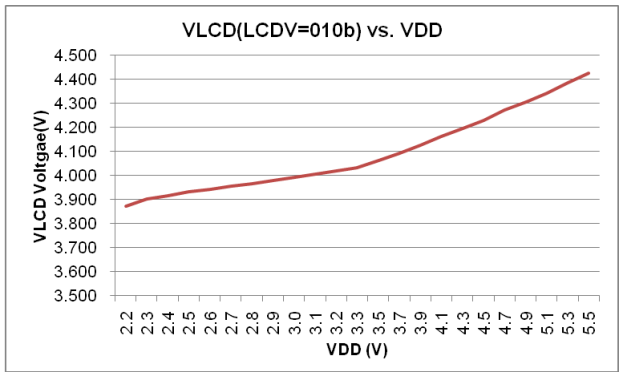


Figure6.7-2 VLCD(LCDV=010b) vs. VDD

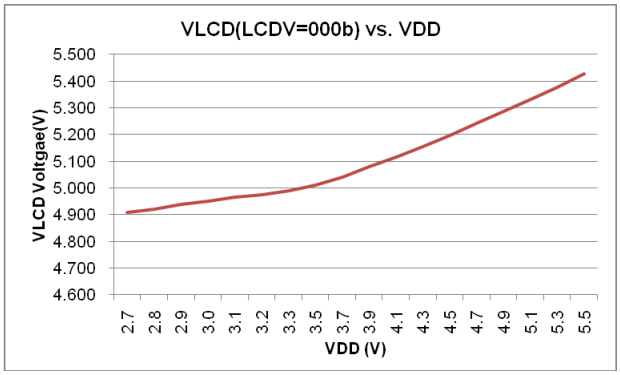


Figure6.7-3 VLCD(LCDV=000b) vs. VDD

6.8. SD18, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENLDO[0]=0		2.4		5.5	V
f_{SD18}	Modulator sample frequency, ADC_CK			115	460		KHz
	Over Sample Ratio, OSR			64		16384	
I_{SD18}	Operation supply current without PGA	ENAD1 [0]=1	GAIN =16, ADC_CK=460KHz		260		uA

6.8.1. PGA, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENLDO [0]=0		2.4		5.5	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<11>			400		uA
G_{PGA}	Gain temperature drift	TA = -40℃~ 85℃	GAIN=128		15		ppm/℃

6.8.2. SD18,performance

TA = 25℃,VDD = 3.6V, VDDA=2.4V,V_{VR}= AI2(short to VDDA)/2

GAIN=16 with PGA=8,f_{SD18}=460KHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,VVR= AI2/2, ΔSI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes3	ADC_CK=460KHz,OSR[3:0]=0000b		23			Bits
G_{SD18}	Temperature drift Gain x16	TA = -40℃~ 85℃			10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=1.2V DCSET[3:0]=<0000> *ΔAI is external short	Gain=2			1	%FSR
	Offset temperature drift with chopper without PGA		GAIN=1		2		uV/℃
			GAIN=2		1		
			GAIN=4		0.5		
			GAIN=16		0.15		
	Offset temperature drift with chopper		GAIN=128		0.02		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}= 1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
			V_{SI}=0V, GAIN=16		75		dB
PSRR	DC power supply rejection	VDDA=3.0V Δ_{VDDA}=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI}-=1.2V,	GAIN=1 PGA=off		75		dB
			GAIN=16 PGA=8				dB

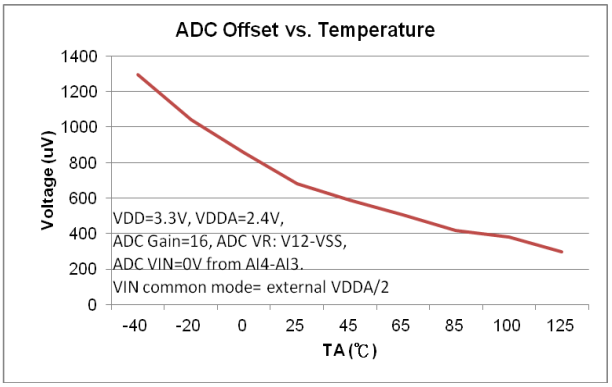


Figure 6.8-1 ADC Offset drift with Temperature

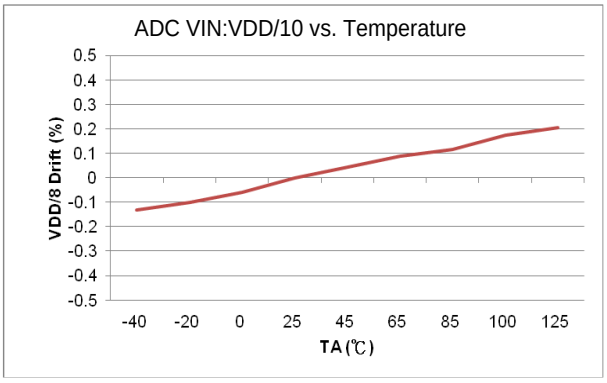


Figure 6.8-2 VDD/10 drift with Temperature

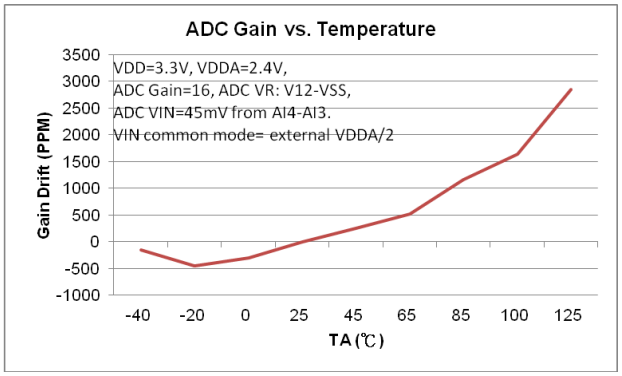


Figure 6.8-3 ADC Gain drift with Temperature

6.8.3. SD18 Noise Performance

HY17P56 针对 SD18 提供了重要的输入噪声规格。下表列出典型的噪声规格表与 Gain, Output rate，及差动最大输入电压等关系。取样 1024 笔资料。

ENOB(RMS) with OSR/GAIN at A/D Clock=460KHz, VDD=3.6V, VDDA=2.4V, VREF=SDR/2=1.2V														
Max Vin(mV) =0.9*VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384
	Output rate(Hz)					7188	3594	1797	898	449	225	112	56	28
	Gain	=	PGAGN	x	ADGN									
±2160	0.25	=	off	x	0.25	14.57	15.06	15.56	16.03	16.56	16.94	17.38	17.84	18.36
±2160	0.5	=	off	x	0.5	14.62	15.03	15.54	16.04	16.47	16.84	17.34	17.87	18.32
±1080	1	=	off	x	1	14.62	15.07	15.63	16.11	16.61	16.93	17.53	17.92	18.4
±540	2	=	off	x	2	14.5	14.99	15.47	15.9	16.47	16.82	17.32	17.87	18.3
±270	4	=	off	x	4	14.49	15.05	15.52	16.06	16.56	16.8	17.35	17.85	18.31
±135	8	=	off	x	8	14.49	14.98	15.44	16.01	16.5	16.86	17.3	17.81	18.18
±68	16	=	off	x	16	14.37	14.95	15.38	15.91	16.39	16.79	17.17	17.72	18.16
±34	32	=	2	x	16	13.39	13.9	14.37	14.88	15.41	15.79	16.31	16.75	17.28
±17	64	=	4	x	16	13.15	13.59	14.12	14.6	15.07	15.43	15.83	16.47	16.94
±8.5	128	=	8	x	16	12.65	13.22	13.76	14.11	14.55	14.94	15.32	15.96	16.42
RMS(uV) with OSR/GAIN at A/D Clock=460KHz,VDD=3.6V, VDDA=2.4V, VREF=SDR/2=1.2V														
Max Vin(mV) =0.9*VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384
	Output rate(Hz)					7188	3594	1797	898	449	225	112	56	28
	Gain	=	PGAGN	x	ADGN									
±2160	0.25	=	off	x	0.25	386.39	275.54	194.62	140.62	97.02	74.67	54.99	40.14	27.99
±2160	0.5	=	off	x	0.5	186.42	140.20	98.54	69.72	51.69	39.98	28.25	19.55	14.39
±1080	1	=	off	x	1	93.40	68.04	46.27	33.27	23.46	18.76	12.42	9.48	6.81
±540	2	=	off	x	2	50.55	36.05	25.91	19.20	12.93	10.18	7.18	4.90	3.64
±270	4	=	off	x	4	25.42	17.31	12.48	8.60	6.09	5.13	3.51	2.49	1.81
±135	8	=	off	x	8	12.74	9.07	6.60	4.44	3.18	2.47	1.81	1.28	0.99
±68	16	=	off	x	16	6.91	4.64	3.44	2.39	1.71	1.29	0.99	0.68	0.50
±34	32	=	2	x	16	6.82	4.81	3.47	2.43	1.69	1.30	0.90	0.66	0.46
±17	64	=	4	x	16	4.03	2.97	2.06	1.48	1.07	0.83	0.63	0.40	0.29
±8.5	128	=	8	x	16	2.86	1.92	1.33	1.04	0.77	0.58	0.45	0.29	0.21

(1) Max.Vin (mV) is the max. input voltage of single end to ground(VSS)

Table6.8-3(a) SD18 ENOB and RMS Noise Table at VDDA=2.4V

ENOB(RMS) with OSR/GAIN at A/D Clock=460KHz, VDD=5.5V, VDDA=5V, VREF=SDR/2=2.5V														
Max Vin(mV) =0.9*VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384
	Output rate(Hz)					7188	3594	1797	898	449	225	112	56	28
	Gain	=	PGAGN	x	ADGN									
±4500	0.25	=	off	x	0.25	14.69	15.33	15.64	16.18	16.66	16.97	17.6	18.06	18.63
±4500	0.5	=	off	x	0.5	14.69	15.29	15.81	16.34	16.81	17.17	17.66	18.13	18.66
±2250	1	=	off	x	1	14.64	15.16	15.65	16.19	16.64	17	17.47	17.96	18.5
±1125	2	=	off	x	2	14.75	15.25	15.74	16.29	16.83	17.09	17.59	18.16	18.64
±562	4	=	off	x	4	14.66	15.12	15.63	16.17	16.67	16.99	17.39	17.98	18.51
±281	8	=	off	x	8	14.67	15.19	15.76	16.13	16.75	17.12	17.51	18.02	18.58
±140	16	=	off	x	16	14.66	15.15	15.68	16.15	16.63	17	17.53	18.01	18.5
±70	32	=	2	x	16	14.11	14.59	15.13	15.61	16.01	16.3	16.88	17.36	17.97
±35	64	=	4	x	16	13.87	14.39	14.82	15.25	15.63	15.9	16.56	16.96	17.66
±17	128	=	8	x	16	13.47	13.92	14.45	14.85	15.35	15.55	15.99	16.55	16.99
RMS(uV) with OSR/GAIN at A/D Clock=460KHz,VDD=5.5V, VDDA=5V, VREF=SDR/2=2.5V														
Max Vin(mV) =0.9*VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384
	Output rate(Hz)					7188	3594	1797	898	449	225	112	56	28
	Gain	=	PGAGN	x	ADGN									
±4500	0.25	=	off	x	0.25	758.72	485.33	392.27	269.49	193.61	156.14	100.97	73.09	49.28
±4500	0.5	=	off	x	0.5	379.65	249.80	174.20	120.50	87.05	67.98	48.27	34.97	24.18
±2250	1	=	off	x	1	196.47	136.56	97.65	67.22	48.90	38.19	27.54	19.71	13.54
±1125	2	=	off	x	2	91.00	64.24	45.84	31.18	21.53	18.01	12.67	8.55	6.14
±562	4	=	off	x	4	48.34	35.26	24.75	17.04	11.99	9.64	7.30	4.83	3.36
±281	8	=	off	x	8	24.06	16.71	11.31	8.70	5.67	4.39	3.35	2.36	1.60
±140	16	=	off	x	16	12.08	8.64	5.96	4.32	3.09	2.39	1.66	1.18	0.84
±70	32	=	2	x	16	8.84	6.35	4.37	3.13	2.38	1.95	1.30	0.93	0.61
±35	64	=	4	x	16	5.23	3.65	2.70	2.01	1.55	1.28	0.81	0.61	0.38
±17	128	=	8	x	16	3.45	2.53	1.75	1.33	0.94	0.81	0.60	0.41	0.30

(1) Max.Vin (mV) is the max. input voltage of single end to ground(VSS)

Table6.8-3(b) SD18 ENOB and RMS Noise Table at VDDA=5V

ENOB(RMS) with OSR/GAIN at A/D Clock=460KHz, VDD=3.6V, VDDA=2.4V, VREF=SDR/2=1.2V at High Accuracy Mode									
Max Vin(mV) =0.9*VREF(1)	OSR					2048	4096	8192	16384
	Output rate(Hz)					112	56	28	14
	Gain	=	PGAGN	x	ADGN				
±2160	0.25	=	off	x	0.25	17.37	17.78	18.36	18.81
±2160	0.5	=	off	x	0.5	17.38	17.84	18.33	18.79
±1080	1	=	off	x	1	17.41	17.99	18.46	18.93
±540	2	=	off	x	2	17.32	17.83	18.32	18.8
±270	4	=	off	x	4	17.39	17.9	18.41	18.92
±135	8	=	off	x	8	17.35	17.8	18.41	18.83
±68	16	=	off	x	16	17.34	17.76	18.2	18.77
±34	32	=	2	x	16	16.23	16.76	17.3	17.82
±17	64	=	4	x	16	15.9	16.41	17.01	17.46
±8.5	128	=	8	x	16	15.38	15.99	16.54	16.87
RMS(uV) with OSR/GAIN at A/D Clock=460Hz, VDD=3.6V , VDDA=2.4V, VREF=SDR/2=1.2V at High Accuracy Mode									
Max Vin(mV) =0.9*VREF(1)	OSR					2048	4096	8192	16384
	Output rate(Hz)					112	56	28	14
	Gain	=	PGAGN	x	ADGN				
±2160	0.25	=	off	x	0.25	55.47	41.59	27.99	20.38
±2160	0.5	=	off	x	0.5	27.50	19.98	14.28	10.39
±1080	1	=	off	x	1	13.47	8.99	6.51	4.71
±540	2	=	off	x	2	7.18	5.03	3.58	2.57
±270	4	=	off	x	4	3.41	2.41	1.68	1.18
±135	8	=	off	x	8	1.76	1.29	0.84	0.63
±68	16	=	off	x	16	0.88	0.66	0.49	0.33
±34	32	=	2	x	16	0.96	0.66	0.45	0.32
±17	64	=	4	x	16	0.60	0.42	0.28	0.20
±8.5	128	=	8	x	16	0.43	0.28	0.19	0.15

(1) Max.Vin (mV) is the max. input voltage of single end to ground(VSS)

Table6.8-3(c) High Accuracy Mode, SD18 ENOB and RMS Noise Table at VDDA=2.4V

ENOB(RMS) with OSR/GAIN at A/D Clock=460KHz, VDD=5.5V, VDDA=5V, VREF=SDR/2=2.5V at High Accuracy Mode									
Max Vin(mV) =0.9*VREF(1)	OSR					2048	4096	8192	16384
	Output rate(Hz)					112	56	28	14
	Gain	=	PGAGN	x	ADGN				
±4500	0.25	=	off	x	0.25	17.43	18.06	18.54	19.07
±4500	0.5	=	off	x	0.5	17.59	18.16	18.67	19.15
±2250	1	=	off	x	1	17.44	17.93	18.58	19.01
±1125	2	=	off	x	2	17.61	18.13	18.65	19.12
±562	4	=	off	x	4	17.43	17.96	18.5	19.05
±281	8	=	off	x	8	17.55	18.15	18.63	19.07
±140	16	=	off	x	16	17.51	17.97	18.54	19.06
±70	32	=	2	x	16	16.92	17.31	17.93	18.48
±35	64	=	4	x	16	16.5	17.06	17.52	18.03
±17	128	=	8	x	16	16.03	16.44	16.96	17.48
RMS(uV) with OSR/GAIN at A/D Clock=460Hz, VDD=5.5V , VDDA=5V, VREF=SDR/2=2.5V at High Accuracy Mode									
Max Vin(mV) =0.9*VREF(1)	OSR					2048	4096	8192	16384
	Output rate(Hz)					112	56	28	14
	Gain	=	PGAGN	x	ADGN				
±4500	0.25	=	off	x	0.25	113.63	73.10	52.63	36.50
±4500	0.5	=	off	x	0.5	50.78	34.25	24.08	17.25
±2250	1	=	off	x	1	28.12	20.00	12.81	9.52
±1125	2	=	off	x	2	12.56	8.73	6.09	4.39
±562	4	=	off	x	4	7.10	4.92	3.38	2.30
±281	8	=	off	x	8	3.25	2.15	1.54	1.14
±140	16	=	off	x	16	1.67	1.22	0.82	0.57
±70	32	=	2	x	16	1.26	0.96	0.63	0.43
±35	64	=	4	x	16	0.84	0.57	0.42	0.29
±17	128	=	8	x	16	0.59	0.44	0.31	0.21

(1) Max.Vin (mV) is the max. input voltage of single end to ground(VSS)

Table6.8-3(d) High Accuracy Mode, SD18 ENOB and RMS Noise Table at VDDA=5V

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \frac{\ln\left(\frac{FSR}{RMS\ Noise}\right)}{\ln(2)}$$

$$RMS\ Noise = \frac{\left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right)}{2^{23}}$$

$$Where\ FSR\ (Full - Scale\ Range) = 2 \times VREF/Gain.$$

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$

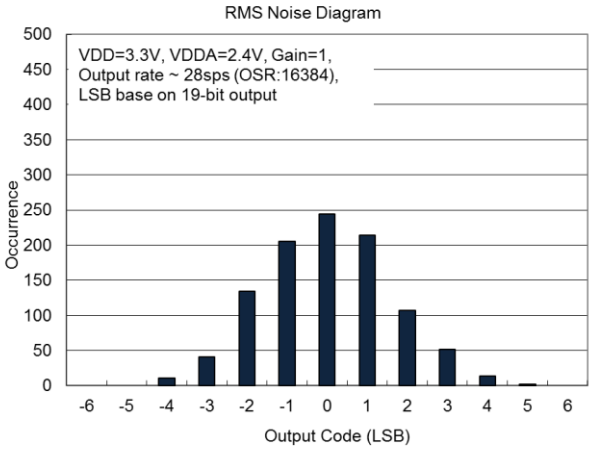


Figure 6.8-4 RMS Noise Diagram

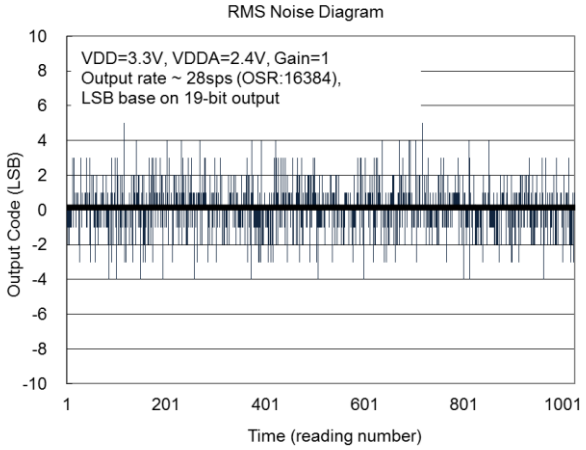


Figure 6.8-5 Output Code Diagram

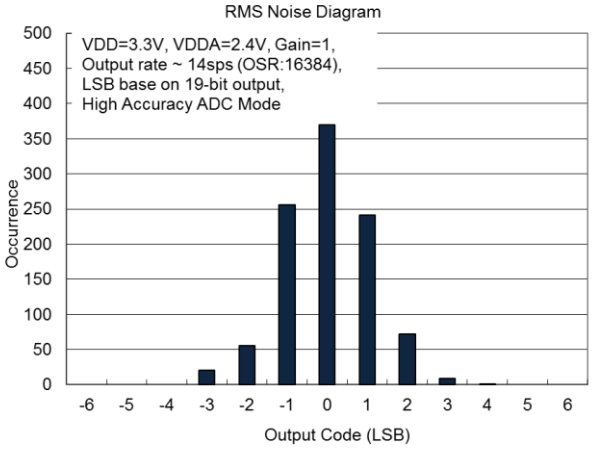


Figure 6.8-6 RMS Noise Diagram

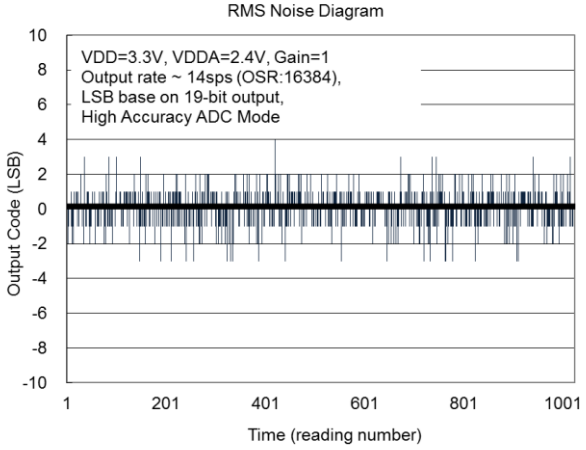


Figure 6.8-7 Output Code Diagram

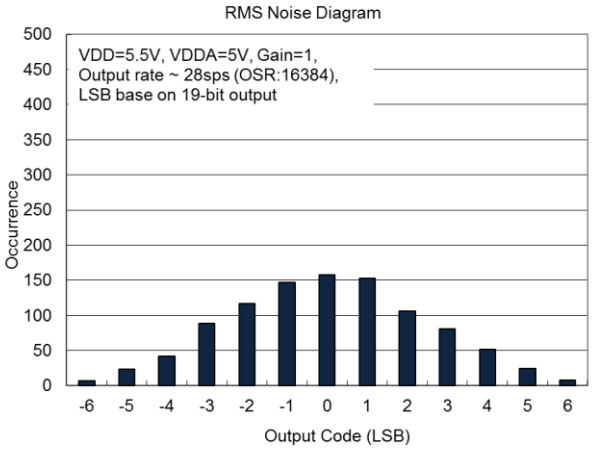


Figure 6.8-8 RMS Noise Diagram

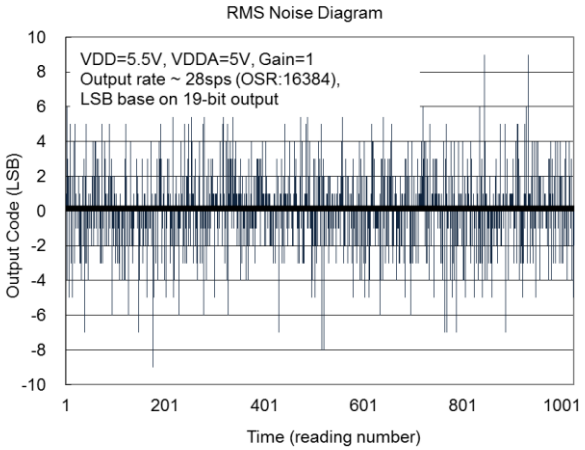


Figure 6.8-9 Output Code Diagram

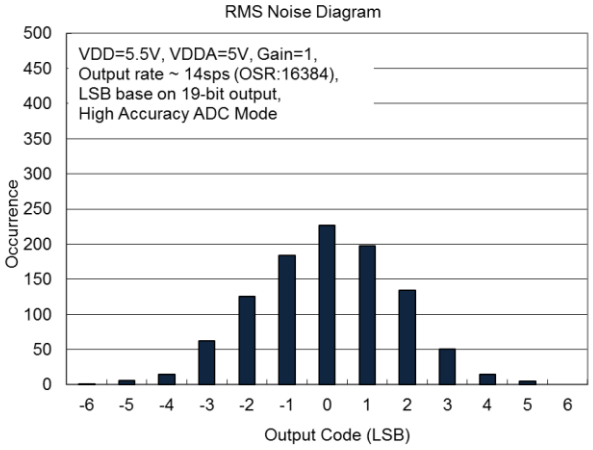


Figure 6.8-10 RMS Noise Diagram

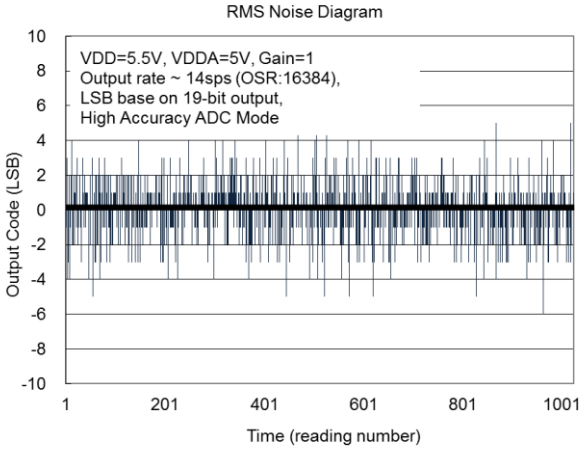


Figure 6.8-11 Output Code Diagram

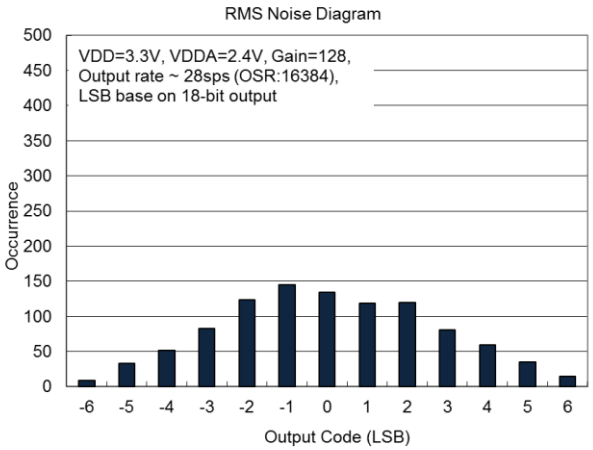


Figure 6.8-12 RMS Noise Diagram

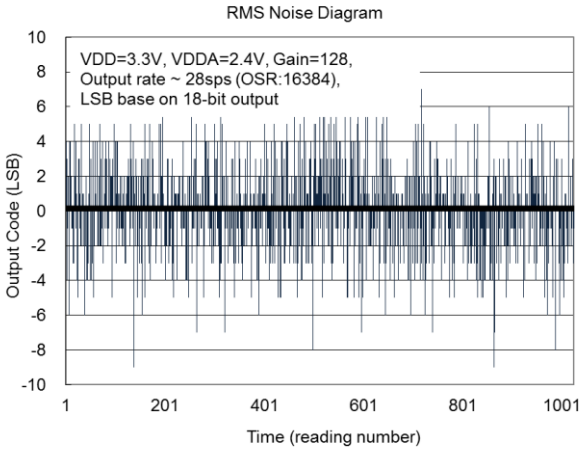


Figure 6.8-13 Output Code Diagram

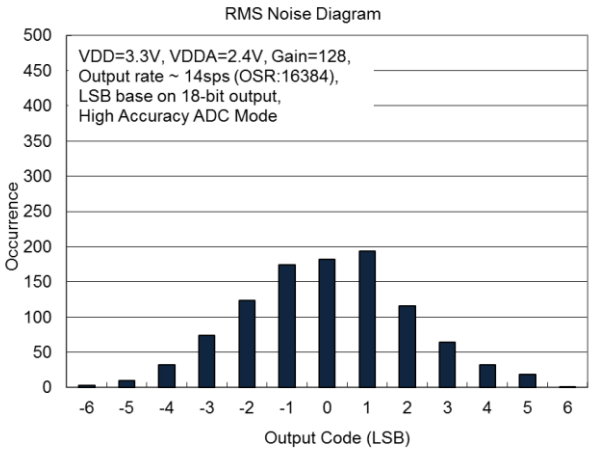


Figure 6.8-14 RMS Noise Diagram

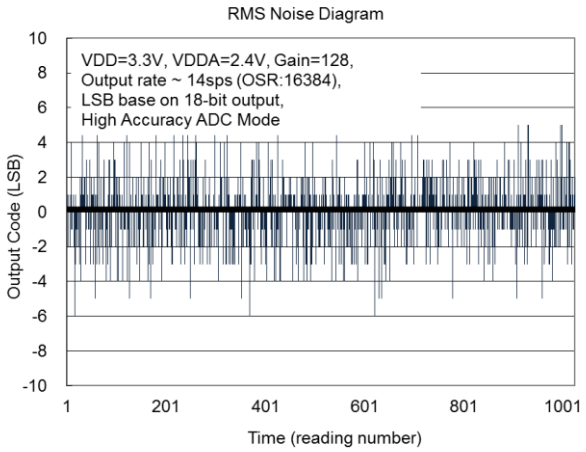


Figure 6.8-15 Output Code Diagram

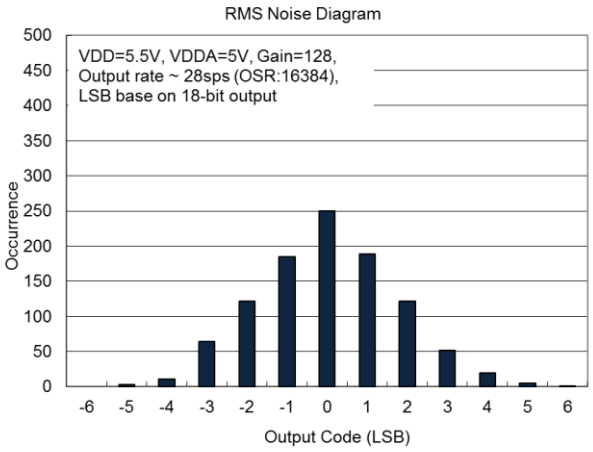


Figure 6.8-16 RMS Noise Diagram

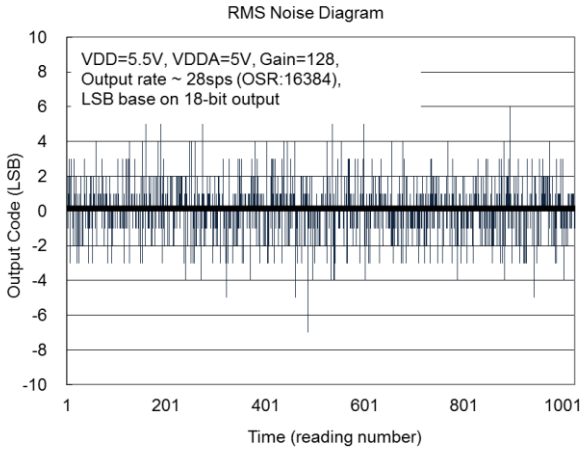


Figure 6.8-17 Output Code Diagram

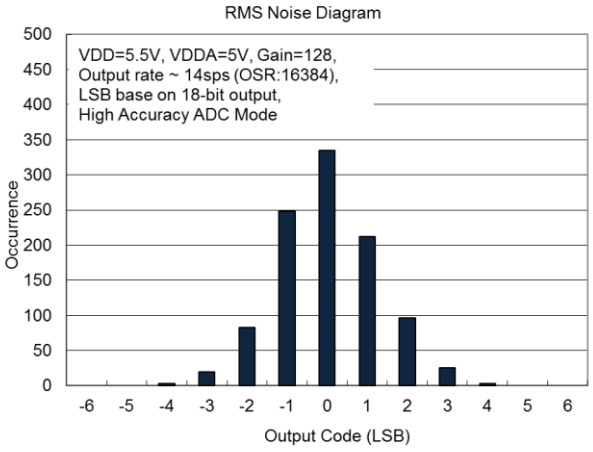


Figure 6.8-18 RMS Noise Diagram

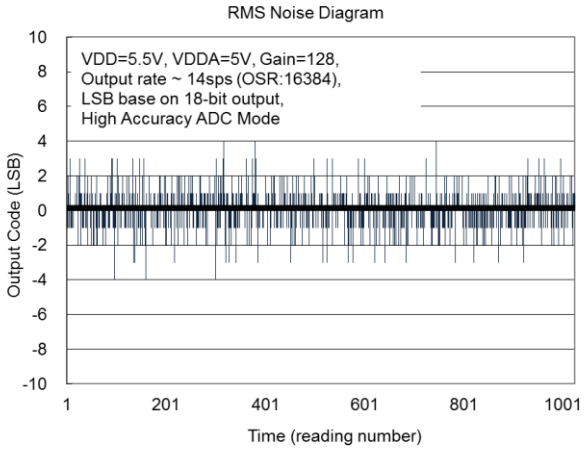


Figure 6.8-19 Output Code Diagram

6.8.4. SD18 ,Temperature Sensor

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			-284		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

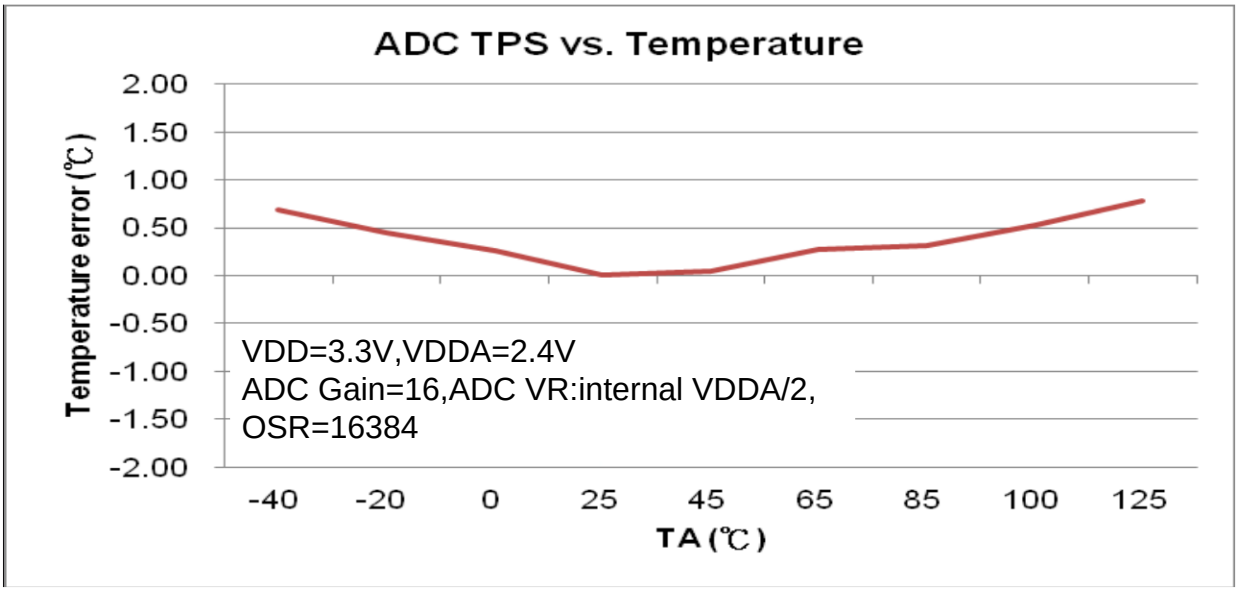


Figure 6.8-20 ADC Temperature Error

6.9. Build-In EPROM(BIE)

TA = 25℃,VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage at VPP PIN		8.5		8.75	V
I_{BIE}	Operation supply current			3		mA
V_{SS}	Supply Voltage			0		V
When connecting to the external VBIE power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.						

6.10. Build-In EPROM(BIE) Low voltage control circuit

TA = 25℃,VDD = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		2.75		5.5	V
V_{SS}	Supply Voltage			0		V
When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external VBIE power source.						

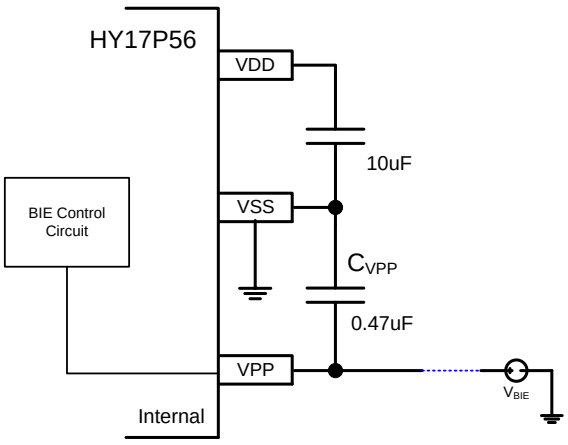


Figure 6.10-1 BIE typical application circuit

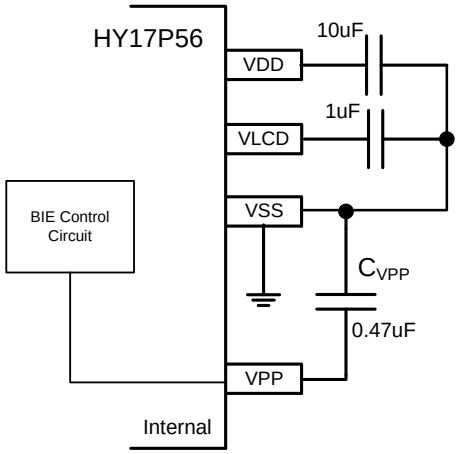


Figure 6.10-2 Use low voltage control circuit

7. 订货信息

下单品名 1	封装型式	引脚数	封装型式		程序代码	出货包装形式	个装数量	材料组成	MSL3
			描述方式		编号 2				
HY17P56-D000	Die	-	D	000	000	-	250	Green4	-
HY17P56-L048	LQFP	48	L	048	000	Tray	250	Green4	MSL-3

[1] **产品名称 – 封装型式描述方式 – 程序代码编号（空白片 / 标准品 / 代客刻录码）**

例如：您的 HY17P56 代客刻录服务申请的程序代码编号为 008，且需要的产品是裸片出货。则下单品名为 HY17P56-D000-008

例如：您的需求是 HY17P56 不带程序代码的空白片且需要的产品是裸片出货。则下单品名为 HY17P56-D000

例如：您的需求是 HY17P56 不带程序代码的空白片且需要的产品是封装片 LQFP48 出货，则下单品名为 HY17P56-L048，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的 HY17P56 代客刻录服务申请的程序代码编号为 009，而需求的产品是封装片 LQFP48 出货，则下单品名为 HY17P56-L048-009，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

[2] 程序代码编号

“001”~“999” 为标准品或代客刻录申请的程序代码编号，而空白芯片不带此码。

[3] MSL:

湿度敏感性等级系依据 IPC/JEDEC J-STD-020 的规范加以试验分级，并参考 IPC/JEDEC J-STD-033 的标准处理、包装、运输与使用。

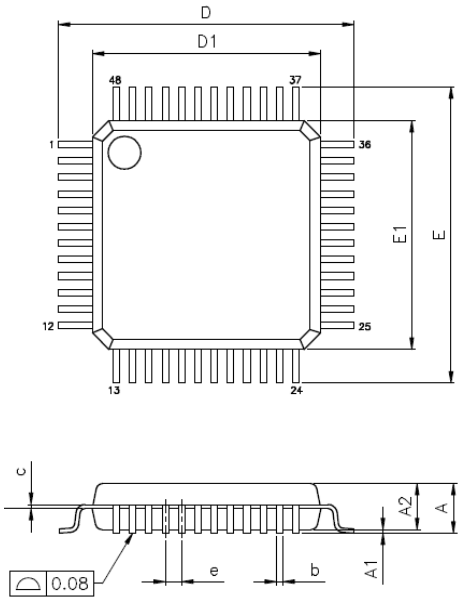
[4] Green (RoHS & no Cl/Br):

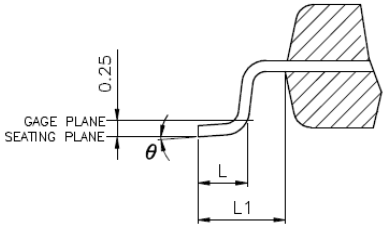
HYCON 产品皆为 Green Product，符合 RoHS 指令，REACH 高关注物质(SVHC)以及无卤素相关规定。

8. 封装型式信息

8.1. LQFP48(L048)

8.1.1. Package Dimensions





SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

9. 修订记录

以下描述本文件差异较大的地方，而标点符号与字形的改变不在此描述范围。

文件版次	页次	日期	摘要
V01	All	2018/07/12	初版发行
V02	6~11	2018/08/8	脚位说明
	12		应用电路修改
	14~16		系统频率修正
	25~27		寄存器列表
	40~44		ADC 操作频率、ENOB 表
V03	22、27	2019/10/19	修改 LCD 寄存器
	32	2020/1/7	新增外振 32768 功耗
V04	24	2020/6/2	修改 SPI 寄存器
	36	2021/1/4	增加 BOR、Reset 时序图
	25~26		修改缓存器列表，增加 INIS1、VRIS、INIS
V05	17	2021/9/11	修改 4.5 章节 BOR、Reset 时序图