HYCON TECHNOLOGY

HY3118/HY3116
Datasheet

24-Bit Analog-to-Digital Convert

High Resolution ΣΔADC

With Rail-to-Rail OPAMP

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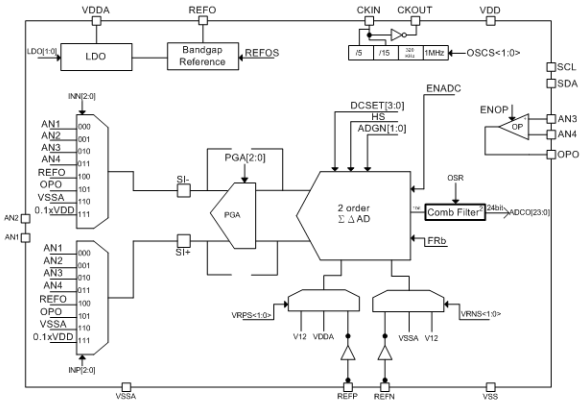
1. Features

- Sensor's pre-signal processing design
  - Equipped with 24-bitΣΔADC analog to digital converter
  - Embedded Rail-to-rail OPAMP
  - Internal VDDA with sensor drive power output of up to 10mA
  - Switchable external crystal oscillator input and high precision internal RC oscillator operating clock
  - I2C digital transmission interface
- Operation environment
  - Digital voltage: 2.2V to 3.6V
  - Analog voltage: 2.4V to 3.6V
  - Operation current:
    1. Full speed: 1050uA (excluding OPAMP)
    2. Ultra-low sleep current: 1uA
  - Operation temperature range: –40°C to +85°C
- Function block diagram



- 24-bits ΣΔADC
  - Embedded programmable preamplifier (PGA) with optional gains of: ×1, ×2, ×4, ×8, ×16, ×32, ×64, and ×128.
  - Optional data conversion output rate with upper limit of 7680Sps. 50/60Hz signal rejection at 10SPS data conversion output rate.
  - Embedded DC bias voltage design that can produce bias voltage at VREF multiples of 0, ±1/8, ±1/4, ±3/8, ±1/2, ±5/8, ±3/4, and ±7/8
  - RMS Noise:
    1. 100nV (Gain = 128) at 10 SPS output rate
    2. 37uV (Gain = 1) at 7680 SPS output rate
    3. 16 bit Noise-free resolution (Gain = 128 and VREF = 3.3V)
  - Optional input buffer for reference voltage input
  - IRQ function
- Rail-to-Rail OPAMP (HY3118 only)
  - Rail-to-rail signal input design
  - I/O current at 1mA
- Internal linear regulator VDDA and reference voltage REFO
  - Available VDDA output voltage: 2.4V, 2.7V, 3.0V or 3.3V
  - Available REFO output voltage: 1.2V or 1.5V
- I2C transmission interface:
  - Both standard and non-standard communication format
  - F_{SCL} = 400KHz
  - ADC IRQ function at non-standard mode
  - Sleep/Wake function (for register control)
- Application
  - Weight Scale
  - Strain Gauge
  - Pressure Scale
  - Industrial Process Control
- Package
  - SSOP16
  - MSOP10

Model No.	Architecture	Input Channels	ENOB (Bits)	RMS Noise	System Clock	Sample Rate(Max)	Rail-to-Rail OPAMP	DC Offset Set	Interface	Package
HY3116	Sigma-Delta	2	20	100nV (10SPS)	Int. 327kHz/1Mhz	7680SPS	NO	4 bits	IIC	MSOP10
HY3118	Sigma-Delta	4	20	100nV (10SPS)	Int. 327kHz/1Mhz Ext.4.9152MHz	7680SPS	YES	4 bits	IIC	SSOP 16

2. Product Overview

HY3118/HY3116 is a high-precision, low-noise and low power 24-bit Analog-to-Digital converter (ADC) with embedded ultra-low-noise programmable preamplifier (PGA) featuring an effective number of bits at 21bit and 100nV sub-variable signal and less than 5 ppm/℃ temperature coefficient of gain for 128 folds of gains as well as two fully differential signal input channels, one fully differential reference voltage input channels, low-noise amplifier, reference voltage input buffer, signal input channel multiplex selector, 50/60 Hz noise interference suppressible design, and zero DC bias regulator for input signal.

In addition, this chip features VDDA voltage source of high-performance and programmable output voltage, low drift internal band gap reference, optional external clock input or internal RC oscillator clock serving as operating frequency, Rail-to-rail low-noise OPAMP and I2C communication interface.

This chip can run on internal RC or external oscillator. Data conversion rate of ADC ranges from 10SPS (50/60 Hz signal interference suppression) to 7680 SPS. Power consumption rate varies with data conversion rate. Standard operation current is 1050uA while sleep current smaller than 1uA. The chip's sleep and wake mechanism employs a special register controlled by I2C communication interface.

This products series are in package format of SSOP16 and MSOP10 for different functions.

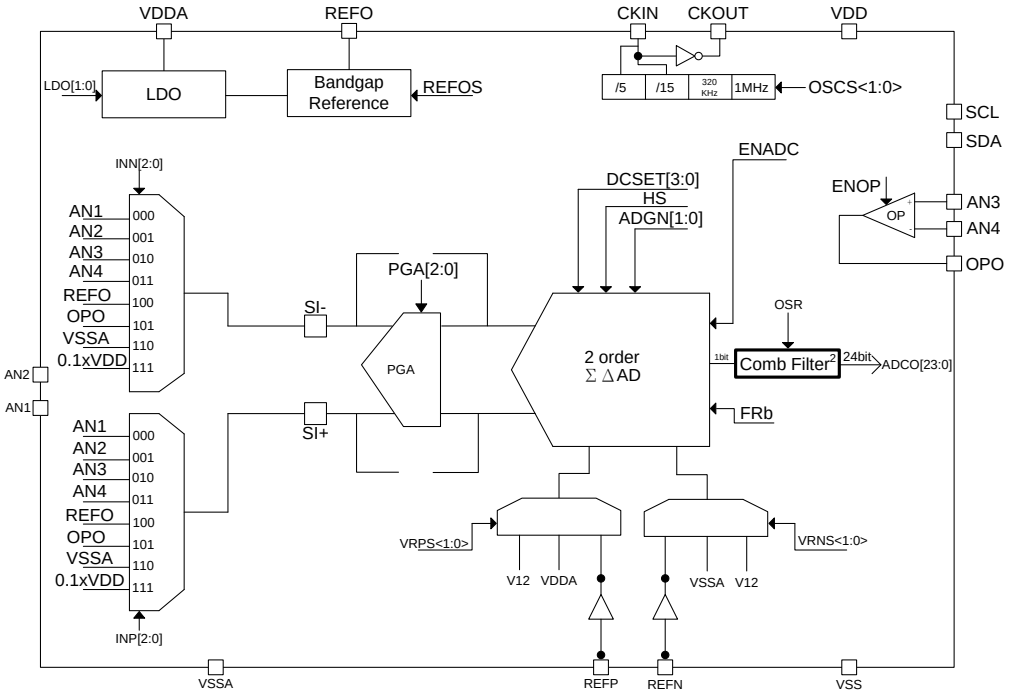


Figure 1 Function Block Diagram

3. Pin Diagram

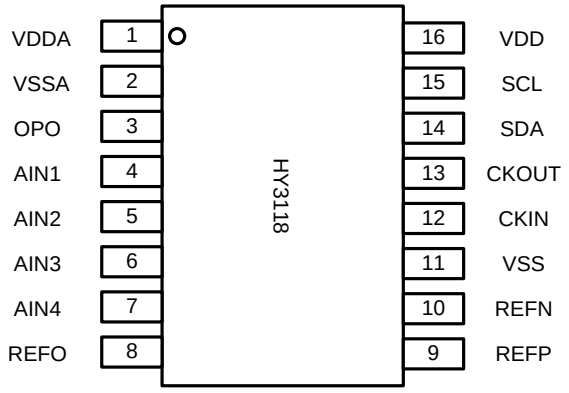


Figure 2 SSOP16 Pin Diagram

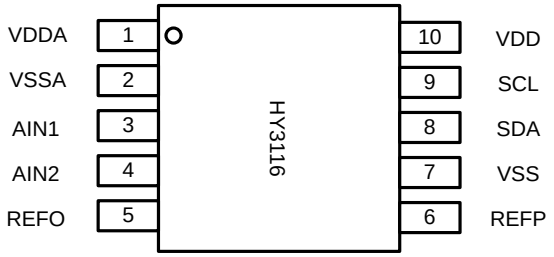


Figure 3 MSOP10 Pin Diagram

3.1. I/O Pin Definition

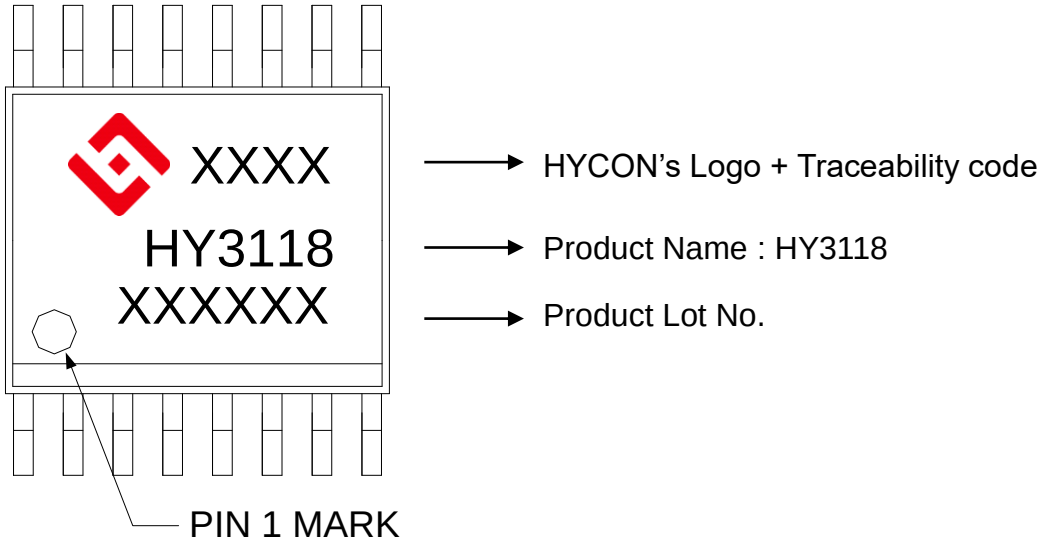
"I" input, "O" output, "S" Smith Trigger, "P" power supply, "A" analog channel

No.		Pin Name	Pin Characteristics		Function Description
SSOP16	MSOP10		Type	Buffer	
1	1	VDDA	P	P	Analog Power Supply: 2.4~3.6V
2	2	VSSA	P	P	Analog Ground
3	-	OPO	O	A	Operational Amplifier
4	3	AIN1	I	A	Analog Input1
5	4	AIN2	I	A	Analog Input2
6	-	AIN3	I	A	Analog Input3
7	-	AIN4	I	A	Analog Input4
8	5	REFO	O	A	Voltage Reference Output
9	6	REFP	I	A	Reference Input (Positive)
10	-*[1]	REFN	I	A	Reference Input (Negative)
11	7	VSS	P	P	Digital Ground
12	-	CKIN	I	A	ADC Clock Input
13	-	CKOUT	O	A	ADC Clock Output
14	8	SDA	I/O	S	I2C Data(Open-drain)
15	9	SCL	I/O	S	I2C CLK(Open-drain)
16	10	VDD	P	P	Digital Power Supply: 2.2~3.6V

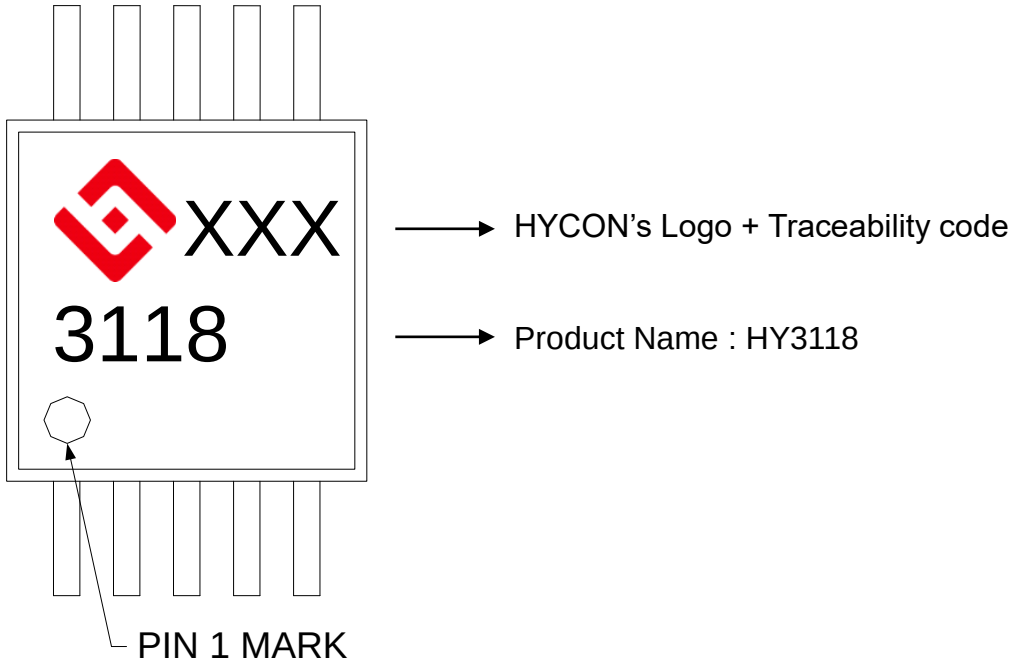
*[1] REFN and VSS were connected when packaged in MSOP10 type.

Table 1 Pin Definition and Function Description

3.1.1. SSOP package marker information



3.1.2. MSOP package marker information



4. Application Circuit

4.1. Bridge Sensor

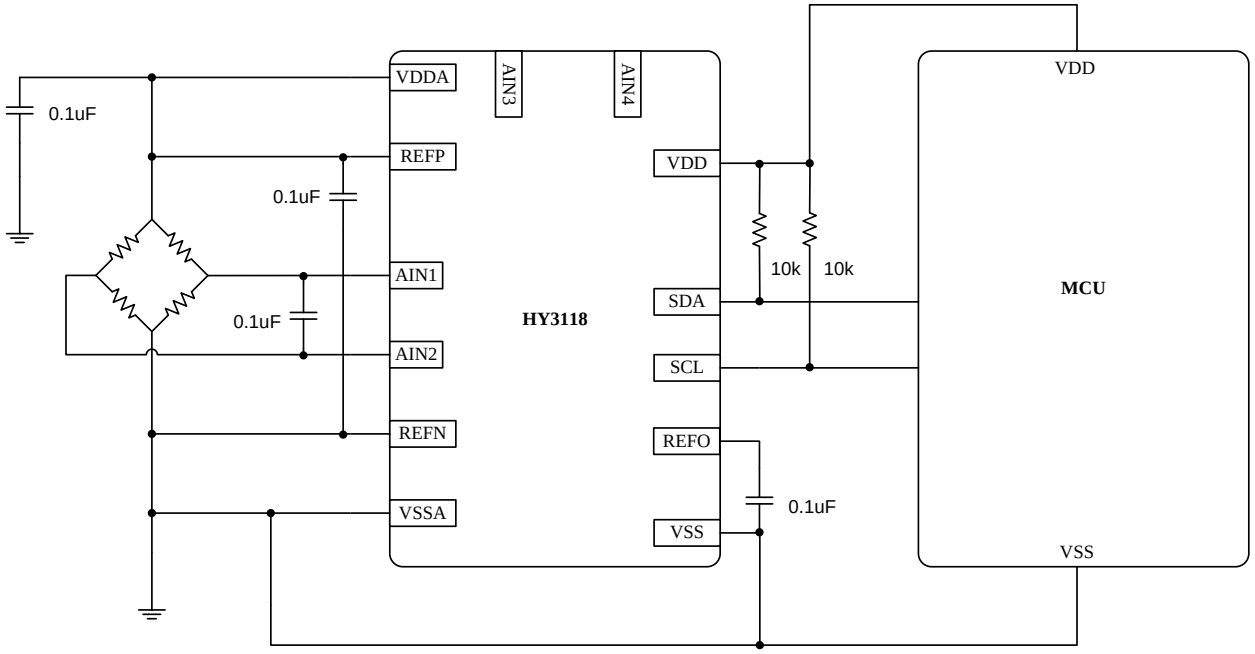


Figure 4 Application Circuit of Bridge Sensor

5. Register List

5.1. Register List

Register		Byte							
Address	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	**SYS**	-	APO	IRQEN	ENADC	ENLDO	ENREFO	ENOP	-
	Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	-
	Initial Status	-	0	0	0	0	0	0	-
01h	**ADC1**	-	-	INN[2]	INN[1]	INN[0]	INP[2]	INP[1]	INP[0]
	Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
	Initial Status	-	-	0	0	0	0	0	0
02h	**ADC2**	VRPS[1]	VRPS[0]	VRNS[1]	VRNS[0]	DCSET[3]	DCSET[2]	DCSET[1]	DCSET[0]
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Initial Status	0	0	0	0	0	0	0	0
03h	**ADC3**	OSCS[1]	OSCS[0]	FRb	PGA[2]	PGA[1]	PGA[0]	ADGN[1]	ADGN[0]
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Initial Status	0	0	0	0	0	0	0	0
04h	**ADC4**	LDO[1]	LDO[0]	REFO	HS	OSR[2]	OSR[1]	OSR[0]	-
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
	Initial Status	0	0	0	0	0	0	0	-
05h	**ADOH**	ADOH<23:16>							
	Read/Write	R	R	R	R	R	R	R	R
	Initial Status	0	0	0	0	0	0	0	0
	ADOM	ADOM<15:8>							
	Read/Write	R	R	R	R	R	R	R	R
	Initial Status	0	0	0	0	0	0	0	0
	ADOL	ADOL<7:1>							ADST
	Read/Write	R	R	R	R	R	R	R	R
	Initial Status	0	0	0	0	0	0	0	0

"-" : unused, "R/W" : read/write, "R" : read only, " ! " : keep as 0

Table 2 Register List

5.2. Register Description

5.2.1. SYS Register - System configuration control register (8bit)

Register		Byte							
Address	Name	7	6	5	4	3	2	1	0
00h	SYS	-	APO	IRQEN	ENADC	ENLDO	ENREFO	ENOP	-
	Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	-
	Initial Status	-	0	0	0	0	0	0	-

Table 3 SYS Register

APO[0] Auto Power off

<0> Disable

<1> Enable

IRQEN[0] SDA interrupt function

<0> Disable SDA interrupt function

<1> Enable SDA interrupt function

ENADC[0] ADC control

<0> Disable

<1> Enable

ENLDO[0] Enable LDO control

<0> Disable

<1> Enable

ENREFO[0] Enable REFO control

<0> Disable

<1> Enable

ENOP[0] Enable rail-to-rail OPAMP

<0> Disable

<1> Enable

5.2.2. ADC1 Register - ADC configuration control register 1(8bit) (ADC input select)

Register		Byte							
Address	Name	7	6	5	4	3	2	1	0
01h	ADC1	-	-	INN[2]	INN[1]	INN[0]	INP[2]	INP[1]	INP[0]
	Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
	Initial Status	-	-	0	0	0	0	0	0

Table 4 ADC1 Register

INN[2:0] Negative input voltage selection

<000> AIN1

<001> AIN2

<010> AIN3

<011> AIN4

<100> REFO

<101> OPO

<110> VSSA

<111> 0.1xVDD

INP[2:0] Positive input voltage selection

<000> AIN1

<001> AIN2

<010> AIN3

<011> AIN4

<100> REFO

<101> OPO

<110> VSSA

<111> 0.1xVDD

5.2.3. ADC2 Register - ADC configuration control register 2 (8bit)

Register		Byte							
Address	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
02h	**ADC2**	VRPS[1]	VRPS[0]	VRNS[1]	VRNS[0]	DCSET[3]	DCSET[2]	DCSET[1]	DCSET[0]
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Initial Status	0	0	0	0	0	0	0	0

Table 5 ADC2 Register

VRPS[1:0] Positive reference voltage selection

<00> Vrefp (Unbuffered)

<01> VDDA

<10> Vrefp (buffered)

<11> Internal reference voltage V12

VRNS[1:0] Negative reference voltage selection

<00> Vrefn (Unbuffered)

<01> VSSA

<10> Vrefn (buffered)

<11> Internal reference voltage V12

DCSET[3:0] DC offset input voltage selection

(VREF = REFP-REFN)

<0000> 0 VREF

<0001> +1/8 VREF

<0010> +1/4 VREF

<0011> +3/8 VREF

<0100> +1/2 VREF

<0101> +5/8 VREF

<0110> +3/4 VREF

<0111> +7/8 VREF

<1000> 0 VREF

<1001> -1/8 VREF

<1010> -1/4 VREF

<1011> -3/8 VREF

<1100> -1/2 VREF

<1101> -5/8 VREF

<1110> -3/4 VREF

<1111> -7/8 VREF

5.2.4. ADC3 Register - ADC configuration control register 3(8bit)

Register		Byte							
Address	Name	7	6	5	4	3	2	1	0
03h	ADC3	OSCS[1]	OSCS[0]	FRb	PGA[2]	PGA[1]	PGA[0]	ADGN[1]	ADGN[0]
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Initial Status	0	0	0	0	0	0	0	0

Table 6 ADC3 Register

OSCS[1:0] Oscillator source select

<00> Internal oscillator 327KHz

<01> Internal oscillator 1000KHz

<10> External oscillator divider by 15

<11> External oscillator divider by 5

FRb [0] Full reference range select

<0> Full reference range input

<1> 1/2 reference range input

PGA[2:0] Input signal gain for modulator

<000> PGA Disable

<001> Gain = 8

<010> Reservations

<011> Gain = 16

<100> Reservations

<101> Reservations

<110> Reservations

<111> Gain = 32

ADGN[1:0] Input signal gain for modulator

<00> Gain = 1

<01> Gain = 2

<10> Reservations

<11> Gain = 4

5.2.5. ADC4 Register - ADC configuration control register 3(8bit)

Register		Byte							
Address	Name	7	6	5	4	3	2	1	0
04h	ADC4	LDO[1]	LDO[0]	REFO	HS	OSR[2]	OSR[1]	OSR[0]	-
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
	Initial Status	0	0	0	0	0	0	0	-

Table 7 ADC4 Register

LDO[1:0] LDO output voltage selection

<00> 3.3V

<01> 3.0V

<10> 2.7V

<11> 2.4V

REFO[0] Reference voltage selection

<0> REFO= 1.2V

<1> REFO = 1.5V

HS[0] High conversion rate

<0> Slow sampling rate (327KHz)

<1> High sampling rate (1000K Hz)

OSR[2:0] ADC output rate select

<000> 2560sps / 7680sps (128)

<001> 1280sps / 3840sps (256)

<010> 640sps / 1920sps (512)

<011> 320sps / 960sps (1024)

<100> 160sps / 480sps (2048)

<101> 80sps / 240sps (4096)

<110> 40sps / 120sps (8192)

<111> 10sps / 30sps (32768)

5.2.6. ADO Register - ADC Output Code(24bit)

Register		Byte							
Address	Name	7	6	5	4	3	2	1	0
05h	ADOH	ADOH<23:16>							
	Read/Write	R	R	R	R	R	R	R	R
	Initial Status	0	0	0	0	0	0	0	0
	ADOM	ADOM<15:8>							
	Read/Write	R	R	R	R	R	R	R	R
	Initial Status	0	0	0	0	0	0	0	0
	ADOL	ADOL<7:1>							ADST
	Read/Write	R	R	R	R	R	R	R	R
	Initial Status	0	0	0	0	0	0	0	0

Table 8 ADO Register

ADO[23:1] ADC output Code

ADOH[7:0] ADC output Code of ADO[23:16]

ADOM[7:0] ADC output Code of ADO[15:8]

ADOL[7:1] ADC output Code of ADO[7:1]

ADST[0] ADC output Code Status

<0> Information has been read

<1> Information is not read

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Description	HY3118/HY3116	UNIT
VDD to VSS	–0.3 to +3.6	V
VDD to VSSA	–0.3 to +3.6	V
VSSA to VSS	–0.3 to +0.3	V
Input Current	100, Momentary	mA
	10, Continuous	mA
Analog Input Voltage to VSSA	–0.3 to VDDA + 0.3	V
Digital Input Voltage to VSS	–0.3 to VDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–60 to +150	°C

Table 9a Electrical Characteristics

6.2. Electrical Characteristics

All specifications at T_A = –40°C to +85°C, VDDA = VDD = REFP = +3V, REFN = VSSA, and PGA*Gain=128, unless otherwise noted.

PARAMETER	CONDITIONS		HY3118/HY3116 MIN	HY3118/HY3116 TYP	HY3118/HY3116 MAX	UNIT
Analog Inputs						
Full-Scale Input Voltage (VINP – VINN)	VREF =VDDA,			±0.5*VREF/(PGA*Gain)		V
Full-Scale Input Voltage (VINP – VINN)	VDDA=3.3V, VREF =1V,			±0.9*VREF/(PGA*Gain)		V
Negative Signal Input (VINN)			VSSA-0.1		VDDA	V
Positive Signal Input (VINP)			VSSA-0.1		VDDA	V
Common-Mode Input Range			VSSA-0.1		VDDA	V
System Performance						
Resolution	No Missing Codes			23		Bits
Data Rate	Internal oscillator 1000KHz, OSR=32768, HS[0]=1b			30		SPS
	Internal oscillator 327KHz, OSR=32768, , HS[0]=0b			10		SPS
	External Oscillator (1) , HS[0]=1b, Speed=High			f_{CLK}/61440		SPS
	External Oscillator (1) , HS[0]=0b, Speed=Low			f_{CLK}/491520		SPS
Digital Filter Settling Time	Full Settling			4		Conversions
Integral Nonlinearity (INL)	Differential Input, End-Point Fit, G = 1, VIN=0.9*VR, delta VR~1.2V			±30	±100	ppm
Input Offset Error	Gain=1,			±50		ppm of FS
	Gain=128,			±3		ppm of FS
Input Offset Drift	Gain=1			2		uV/°C
	Gain=128,			20		nV/°C
Gain Drift	Reference Buffer off, Input common voltage=VDDA/2			5		
	Reference Buffer on, Input common voltage=VDDA/2			50		ppm/°C
Normal-Mode Rejection	fIN = 50Hz or 60Hz ±1Hz, fDATA = 10SPS	Internal Oscillator		90		dB
		External Oscillator(1)		90		dB

Common-Mode Rejection	at DC, Input Voltage=VDDA/2± 0.1V		75	dB
Input-Referred Noise	fDATA = 10SPS , Gain=128,		100	nV, rms
	fDATA = 7680SPS , Gain=1,		3700	nV, rms
Power-Supply Rejection	at DC,VDDA=3V±0.1V, Gain=1		60	dB
	at DC,VDDA=3V±0.1V, Gain=128		95	dB
Voltage Reference Input				
Voltage Reference Input (VREF)	VREF = REFP – REFN		VDDA	V
Negative Reference Input (REFN)			VSS-0.1 ~ VDDA/2	V
Positive Reference Input (REFP)			VDDA/2 ~ VDDA+0.1	V
Voltage Reference Input Current	Input buffer on		10	nA
Power System				
VDDA operation current	I_L = 0mA, ENLDO[0]=1b, LDO[1:0]=00b		45	uA
VDDA output voltage	I_L = 0.1mA, ENLDO[0]=1b, VDD≧ VDDA+0.2V	LDO[1:0]=00b	3.3	V
		LDO[1:0]=01b	3.0	V
		LDO[1:0]=10b	2.7	V
		LDO[1:0]=11b	2.4	V
VDDA Dropout voltage	I_L = 10mA, ENLDO[0]=1b,	LDO[1:0]=00b	130	mV
		LDO[1:0]=01b	140	mV
		LDO[1:0]=10b	155	mV
		LDO[1:0]=11b	175	mV
VDDA temperature drift	I_L = 0.1mA, ENLDO[0]=1b, LDO[1:0]=11b	T_A=-40℃~85℃	50	PPM/℃
VDDA voltgage drift	I_L = 0.1mA, ENLDO[0]=1b, LDO[1:0]=11b	VDD=2.5V~3.6V	±0.2	%/V
REFO operation current	I_L = 0mA, ENREFO[0]=1b, REFO[0]=1b		45	uA
REFO output voltage, V_{REFO}	I_L = 10uA, ENREFO[0]=1b	REFO[0]=0b	1.2	V
		REFO[0]=1b	1.5	V
REFO output voltage with load	I_L = ±200uA, ENREFO[0]=1b		0.98 ~ 1.02	V_{REFO}
REFO temperature drift	I_L = 10uA,	T_A=-40℃~85℃	50	PPM/℃

		ENREFO[0]=1b				
REFO voltgage drift		I_L = 10uA, ENREFO[0]=1b	VDDA=2.4V~3.6V		100	uV/V
Internal RC Oscillator						
Low speed oscillator frequency		Internal oscillator, 327KHz, TA=25℃		290	327 360	KHz
Low speed oscillator Voltage drift		VDD=2.2V~3.6V			0.5	%
Low speed oscillator temperature drift		TA=-40℃~85℃			2	%
High speed oscillator frequency		Internal oscillator, 1000KHz, TA=25℃		900	1000 1100	KHz
High speed oscillator Voltage drift		VDD=2.2V~3.6V			1	%
High speed oscillator temperature drift		TA=-40℃~85℃			2	%
Digital						
Logic Levels	VIH	Digital inputs_SCL		0.7 VDD	VDD + 0.1	V
		Digital inputs_S		0.7 VDD	3.7	V
	VIL			VSS	0.2 VSS	V
	VOH	IOH = 1mA		VDD – 0.4		V
	VOL	IOL = 1mA			0.2 VDD	V
Input Leakage		0 < VIN < VDD			0.1	nA
External Clock Input Frequency (f_{CLKIN})					4.9152	MHz
Serial Clock Input Frequency (f_{SCLK})					5	MHz
(1). HY3116 does not support external oscillator function.						

Table 9b Electrical Characteristics

All specifications at VDD=3.6V, internal VDDA, Internal Oscillator enable, unless otherwise noted.						
PARAMETER	**CONDITIONS**		**HY3118/HY3116**			**UNIT**
			MIN	**TYP**	**MAX**	
Power Supply						
Power-Supply Voltage (VDDA, VDD)			2.4		3.6	V
Analog Supply Current I, Internal oscillator 327KHz, OSR=32768, HS[0]=0b, fDATA = 10SPS	VDDA=2.4V, Gain=1			180		μA
	VDDA=2.4V, Gain=128			530		μA
	VDDA=3.0V, Gain=1			260		μA
	VDDA=3.0V, Gain=128			550		μA
	VDDA=3.3V, Gain=1			270		μA
	VDDA=3.3V, Gain=128			570		μA
	Reference input buffer (VRPS[1:0]=VRNS[1:0]=10b)			30		μA
Analog Supply Current II, Internal oscillator 1000KHz, OSR=32768, HS[0]=1b, fDATA = 30SPS	VDDA=2.4V, Gain=1			440		μA
	VDDA=2.4V, Gain=128			1110		μA
	VDDA=3.0V, Gain=1			450		μA
	VDDA=3.0V, Gain=128			1150		μA
	VDDA=3.3V, Gain=1			460		μA
	VDDA=3.3V, Gain=128			1180		μA
Analog Supply Current III, External Oscillator 4.9152MHz, OSR=32768, HS[0]=0b, fDATA = 10SPS	VDDA=2.4V, Gain=1			270		μA
	VDDA=2.4V, Gain=128			630		μA
	VDDA=3.0V, Gain=1			276		μA
	VDDA=3.0V, Gain=128			650		μA
	VDDA=3.3V, Gain=1			280		μA
	VDDA=3.3V, Gain=128			670		μA
Analog Supply Current IV, External Oscillator 4.9152MHz, OSR=32768, HS[0]=1b, fDATA = 30SPS	VDDA=2.4V, Gain=1			520		μA
	VDDA=2.4V, Gain=128			1150		μA
	VDDA=3.0V, Gain=1			560		μA
	VDDA=3.0V, Gain=128			1215		μA
	VDDA=3.3V, Gain=1			570		μA
	VDDA=3.3V, Gain=128			1240		μA
Power down current	ENLDO[0]=ENADC[0]= ENOP[0]=0b,	VDD = 2.4V		0.6		μA
		VDD = 3.6V		0.75		μA

Table 9c Electrical Characteristics

6.3. OPAMP, Electrical Specification

All specifications at VDD=3V, internal VDDA, Internal Oscillator enable, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
VDDA	Power supply		2.4		3.6	V
V_{OUT}	Output range		0		VDDA	V
VINC	Input common range		0		VDDA	V
I_{OA}	OA current	Each OA		70		μA
I_{OA_LOAD}	Output current loading (push or pull)	VDDA = 3.0V, 0.3V < Output voltage < VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V < Output voltage < VDDA-0.3V			0.5	mA
C_{LOAD}	Max output capacitor load				1000	pF
R_{FB}	Reference input resistance			5K		Ω
R_{SW}	Switch turn on resistance				300	Ω
SR	ADC input clock	Loading R=10K, C=100pF		0.6		V/ms
G_{OPEN}	Open loop gain	Loading C=100pF		100		dB
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
PM	Phase margin	Loading C=100pF		68		Deg
GM	Gain margin			18		dB
NVIN	AINx Input refer noise	Vin= 1.2V, 1KHz		220		nV/√Hz
		Vin= 1.2V, 10KHz		75		nV/√Hz
V_{OS}	Offset error				±25	mV
PSRR	Power supply rejection ratio	Vout=1.2V, ΔVDD = 100mV, at DC		70		dB
CMRR	Common mode rejection ratio	Vout=1.2V, ΔVIN= 100mV, at DC		70		dB

7. ENOB and Noise-Free

Table 10 points out the relations between typical noise performance, gain and data rate. Test conditions are configured as DD=3.3V, VDDA=3.0V, difference of reference voltage of ADC=VDDA/2, ADC equivalent input impedance=1K load cell short and sampling 1024 data records.

ΣΔADC Noise Performance with Output rate/GAIN at VDDA=3.0V, VREF=1.5V										
Output rate (sps)	**Max. Vin(mV) =0.9*VREF (1)**	**Gain**	**=**	**PGA**	**×**	**ADGN**	ENOB (RMS Bit)	RMS Noise (nV)	Noise Free (Bit)	PEAK-TO-PEAK Noise (nV)
10	**±1350**	**1**	**=**	**1**	**×**	**1**	20.26	2389	17.54	15699
	±675	**2**	**=**	**1**	**×**	**2**	20.20	1246	17.56	7810
	±338	**4**	**=**	**1**	**×**	**4**	20.05	690	17.33	4594
	±169	**8**	**=**	**8**	**×**	**1**	20.04	347	17.29	2345
	±42	**32**	**=**	**32**	**×**	**1**	19.59	120	16.80	829
	±21	**64**	**=**	**32**	**×**	**2**	18.79	105	16.00	729
	±11	**128**	**=**	**32**	**×**	**4**	17.82	100	15.23	619
80	**±1350**	**1**	**=**	**1**	**×**	**1**	18.70	7045	15.96	47382
	±675	**2**	**=**	**1**	**×**	**2**	18.73	3439	16.02	22550
	±338	**4**	**=**	**1**	**×**	**4**	18.54	1960	15.92	12163
	±169	**8**	**=**	**8**	**×**	**1**	18.50	1009	15.81	6518
	±42	**32**	**=**	**32**	**×**	**1**	18.19	312	15.47	2069
	±21	**64**	**=**	**32**	**×**	**2**	17.42	267	14.78	1665
	±11	**128**	**=**	**32**	**×**	**4**	16.55	245	13.89	1554
2560	**±1350**	**1**	**=**	**1**	**×**	**1**	16.22	39153	13.48	262213
	±675	**2**	**=**	**1**	**×**	**2**	16.11	21075	13.38	140432
	±338	**4**	**=**	**1**	**×**	**4**	15.99	11539	13.30	74202
	±169	**8**	**=**	**8**	**×**	**1**	16.01	5664	13.25	38456
	±42	**32**	**=**	**32**	**×**	**1**	15.66	1810	12.93	12057
	±21	**64**	**=**	**32**	**×**	**2**	14.95	1474	12.23	9772
	±11	**128**	**=**	**32**	**×**	**4**	14.08	1352	11.40	8694
7680	**±1350**	**1**	**=**	**1**	**×**	**1**	16.31	36854	13.57	247636
	±675	**2**	**=**	**1**	**×**	**2**	16.18	20172	13.51	128579
	±338	**4**	**=**	**1**	**×**	**4**	16.07	10915	13.31	73940
	±169	**8**	**=**	**8**	**×**	**1**	16.10	5332	13.36	35838
	±42	**32**	**=**	**32**	**×**	**1**	15.76	1685	12.95	11822
	±21	**64**	**=**	**32**	**×**	**2**	15.01	1416	12.27	9466
	±11	**128**	**=**	**32**	**×**	**4**	14.07	1363	11.35	8969

(1) Max.Vin (mV) is the max. input voltage of single end to analog ground (AVSS).

Table 10 ΣΔADC Noise Performance Table

The RMS Noise and Peak-to-Peak noise are referred to the noise generated from the chip itself at the input end. RMS Noise is ADC input noise and the Peak-to-Peak noise referring in this spec is the deviation of maximum and minimum noise of 1000 records (±3.3 standard deviation).

$$\text{ENOB} = \frac{In\frac{\text{FSR}}{\text{RMS Noise}}}{In2} \qquad \text{Noise - Free Bits} = \frac{In\frac{\text{FSR}}{\text{Peak-to-Peak Noise}}}{In2}$$

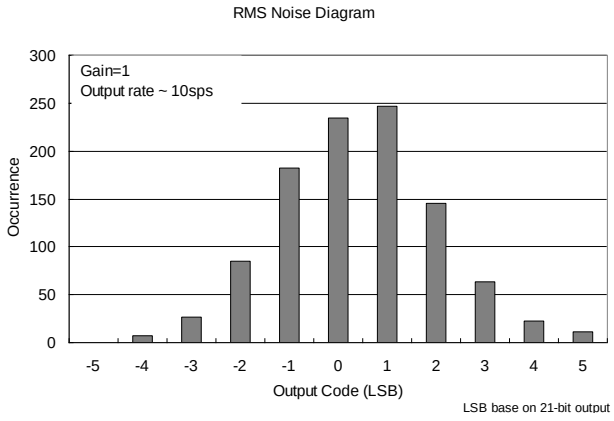


Figure 5 RMS Noise Diagram

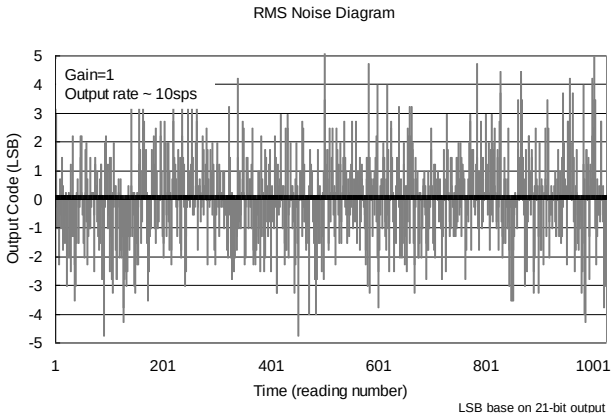


Figure 6 Output Code Diagram

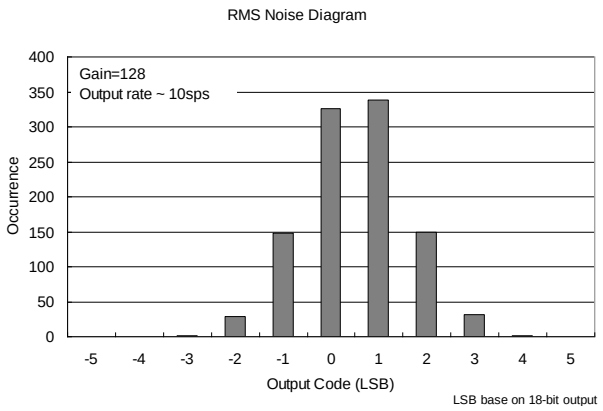


Figure 7 RMS Noise Diagram

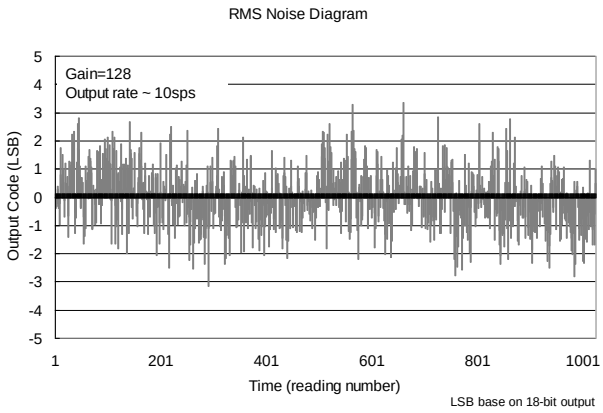


Figure 8 Output Code Diagram

8. I²C Communication Protocol

- ADC IRQ vector support
- Dual lines communication interface
- f_{SCL} = 400KHz
- Address definition: 0xA0h
- Low power consumption communication interface

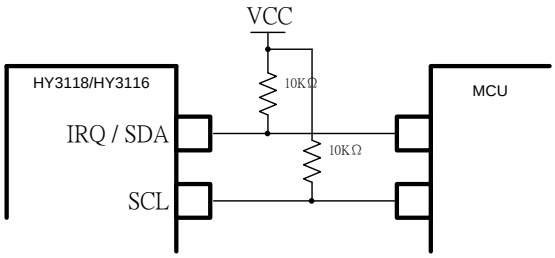


Figure 9 Communication Interface Connection Diagram

Chip's communication mechanism employs flexible I²C structure that allows with- or without-IRQ notice after completion of ADC conversion for different applications. In case of communication protocol without IRQ notice the time for retrieving the end of ADC conversion must be measured by users manually. For protocol with IRQ notice, an IRQ pulse signal will be given after ADC conversion.

IRQ pulse signal is generated by I²C's SDA communication PIN. When set at this mode the SDA pin is at high potential caused by external pull-up resistor after end of data transmission and generates a low potential pulse signal after ADC conversion as a notice to chip users. Current consumption for SDA at low potential is measured by pull-up resistance and VCC voltage.

In an IRQ not initiated mode, users determine whether the ADC output data has been read by reading the status data of the ADO [ADST] buffer and the ADO [ADST] status will update at the time of ADO buffer reading. As a result, when IRQ is inactive the ADC output data and the ADO [ADST] status remain intact when the ADC interrupts at the time of ADO buffer reading.

Chip address is fixed at 0xA0h, that is, device address [6:0] = 1010000b.

8.1. I2C Communication Sequence Diagram

I²C communication format of HY3118/HY3116 are illustrated below:

a. Data Validity Definition
b. Start and Stop Definition
c. ACK Definition
d. IRQ Definition
e. Wave Definition
f. Write Register
g. Read Register
h. Reread Register

i. Write Register then Read Register
j. IRQ Read Register
k. Call Chip Reset

有效資料定義（Data Validity Definition）

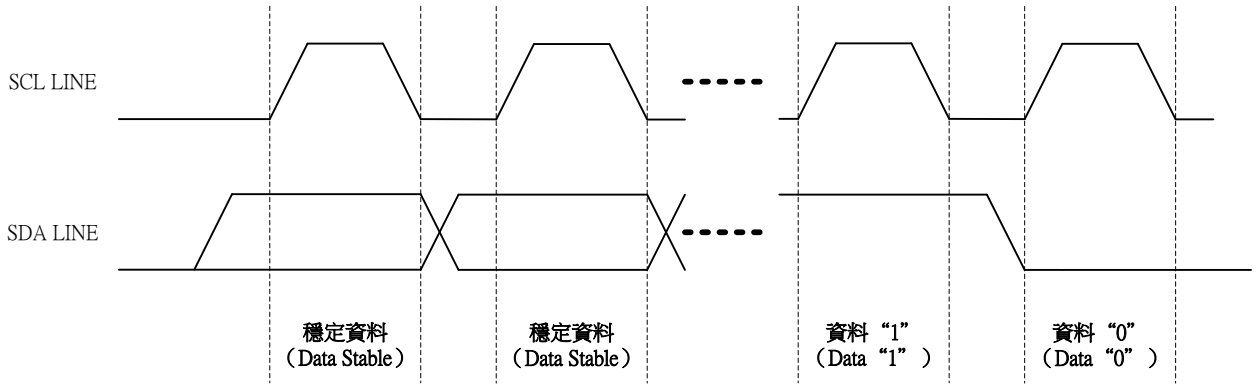


Figure 10 Valid Data Wave Form of Communication I²C

開始與停止定義（Start and Stop Definition）

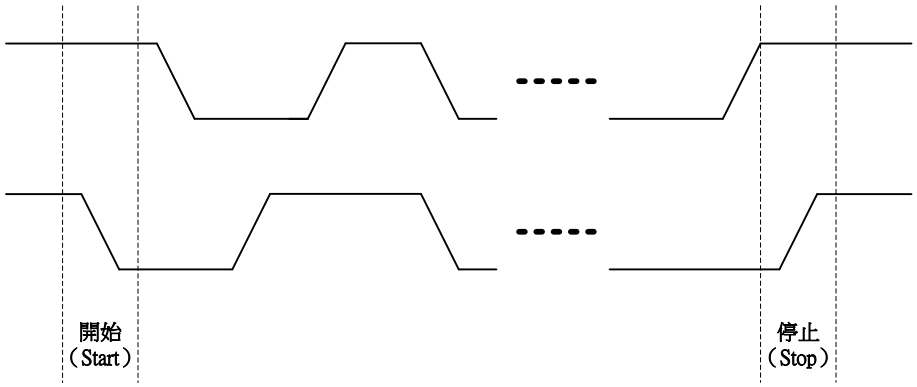
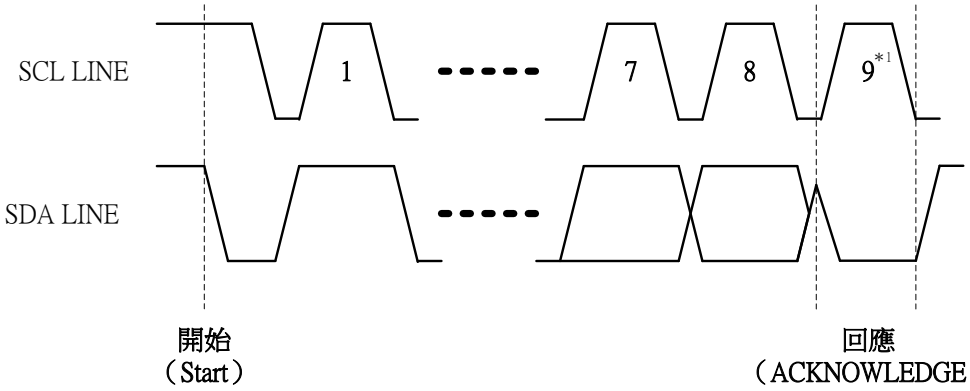


Figure 11 Start and End Wave Form of Communication I²C

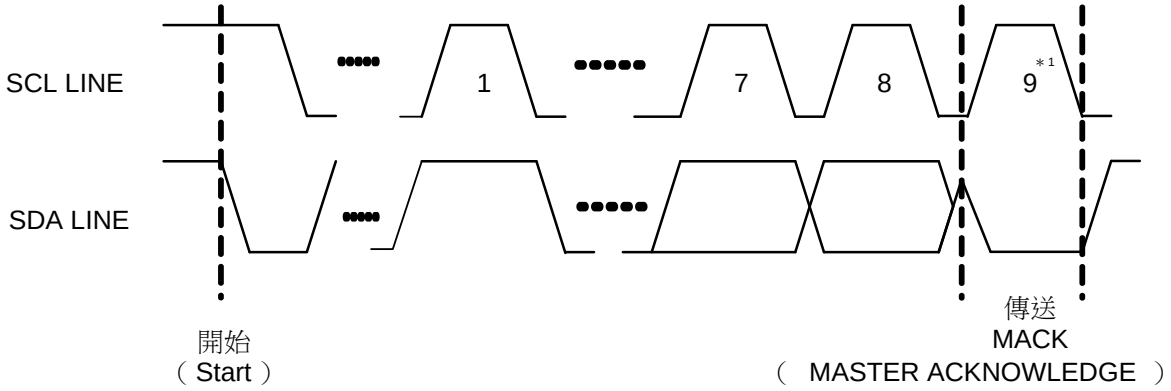
ACK 回應信號定義（ACK Definition）



*1 When the 8th-clocking SCL signal is sent from the mater to the slave end, the master's SDA pin must change from output to input status for receiving the ACK signal sent by the slave end.
When the slave end is set up with ADC IRQ interruption signal, the master's SDA pin must set to input status for receiving the IRQ low potential pulse signal sent by the slave end.

Figure 12 ACK Wave Form of Communication I²C

MACK 傳送信號定義（ MACK Definition ）



*1 MACK occurred when read in values at word address 05h (ADO) and continually read 3 bytes of data output. Before Data 2/Data 3 are outputted, SDA pin must be set to output pin by Master end and set output to low before the 9th-clocking rising edge then notice Slave end so that Data 2/Data 3 can be outputted continually.

Figure 13 MACK Wave Form of Communication I²C

IRQ 中斷信號定義（IRQ Definition）

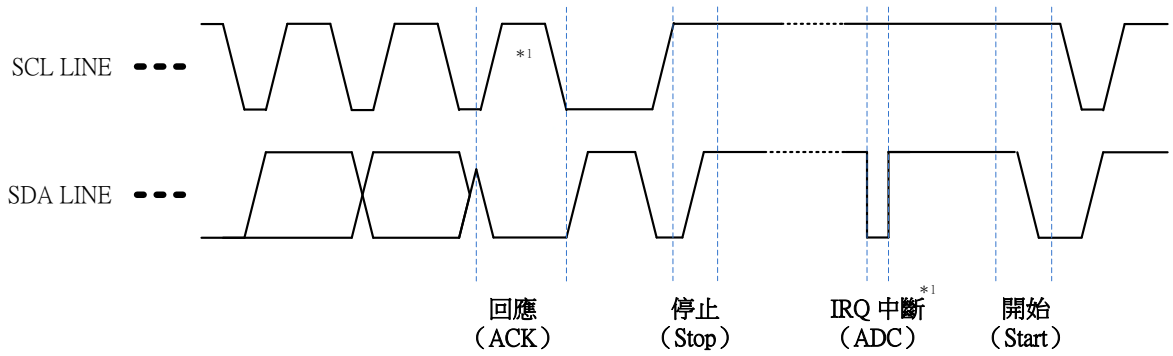


Figure 14 Interruption Wave Form (IRQ) of Communication I²C

波形描述定義（Wave Definition）

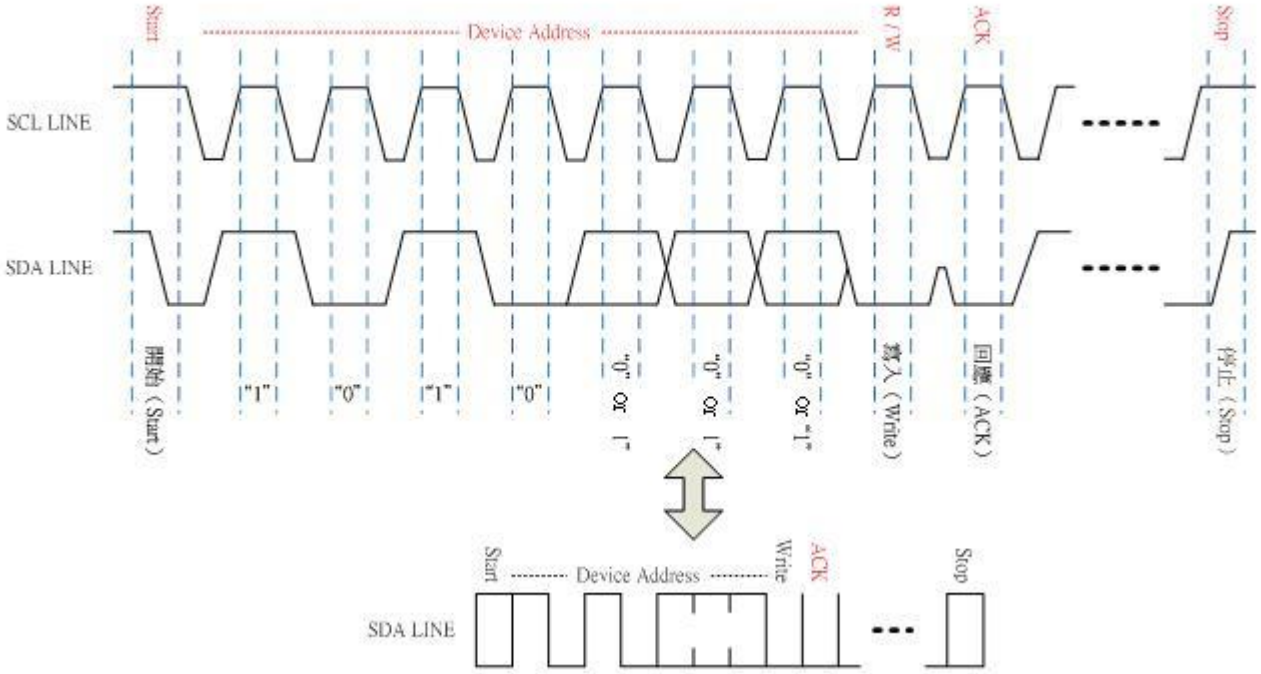
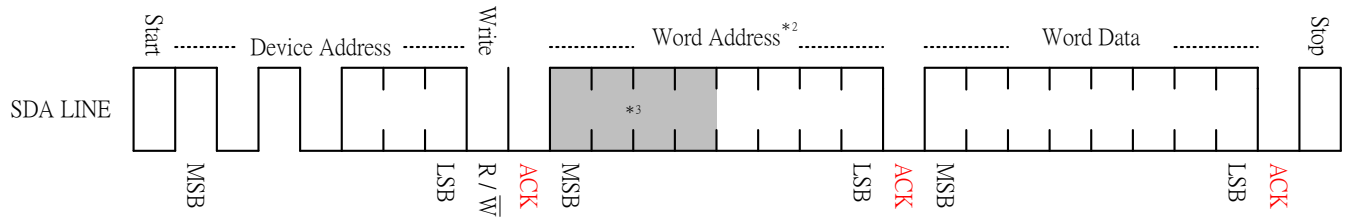


Figure 15 Wave Definition

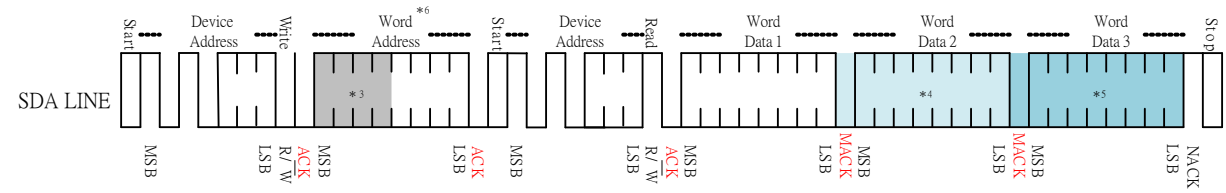
暫存器的寫入（Write Register）



*2 When write-in word address is bigger than 04h, there will be no ACK response and no word address update and the I2C communication will be terminated. Communication resumes after the I2C communication is stopped and started again.
*3 Write-in value of these four bits must all be zero to avoid chip's malfunctioning.

Figure 16 Write Register of Communication I²C

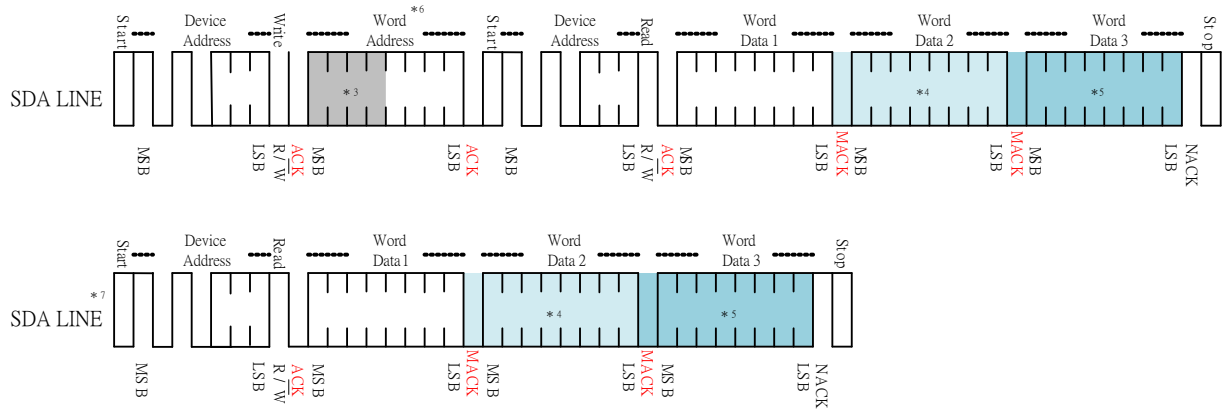
暫存器的讀取（ Read Register)



*4 When read in values at word address 00h ~ 04h the return value is word data 1 only.
*5 When read in values at word address 05h (ADO) the return value is word data 1+word data 2+word data 3. When Data 2/Data 3 have to be returned, MACK has to be set to low by master control terminal.
*6 When read in values at word address bigger than 06h, there will be no ACK response and no word address update and the I2C communication will be terminated. Communication resumes after the I2C communication is stopped and started again.

Figure 17 Read Register of Communication I²C

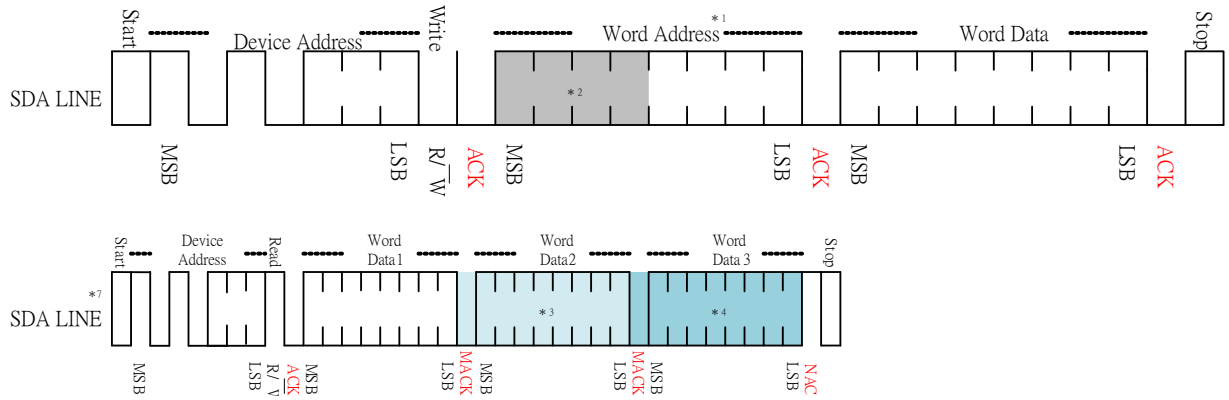
重新讀取暫存器（ Reread Register）



*7 When reading a word address that has been specified for reading once, no assignment are required for the following readings.

Figure 18 Re-read Register of Communication I²C

暫存器的寫入確認（ Write Register then Read Register）



*7 When the word data in a word address that has been specified for writing once, no assignment is required for the following readings.

Figure 19 Write Register then Read Register of Communication I²C

中斷 IRQ的 ADO 暫存器讀取(IRQ Read Register)

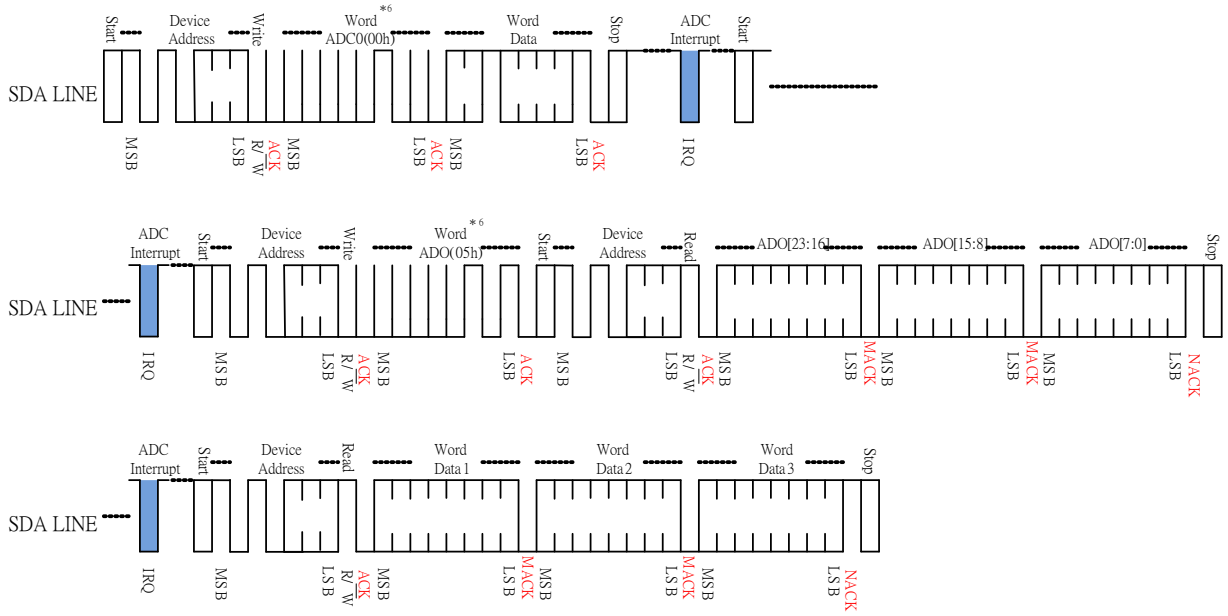


Figure 20 IRQ Read Register

復位晶片 (Call Chip Reset)

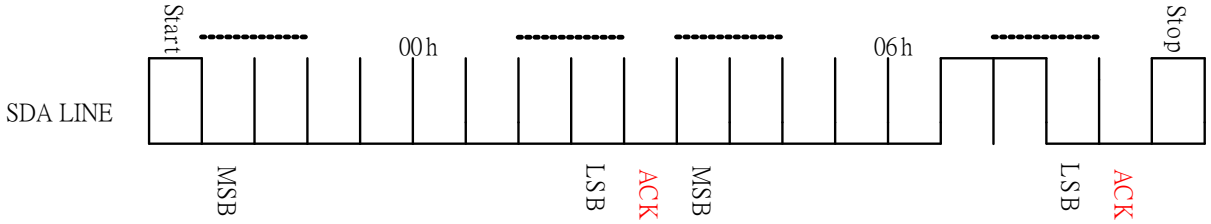


Figure 21 Call Chip Reset of Communication I²C

9. Overview

9.1. Frequency vs. Low Power mode

- Optional internal and external oscillators
  - 327KHz low speed RC oscillator
  - 1000KHz high speed RC oscillator
  - External oscillator through frequency divider of 5 folds frequency elimination
  - External oscillator through frequency divider of 15 folds frequency elimination
  - Programmable operating frequency and ΣΔADC sampling frequency
- Low power mode design
  - Chip sleep mode
  - Auto Power Off mode

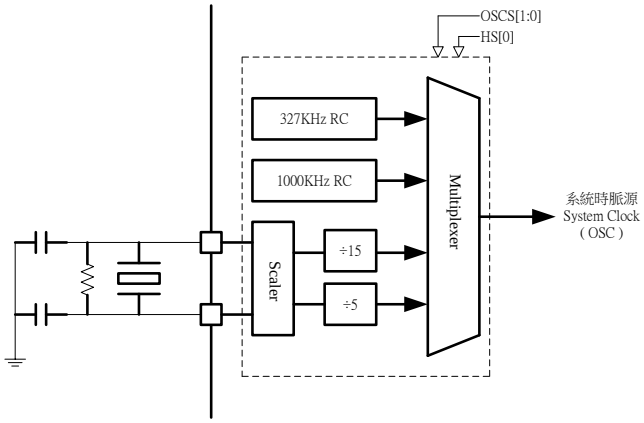


Figure 22 System Clock Diagram

Select system clock (same as ADC sampling rate) by configuring oscillator OSCS[1:0] to generate system's operating frequency (OSC). When sampling frequency of ΣΔADC is running at above 327 KHz, please set value of register HS[0] to "1" to switch to high speed mode. Chip's loss current increases when ΣΔADC is set to high speed mode.

Register / OSC	OSCS[1:0]	00	01	10	11
	HS[0]	0	1	0/1	0/1
System Clock		327KHz	1000KHz	EXO ÷ 15	EXO ÷ 5
ADC Sample Rate					

0/1: Set to "1" when divided frequency of system clock is more than 327KHz.

EXO: frequency of external frequency

Table 11 System Operating Clock and ADC Sampling Frequency

For the 50/60Hz interference caused by AC power, it is recommended to use an external oscillator with crystal frequency of 4.9152MHz as the internal RC oscillator, which tolerance is 5% may lead to poor performance in rejecting AC power interference.

There are two low power modes: auto close and sleep.

- Turn on the "auto close" mode if you want to turn the chip off after the latest ADC data is converted.
  - Set APO[0] to "1" in testing mode to turn on the "auto close" function.
  - Set APO[0] to "1", then the ADC set registers ENLDO[0] and ENADC[0] to "0" after the last ADO[23:0] conversion to switch off chip power and enter sleep mode.

- I2C communication interface is of low power design. Please ensure that the pull-up resistor pin is not at low potential.

◆ Loss current at sleep mode decreases to lower than 1uA. Please follow steps described below to enter this chip into sleep mode:

- Set register ENADC[0] to “0” to power off both internal and external oscillators
- Set register ENOP[0], ENLDO[0] and ENREFO[0] to “0” to power off operation amplifiers OPAMP、VDDA and REFO。
- I2C communication interface is of low power design. Please ensure that the pull-up resistor pin is not at low potential.

9.2. VDDA Power (Low Dropout Regulator)

- 10mA load driving capacity
- Programmable output voltage
- Optional external voltage input
- Low temperature coefficient

VDDA is a voltage source to the ADC, OPAMP and input buffer with low temperature drift coefficient and programmable linear output regulator. Featuring programmable output voltage, 10mA load capacity and low temperature drift coefficient circuit, is perfect in driving small current sensor.

For measuring system that requires shared power supply, users may turn off VDDA and drive with external input voltage. Set register ENLDO[0] to “1” to enable VDDA. Select VDDA’s output voltage through register LDO[1:0].

register / LDO	ENLDO[0]*1	1	1	1	1	0	0	0	0
	LDO[1:0]	00	01	10	11	00	01	10	11
VDDA*1		3.3V	3.0V	2.7V	2.4V	off/EXT			

*1off/EXT: no VDDA output voltage and accept external input voltage

Table 12 Configuration of VDDA’s Output Voltage

9.3. REFO Reference Voltage

- 200uA load driving capacity
- Programmable output voltage
- Optional external voltage input
- Low temperature coefficient

With low temperature drift coefficient and programmable REFO reference voltage output, it suits your needs for reference voltage for it is the power source of analog circuit common ground, programmable output voltage, 200uA load capacity and low temperature drift coefficient circuit design.

For measuring system that requires common reference voltage, you may turn off REFO and drive with external input voltage. Set register ENREFO[0] to “1” to enable REFO. Select REFO’s output voltage through register REFO[0].

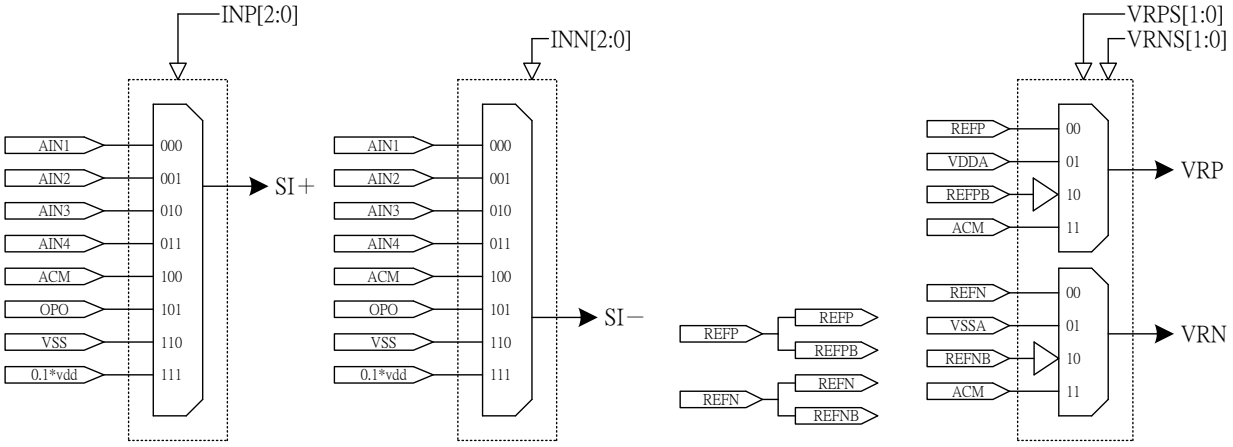
Register / REFO									
	ENREFO[0]*1	1	1			0	0		
	REFO[0]	0	1			0	1		
REFO*1		1.2V	1.5V			off/EXT			

*1off/EXT: no REFO output voltage and accept external input voltage

Table 13 Configuration of REFO’s Output Voltage

9.4. Input Channel Multiplexer with IRQ

- Flexible input multiplexer for measurement and reference signal
- Network switchable input multiplexer design and ADC conversion data suppression function
- Steady time calculation for ADC conversion data suppressed output
- Response IRQ function for end of ADC data conversion



Measurement signal input network　　Reference voltage input network

Figure 23 Input Channel Multiplexer

Signal input is featured with flexible network switchable multiplexer design. After the input network controller is switched, the embedded data conversion suppressor is initiated to delay data update in ADO[23:0] register until ADC data conversion is completed. The data update steady time can be derived from the equation described below:

$$t_{Stable}^{ADC} \cong 128 \times \frac{1}{f_{OSCS}^{ADC}} + 4 \times \frac{1}{f_{OSR}^{ADC}} \quad \text{(Formula 1)}$$

t_{Stable}^{ADC} : steady time after ADC network switch

f_{OSCS}^{ADC} : ADC sampling frequency

f_{OSR}^{ADC} : ADC conversion frequency

If IRQEN<0> of ADC4[7:0] is set to “1”, then a piece of data will be written into register ADO[23:0] and an IRQ signal will be generated at SDA pin. The IRQ signal is a low potential pulse signal that triggers the master end to read contents in ADO[23:0] after being received at the master end.

Please note that after configuration of the input channel multiplexer is switched, both the +/- input short or exchange and reference voltage change need a period of t_{Stable}^{ADC} before the ADC can generate valid conversion data or interruption response IRQ.

9.5. Reference Voltage and its Input Channel with VREF

- Full differential signal input design
- Rail-to-Rail signal input voltage level
- Low-Drift and Low-Noise design
- Programmable reference voltage attenuation factor
- Input buffer design
- Input impedance matching relation

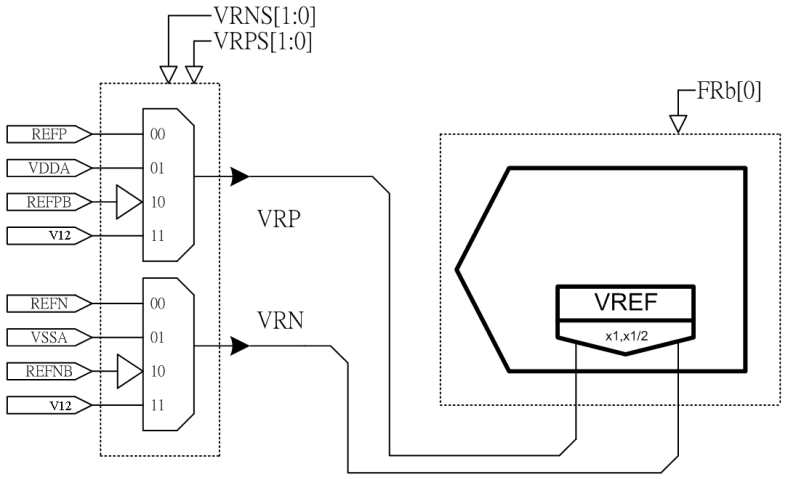


Figure 24 Reference Voltage Input and Attenuator

Reference voltage of full differential input design as well as embedded programmable input attenuator featuring Low-Drift and Low-Noise

The reference voltage input can be configured with proper input channel through multiplexer VRPS[1:0] and VRNS[1:0] as described in Table 14.

Register / Channel	VRPS[1:0] / VRNS[1:0]						
	00	01	10	11			
VRP	REFP	VDDA	REFPB	V12*1			
VRN	REFN	VSSA	REFNB	V12*1			
V12: internal reference voltage 1.2V.							

Table 14 Configuration Table for Measurement Signal Input

△V_{REF} voltage difference is generated based on reference voltage input from pin REFP and REFN. It then generates reference voltage VREF for ΣΔADC, REFP input voltage always bigger than REFN, based on attenuation factor selected by register FRb[0] which is controlled by programmable reference voltage attenuator.

Register / G_{REF}	FRb[0]							
	0	1						
Gain	1	1/2						

Table 15 Cross Reference of Factors of Reference Voltage Attenuator

Value of VREF is derived by formulas described below:

$$\Delta V_{REF} = V_{REFP} - V_{REFN} \quad \text{(Formula 2)}$$

$$VREF = G_{REF} \times \Delta V_{REF} \quad \text{(Formula 3)}$$

ΔV_{REF} : The voltage difference caused by the external input PIN
V_{REFP}、V_{REFN}: The voltage caused by the external input PIN（$V_{REFP} > V_{REFN}$）
G_{REF}: Reference voltage input and attenuator
$VREF$：ADC internal reference voltage

Please note that the design value of input impedance of REFP / REFN is 500KΩ, input voltage to REFP or REFN must be greater than VSS -100mV and less than VDDA +100mV. You may increase the input impedance to REFP and REFN by setting input of VRP / VRN to REFPB / REFNB with the constraint that the input voltage to REFP is greater than 1.2V and the input voltage to REFN is smaller than VDDA - 1.2V.

Signal end / Pin end	VRP	VRN
REFP	VSSA - 0.1V ≦ REFP ≦ VDDA + 0.1V	
REFN	VSSA - 0.1V ≦ REFN ≦ VDDA + 0.1V	
REFPB	VSSA + 0.15V ≦ REFN ≦ VDDA – 1.2V	
REFNB	VSSA + 1.2V ≦ REFP ≦ VDDA – 0.15V	

Table 16 Constraints on Reference Voltage Input

9.6. Measurement Signal Input Channel with PGA

- Full differential signal input design
- Rail-to-Rail signal input voltage level
- Low-Drift and Low-Noise design
- Programmable reference voltage attenuation factor
- Input signal zero offset design
- Minimum resolution signal:100nV$_{RMS}$

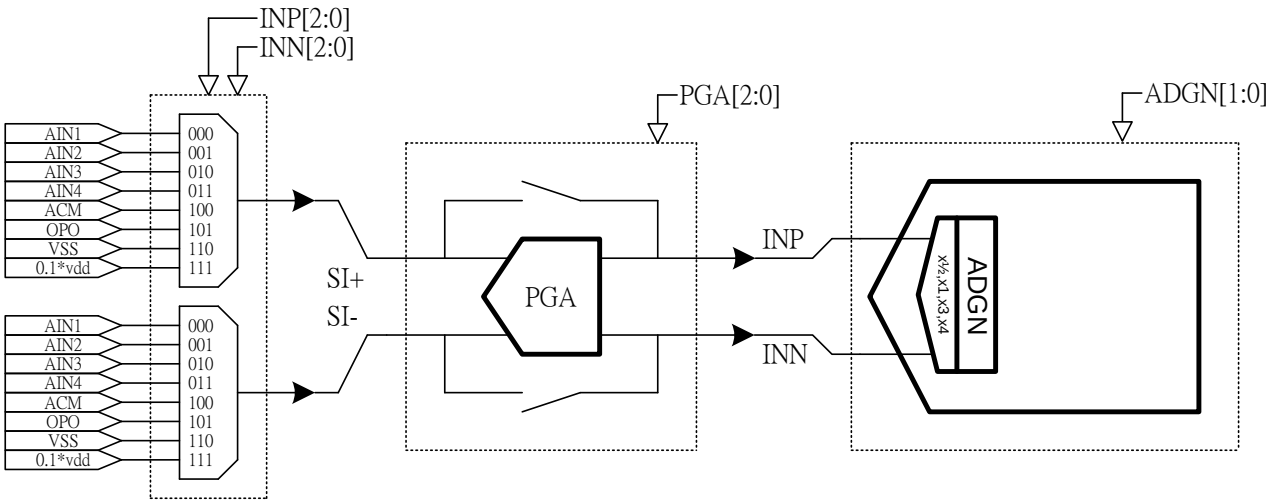


Figure 25 Signal Input and Amplified

Full differential design based signal measurement may be used in the single-end signal measurement. Embedded low-drift and low-noise PGA may reach a minimum signal input resolution at 100nV$_{RMS}$ when input signal is amplified 128 folds (PGA set to 32 folds and ΣΔAD to 4 folds).

Input signal may connect to SI+ or SI- channel through multiplexer. Control register of the multiplexer is INP[2:0] and INN[2:0].

Register / channel	INP[2:0] / INN[2:0]							
	000	001	010	011	100	101	110	111
SI＋	AIN1	AIN2	AIN3	AIN4	REFO	OPO	VSSA	0.1*VDD
SI－	AIN1	AIN2	AIN3	AIN4	REFO	OPO	VSSA	0.1*VDD

Table 17 Cross Reference of Measurement Signal Input Configuration

Amplification rate of input signal is determined by gains from ΣΔAD. Available magnification rates and ranges of input voltage are presented in Table 18, Table 19, and Table 20, Input Impedance generated by different PGA and ΣΔAD Gain Composition is shown as Table 21：

Register / PGA	PGA[2:0]							
	000	001	010	011	100	101	110	111
Gain	off	8	-	16	-	-	-	32

Table 18 Amplification Rate of Input Signal by PGA

Register / ΣΔAD	ADGN[1:0]							
	00	01	10	11				
Gain	1	2	-	4				

Table 19 Amplification Rate of Input Signal by ΣΔAD

Signal end / Pin end	SI+	SI-
AIN0	VSSA - 0.1V ≦ AIN0 ~ AIN3 ≦ VDDA + 0.1V	
AIN1		
AIN2		
AIN3		
VDDA	2.3V ≦ VDDA ≦ 3.6V	
REFO	1.0V ≦ REFO ≦ 1.5V	

Table 20 Attributes of Reference Voltage Input Limit

Gain	=	PGA	×	ADGN	×	FRb	Sensor output impedance(KΩ)
1	=	1	×	1	×	1	200
2	=	1	×	2	×	1	100
4	=	1	×	4	×	1	32
32	=	8	×	4	×	1	4
64	=	16	×	4	×	1	2
128	=	32	×	4	×	1	1

Table 21 Input Impedance generated by PGA and ΣΔAD Gain

All the application input signals of different measurements are attributed with zero offset (translation adjustment). You may change location of the input signal's zero point to improve the maximum measurement range overflow caused by too large an input offset voltage from the sensor. See Figure 25 for an illustration on 16-bit (±15-bit) sampling to a measurement signal. Before doing a zero shift adjustment, overflow in the full range exists, but not after running a -1/4 VREF zero offset alignment.

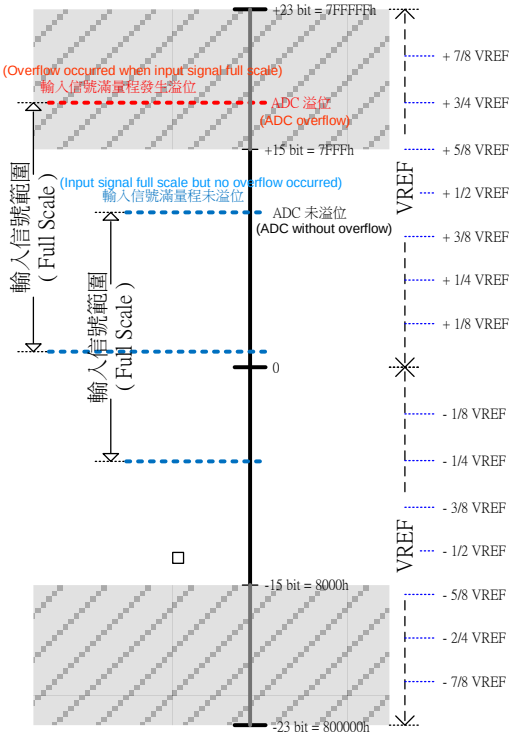


Figure 26 Overflow Treatment of 16 Effective Bits

9.7. COMB Filter

- 3-tier COMB filter
- Programmable over sampling frequency
- AC frequency interference suppression

3-tier digital filter based ΣΔADC can get different data conversion frequency by changing settings of OSR[2:0].

Register / OSR	OSR[2:0]							
	000	001	010	011	100	101	110	111
OSR	128	256	512	1024	2048	4096	8192	32768

Table 21 Frequency Division for Over-sampling Frequency

OSCS / HS / OSR		00	01	10	11	OSCS[1:0]
		0	1	1	0	HS[0]
OSR[2:0]	000	2500	7812.5	7680	2560	EXO: external 4.9152MHz crystal oscillator
	001	1250	3906.2	3840	1280	
	010	625	1953.1	1920	640	
	011	312.5	976.5	960	320	
	100	156.2	488.2	480	160	
	101	78.1	244.1	240	80	
	110	39	122	120	40	
	111	9.7	30.5	30	10	

Table 22 ΣΔADC Over-sampling Conversion Frequency

For a 4.9152MHz external oscillator the output frequency of ΣΔADC may range in 2560, 640, 80 and 10Hz. See Figure 26 for suppression of the 10SPS frequency response to the 50/60Hz interference from AC power.

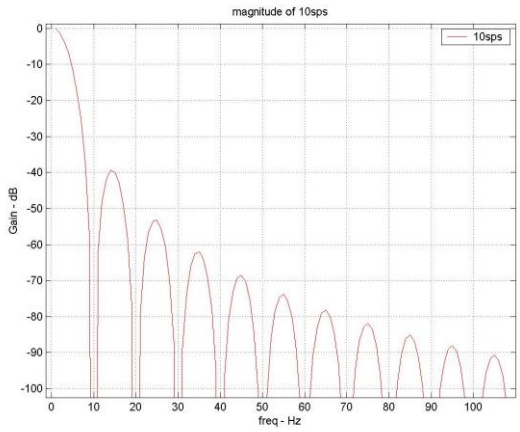


Figure 27 10SPS Frequency Response

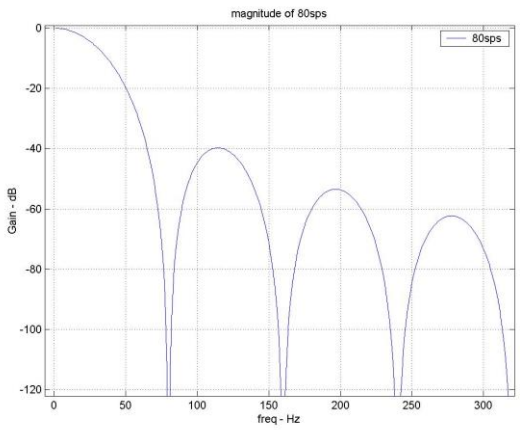


Figure 28 80SPS Frequency Response

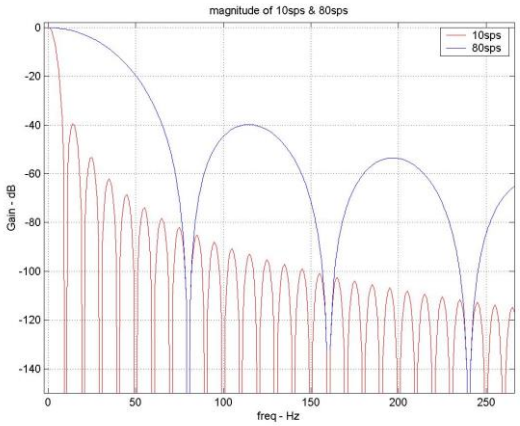


Figure 29 10/80SPS Frequency Response

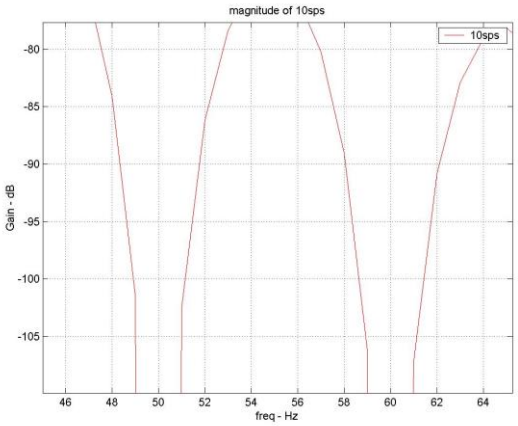


Figure 30 Magnified 10SPS Frequency Response

9.8. Data Conversion Format

- ADO register
- 24-bit data length
- Bi-polar output
- Two's complement format

Data converted by COMB filter is saved in the ADO register. The converted external input signal is stored in ADO[23:0]. See Figure 30 for data format of ADO[23:0] where ADO[23:1] is ADC's conversion output and ADO[0] the read status flag, ADST[0], of ADO.

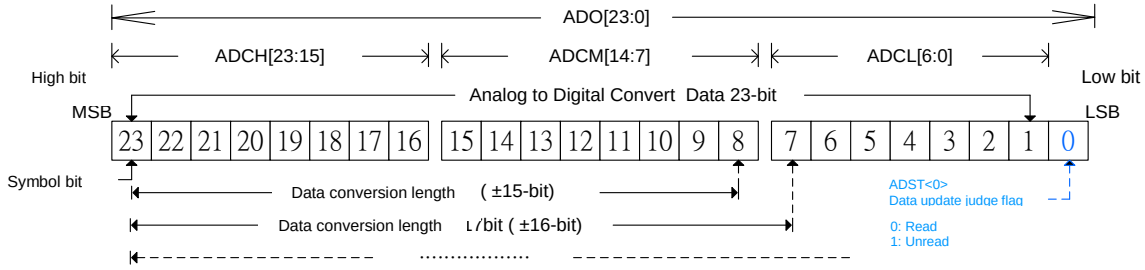


Figure 31 ADO Data Conversion Format

	Equivalent test pending signal	ADO[23:0]	
		hexadecimal	Binary coded decimal
Bipolar output Two's complement format	△VR	7F FF FE	0111-1111 1111-1111 1111-111x
	△VR*(1/2^{22})	00 00 02	0000-0000 0000-0000 0000-001x
	0	00 00 00	0000-0000 0000-0000 0000-000x
	-△VR*(1/2^{22})	FF FF FE	1111-1111 1111-1111 1111-111x
	-△VR	80 00 00	1000-0000 0000-0000 0000-000x

Table 23 Relation between ADO[23:0] and Input Signal

9.9. Rail-to-Rail OPAMP

- Rail-to-Rail signal input design
- 1mA I/O current

Rail-to-Rail OPAMP design with 90dB DC gain and 70dB CMRR for a maximum of 1uF capacitive load. Voltage range of the ORAMP's input signal can be found in Table 14.

Signal / OPAMP	Range of OPAMP input voltage
OPP	VSSA ≦ OPP ≦ VDDA
OPN	VSSA ≦ OPN ≦ VDDA

Table 24 Constraints on Reference Voltage Input

Output voltage of ORAMP OPO is smaller than 0.3V or greater than VDDA - 0.3V. Output impedance of ORAMP may increase. Figure 31 is the change curve of OPO output impedance when ORAMP is set to a unit gain buffer.

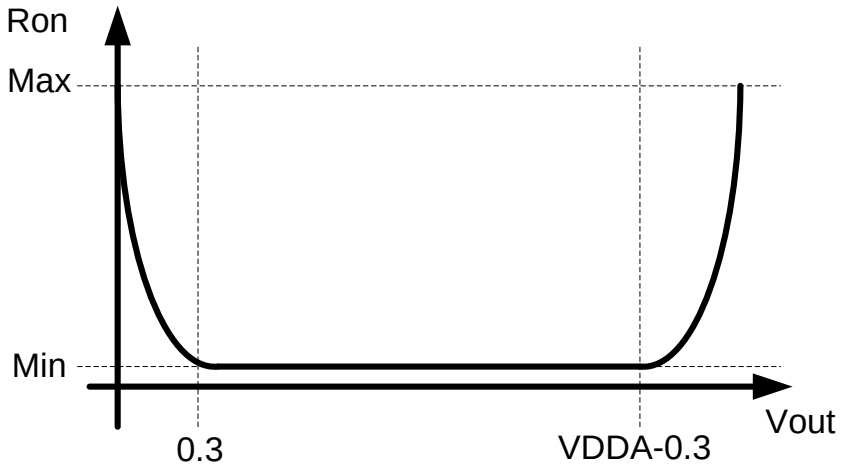


Figure 32 Change Curve of OPO Output Impedance

You may set ENOP[0] to "1" to use the Rail-to-Rail ORAMP. Please make sure that the VDDA is set to ON when using the ORAMP. The OPO output signal can be detected by ADC only by setting up register INP[2:0] and INN[2:0].

10. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Shipment Packing Type	Unit Q'ty	Material Composition	MSL[2]
HY3118-E016	SSOP	16	E	016	Tube	100	Green[3]	MSL-3
HY3118-E016	SSOP	16	E	016	Tape & Reel	2500	Green[3]	MSL-3
HY3116-M010	MSOP	10	M	010	Tape & Reel	3000	Green[3]	MSL-3

[1] **Device No.: Model No. – Package Type Description (Standard Code)**

Ex: You request HY3118 in SSOP16 package and shipment packing type is Tube. The device number will be HY3118-E016. And please clearly indicate the shipment packing type (Tube) when placing orders.

Ex: You request HY3116 in MSOP10 package and shipment packing type is Tape & Reel. The device number will be HY3116-M010. And please clearly indicate the shipment packing type (Tape & Reel) when placing orders.

[2] **MSL:**

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

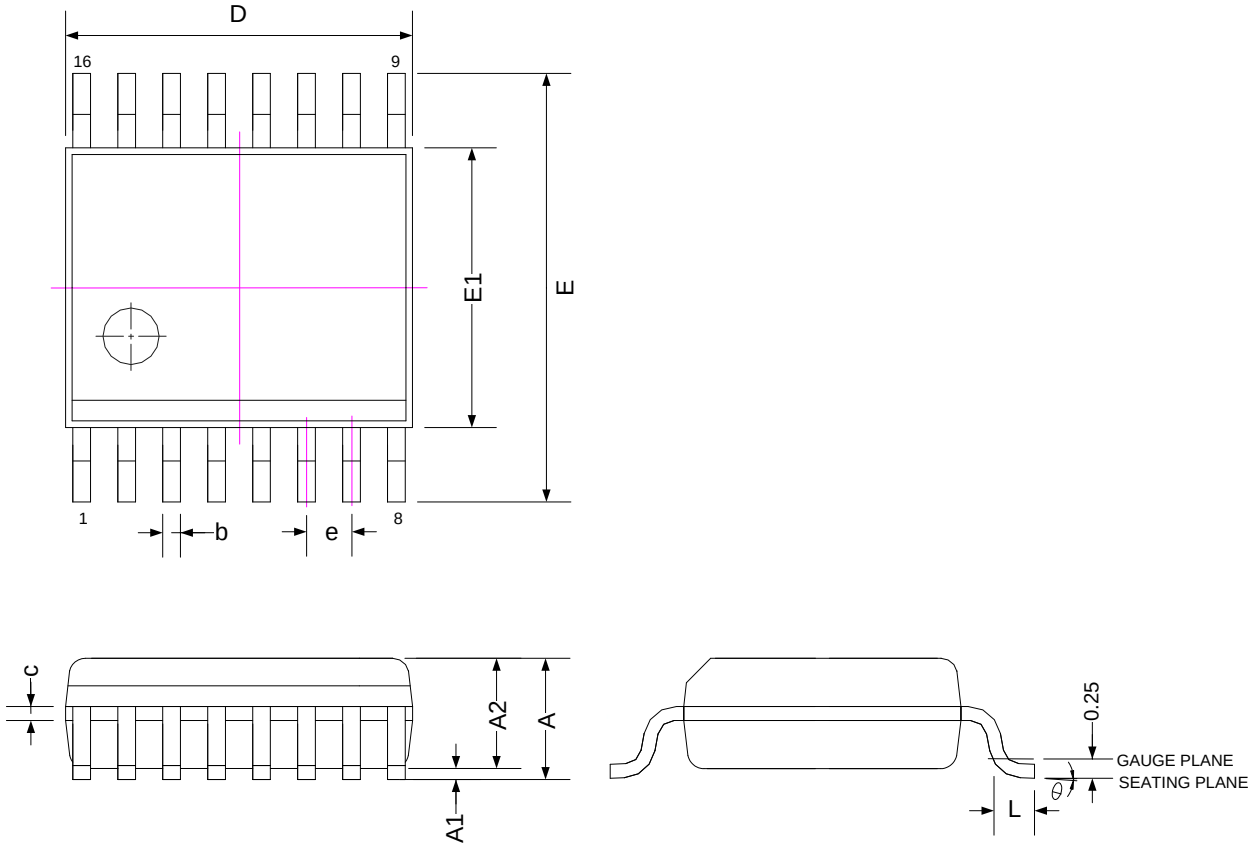
[3] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that are compliant with RoHS directive, SVHC under REACH and Halogen free.

11. Package Information

11.1. SSOP16

11.1.1. Package Dimensions

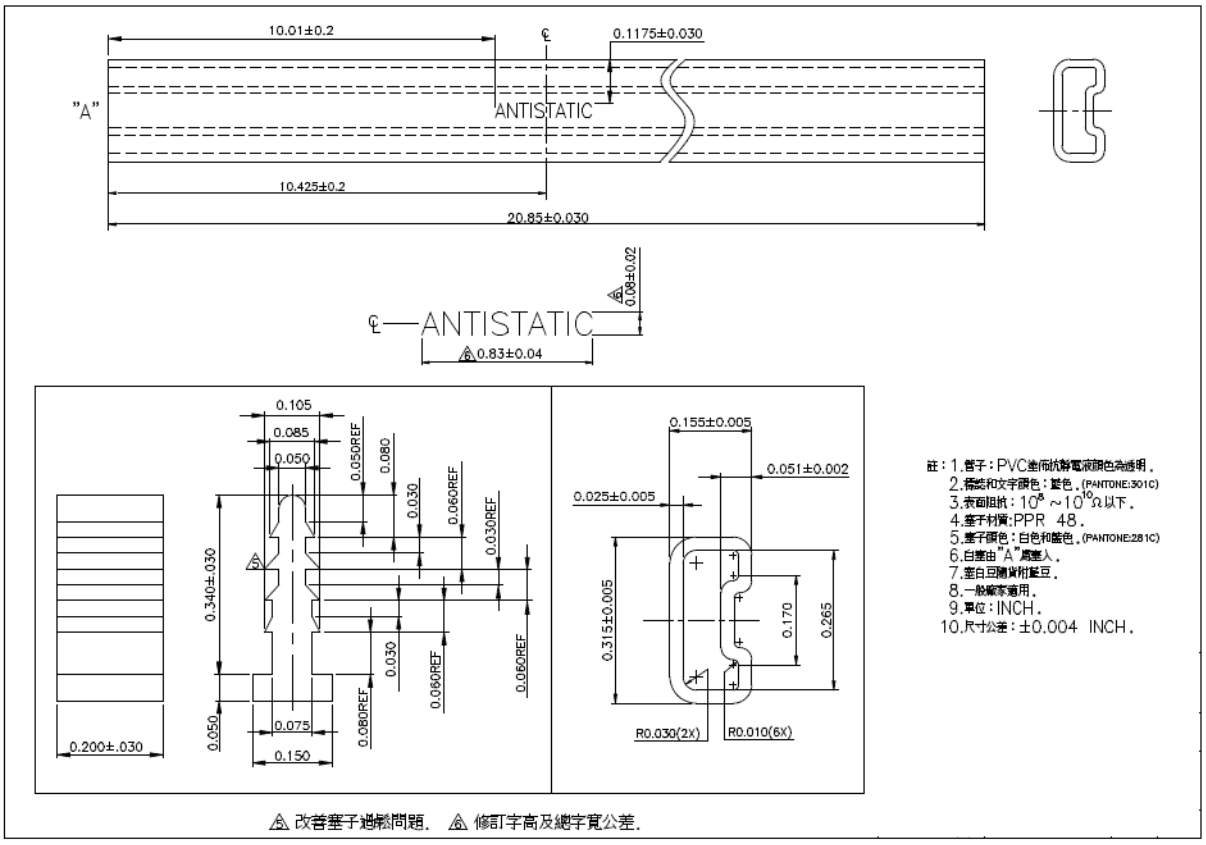


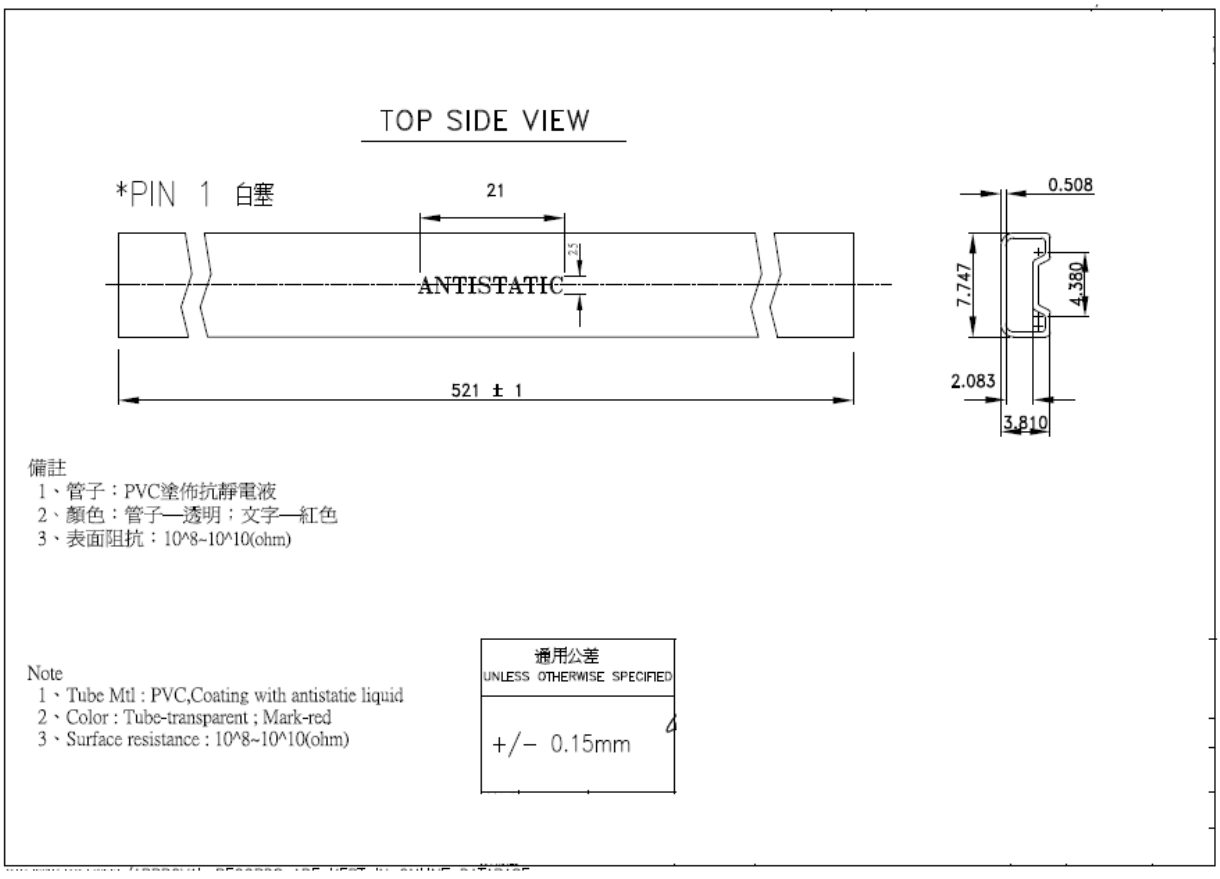
SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	4.80	4.90	5.00
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	-	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit : mm

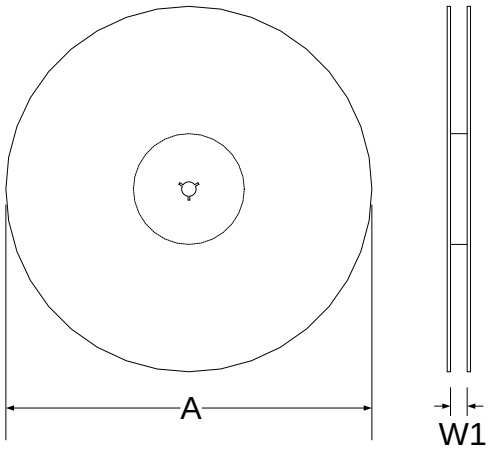
11.1.2. Tube Dimensions



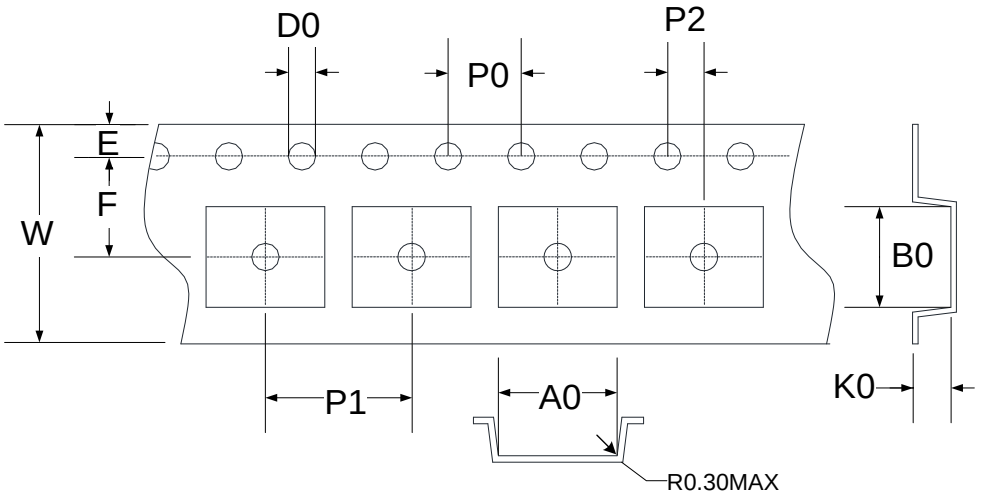


11.1.3. Tape & Reel Information

11.1.3.1. Reel Dimensions-Type 1…….…….. Unit : mm



11.1.3.2. Carrier Tape Dimensions

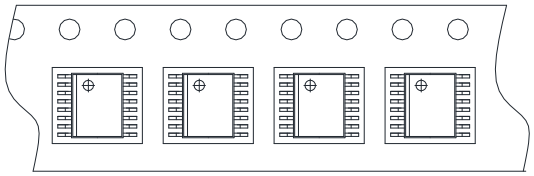


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

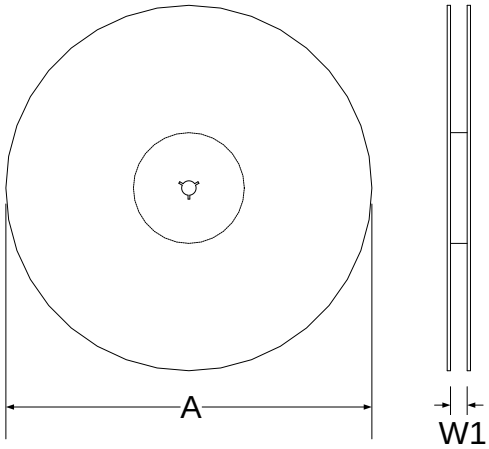
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

Unit : mm

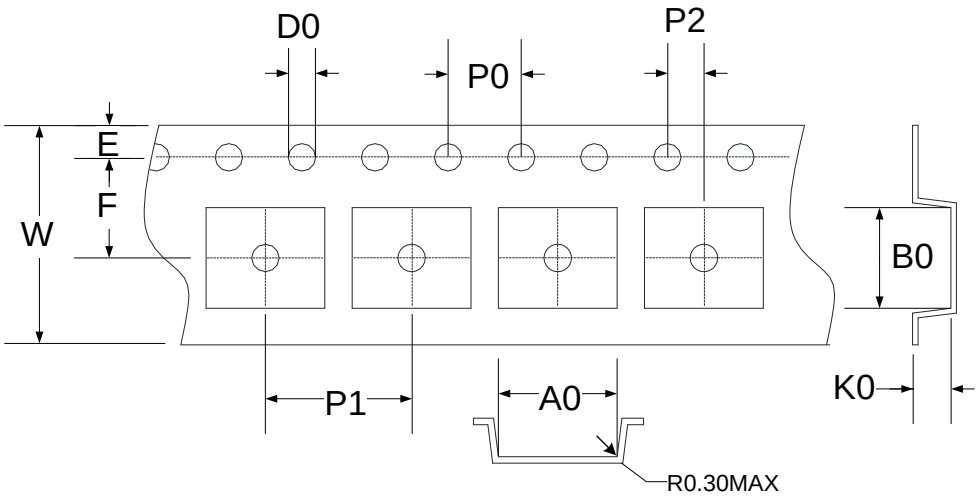
11.1.3.3. Pin1 direction



11.1.3.4. Reel Dimensions-Type 2…….…….. Unit : mm



11.1.3.5. Carrier Tape Dimensions

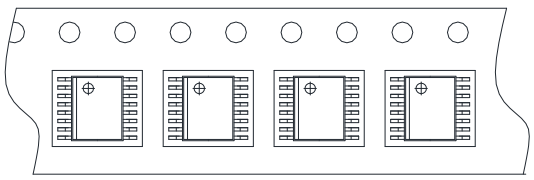


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.50	5.20	2.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

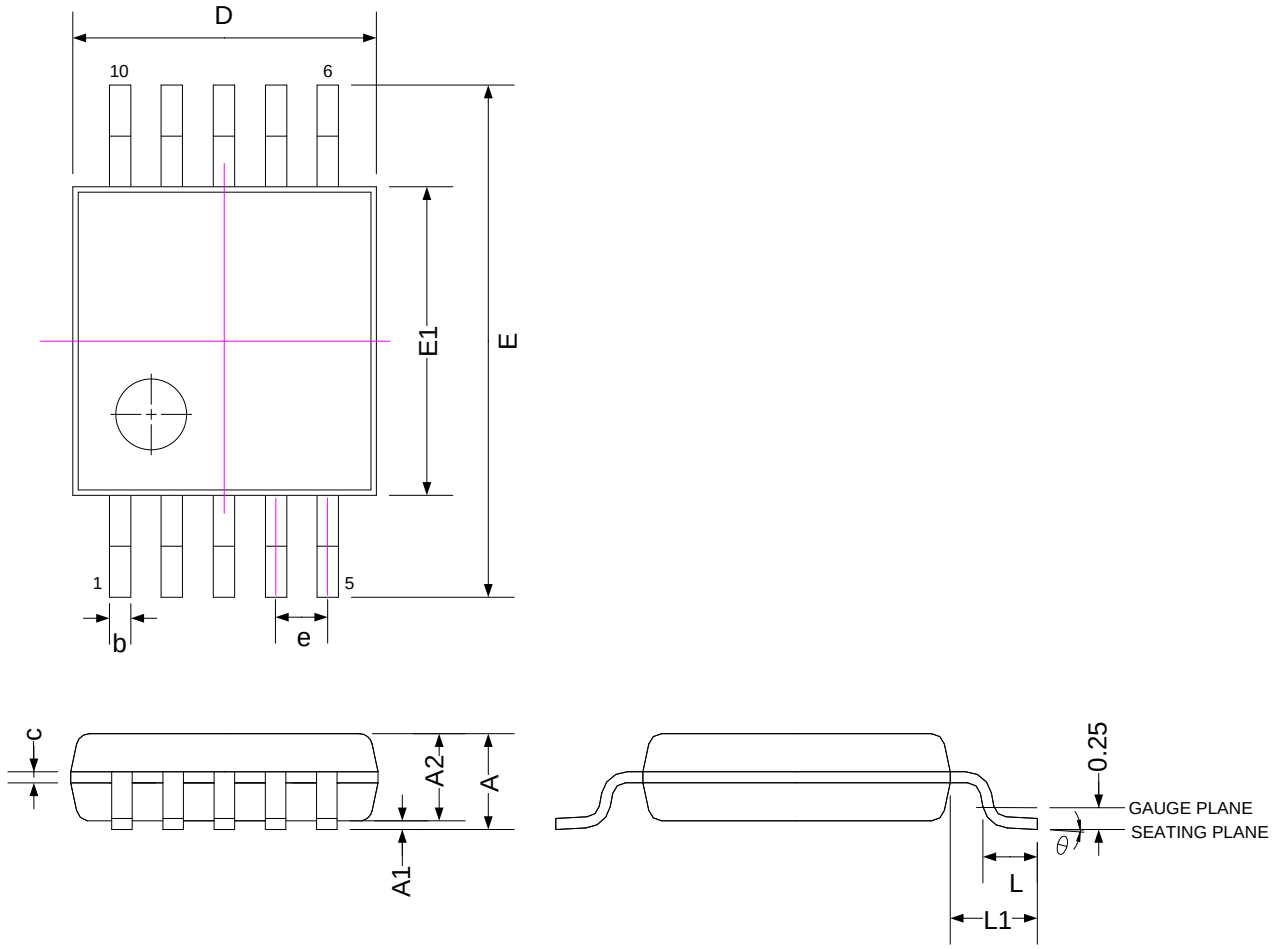
Unit : mm

11.1.3.6. Pin1 direction



11.2. MSOP10

11.2.1. Package Dimensions



SYMBOLS	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.10	0.15
A2	0.75	0.85	0.95
b	0.17	0.20	0.27
c	0.08	0.15	0.23
D	3.00 BASIC		
E1	3.00 BASIC		
E	4.90 BASIC		
L	0.40	0.60	0.80
L1	0.95 REF		
e	0.50 BASIC		
θ°	0	-	8

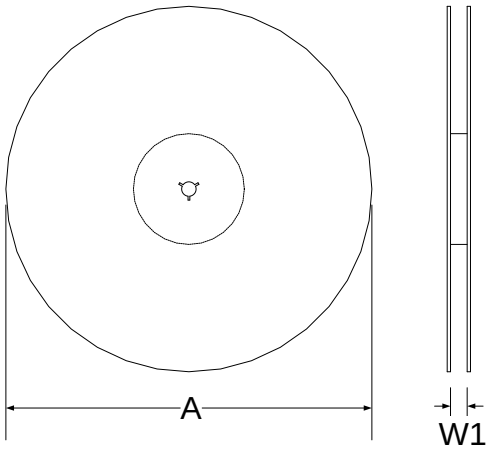
*Note:

1.All dimensions refer to JEDEC OUTLINE MO -187.

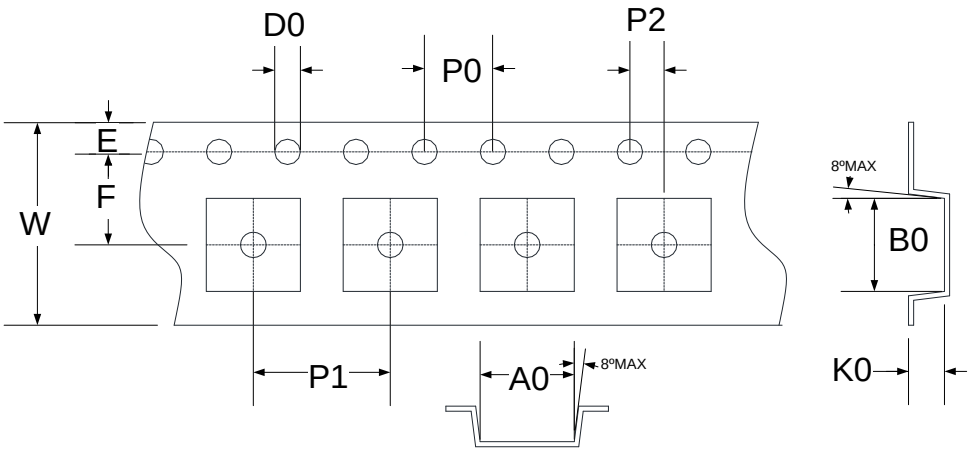
2.Do not include Mold Flash or Protrusions.

11.2.2. Tape & Reel Information

11.2.2.1. Reel Dimensions-Type 1…….……..…….. Unit : mm



11.2.2.2. Carrier Tape Dimensions

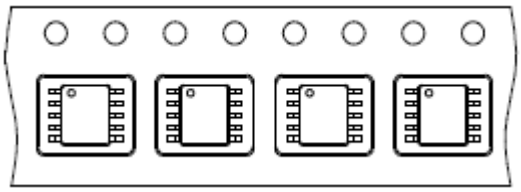


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	5.30	3.40	1.40	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	±2.00	±1.50	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.20

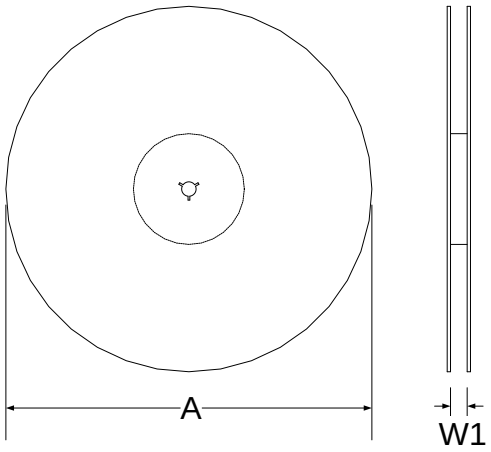
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

Unit : mm

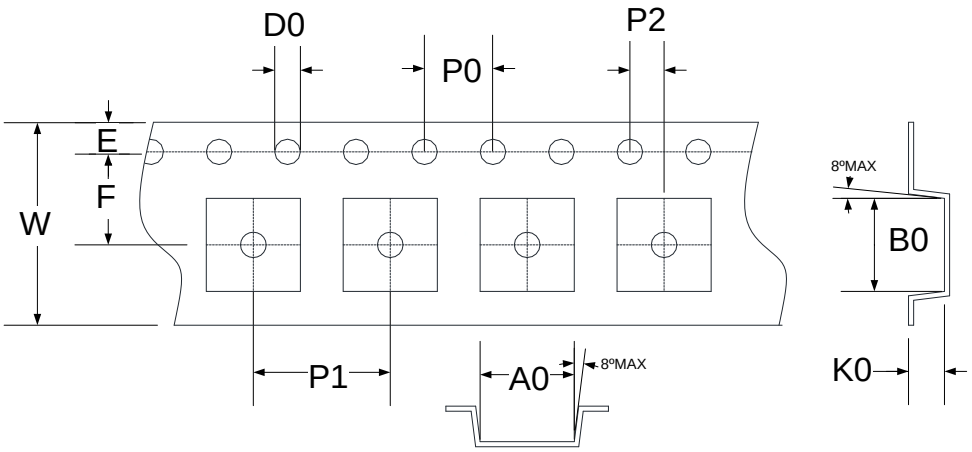
11.2.2.3. Pin1 direction



11.2.2.4. Reel Dimensions-Type 2…….…….. Unit : mm



11.2.2.5. Carrier Tape Dimensions

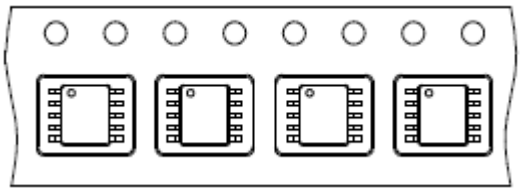


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	5.20	3.30	1.20	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	±2.00	±1.50	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

Unit : mm

11.2.2.6. Pin1 direction



12. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V04	All	First Edition
V05	45	The MSOP10 package type revision
	23	Revise the description of I^2C communication protocol
	26	Add Figure 33 MACK Wave Form of Communication I^2C
	27~29	Update Figure 17~Figure 21 (ACK -> MACK)
V07	44	Add in SSOP16 package information
V08	37~38	Add Input Impedance Table
V09	9	Update Package marker information
	45	Update Green (RoHS & no Cl/Br)
	47	Update Tube Dimensions
	48~49	Update Tape & Reel Information
	51~52	Update Tape & Reel Information
V10	12	Corrected bit description of the ADC1 register in Section 5.2.2
	11~15	Correct the address of the register
V11	11	Correct Ch5.1&Ch5.2.2 Register List, register name ADC1 control bits INP and INN swap